PS01TR01

IEEE 802.11B(G) Compliant 2.4GHz WLAN Transceiver

FEATURES

- **IEEE 802.11B Compliant**
  - **Supports CCK/DSSS Modes**
  - **1, 2, 5.5, 11Mbps (CCK / DSSSS / PBCC)**
  - **6, 9, 12, 18, 24, 36, 48, 54Mbps (OFDM)**
- **High Level of Integration**
  - **Integrated VCO / Synthesizer**
  - **Integrated LNA**
  - **Integrated Power Amplifier**
  - **SuperHeterodyne Architecture**
  - **Single Chip With External SAW Filter**
  - **All CMOS Implementation**
- **Receiver Sensitivity**
  - **CCK: -82dBm**
  - **DSSS: -90dBm**
- **Transmitter Power**
  - **+22dBm @ P1dB**
- **Available Package**
  - **48-Pin QFN (7mm x 7mm)**

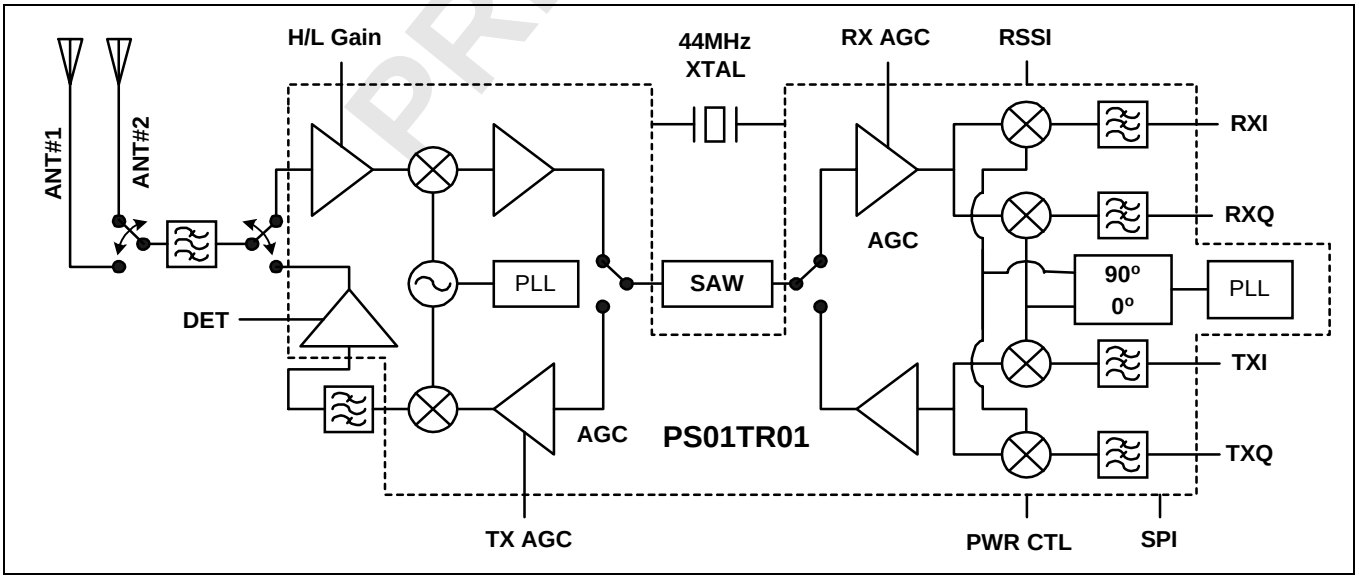
PRODUCT DESCRIPTION

The PS01TR01 is a highly integrated CMOS single transceiver chip solution for 802.11B(G) WLAN applications. The transceiver is fully compliant with IEEE 802.11B(G) standards. It supports both PFDM and CCK/DSSS/PBCC mode.

The chip is a high performance and low DC power consumption SuperHeterodyne architecture. It requires only one external SAW filter for channel filtering. The transceiver does not require RF balun for the receive input and transmit output. The baseband IQ input and output are differential and DC coupled. The receiver provides 100dB AGC range -30dB in the LNA and 70dB in the IF amplifier. The transceiver has power saving mode build-in. At 3.3V power supply, the radio power consumption during receive mode is typically 51mA and 53mA in transmit mode. THe power amplifier draws typically 250mA. The low receive power consumption makes this chip ideal for portable wireless applications such as PDA, cellular phone, and laptop computers.

The chip comes in a 48-pin QFN.

CHIP BLOCK DIAGRAM



PIN ASSIGNMENT AND DESCRIPTION

Pin	Function	Description	Interface
1	TX_UPC_VDD	Transmit upconverter positive power supply	2.7V~3.6V
2	TA_FLT_OUT	Transmit upconverter output to image filter	50Ω output
3	LNA_VDD	Receiver low noise amplifier positive power supply	2.7V~3.6V
4	GND	Ground	
5	RFIN	Receiver low noise amplifier input	50Ω output
6	GND	Ground	
7	TX_FLT_IN	Transmit power amplifier input from image filter	50Ω output
8	RFAGC_CTL	Receiver low noise amplifier High/Low gain select input	CMOS logic input
9	TX_RFA_VDD	Transmit pre-amplifier positive power supply	2.7V~3.6V
10	TX_PA_PD	Transmit power amplifier power down control	Shunt capacitor
11	TX_PA_VDD1	Transmit power amplifier positive power supply, 1st stage	2.7V~3.6V
12	TX_PA_DET	transmit power detector output	1.5V to 2V
13	TX_PA_OUT	Transmit power amplifier output	50Ω output
14	TX_PA_VDD2	transmit power amplifier positive power supply	2.7V~3.6V
15	REF_IN	44MHz reference clock in or 44MHz crystal	CMOS logic input
16	REF_OUT	44MHz reference clock out or 44MHz crystal	CMOS logic output
17	RF_PLL_VDD	RF phase locked loop digital positive power supply	2.7V~3.6V
18	TX_IP	Baseband in-phase transmit positive input	1.2V input com. mode
19	TX_IN	Baseband in-phase transmit negative input	1.2V input com. mode
20	TX_QN	Baseband quadrature-phase transmit negative input	1.2V input com. mode
21	TX_QP	Baseband quadrature-phase transmit positive input	1.2V input com. mode
22	TX_LPF_VDD	Baseband transmit low pass filter positive power supply	2.7V~3.6V
23	IF_PLL_VDD	IF phase locked loop positive power supply	2.7V~3.6V
24	TX_IF_VDD2	Baseband IF transmit amplifier positive power supply	2.7V~3.6V
25	BB_IFP	Baseband IF positive input/output from/to SAW filter	900Ω differential
26	BB_IFN	Baseband IF negative input/output from/to SAW filter	900Ω differential
27	RX_AGC_VDD1	RX IF AGC amplifier (1) positive power supply	2.7V~3.6V
28	RX_VAGC	RX IF AGC amplifier gain control input	0.8V~2.2V
29	RX_AGC_VDD2	RX IF AGC amplifier (2) and demodulator positive power supply	2.7V~3.6V
30	LD	RF and IF synthesizers' lock detect output	CMOS logic output
31	RX_IP	Baseband in-phase receive positive output	1.2/1.7V output com. mode
32	RX_IN	Baseband in-phase receive negative output	1.2/1.7V output com. mode
33	TX_QP	Baseband quadrature-phase receive positive output	1.2/1.7V output com. mode

Pin	Function	Description	Interface
34	RX_QN	Baseband quadrature-phase receive negative output	1.2/1.7V output com. mode
35	PE1	Radio power control logic input (1)	CMOS logic input
36	PE2	Radio power control logic input (2)	CMOS logic input
37	RX_LPF_VDD	Baseband receive low pass filter positive power supply	2.7V~3.6V
38	CMREF	Common reference voltage for baseband receive output	1.2/1.7V
39	LE	Latch enable input for radio register programming	CMOS logic input
40	CLK	Clock input for radio register programming	CMOS logic input
41	Data	Data input for radio register programming	CMOS logic input
42	RF_CP_DO	RF phase locked loop charge pump output	0.5V~2.5V
43	RF_VCO_VDD	RF phase locked loop VCO positive power supply	2.7V~3.6V
44	RF_VCO_TUNE	RF phase locked loop VCO frequency tuning input	0.5V~2.5V
45	RF_IFN	RF IF negative input/output from/to SAW filter	800Ω differential
46	RF_IFP	RF IF positive input/output from/to SAW filter	800Ω differential
47	RF_IF_VDD	RF transmit and receive IF amplifier positive power supply	2.7V~3.6V
48	TX_IF_AGC	TX IF AGC amplifier gain control input	0.8V~2.2V

BASEBAND INTERFACE SPECIFICATIONS

Pin	Function	Description	Interface
8	RFAGC_CTL	Min. High = Vdd-0.2V Max. Low = 0.2V	Settling Time: 100ns Input Impedance = 1MΩ || 5pF
10	TX_PA_PD	Internal 4KΩ + external shunt capacitor set power ramp up and ramp down timing	68pF
12	TX_PA_DET	Min. output = 1.5V Max. output = 2.2V	Slope = Positive Settling Time = 10µS Load Impedance = 15pF
16	REF_OUT	Min. High = Vdd-0.2V Max. Low = 0.2V	44MHz output Ouput Load: 15pF
18	TX_IP	1.2±0.1V common mode input 50±25mVp signal input	Max. differential offset = 5mV Input Impedance = 1MΩ || 5pF
19	TX_IN	1.2±0.1V common mode input 50±25mVp signal input	Max. differential offset = 5mV Input Impedance = 1MΩ || 5pF
20	TX_QP	1.2±0.1V common mode input 50±25mVp signal input	Max. differential offset = 5mV Input Impedance = 1MΩ || 5pF
21	TX_QN	1.2±0.1V common mode input 50±25mVp signal input	Max. differential offset = 5mV Input Impedance = 1MΩ || 5pF
28	RX_VAGC	Min. input = 0.5V Max. input = 2.2V Gain range = -5dB to 75dB	Slope = Negative Max. TX/RX settling time = 500ns Max. VAGC settling time = 300ns Input Impedance = 1MΩ || 5pF

Pin	Function	Description	Interface
30	LD	Min. High = Vdd-0.2V Max. Low = 0.2V	Lock = High Load Inpedance = 15pF
31	RX_IP	1.2(1.7)±0.1V common mode output 500±250mVp signal output	Max. differential offset = 20mV Load Impedance = 10pF
32	RX_IN	1.2(1.7)±0.1V common mode output 500±250mVp signal output	Max. differential offset = 20mV Load Impedance = 10pF
33	RX_QP	1.2(1.7)±0.1V common mode output 500±250mVp signal output	Max. differential offset = 20mV Load Impedance = 10pF
34	RX_QN	1.2(1.7)±0.1V common mode output 500±250mVp signal output	Max. differential offset = 20mV Load Impedance = 10pF
35	PE1	Min. High = Vdd-0.2V Max. Low = 0.2V	See power enable table Input Impedance = 1MΩ || 5pF
36	PE2	Min. High = Vdd-0.2V Max. Low = 0.2V	See power enable table Input Impedance = 1MΩ || 5pF
38	CMREF	Mode1 = 1.2±0.1V Mode2 = 1.7±0.1V	Mode1 and Mode1 selectable through a register Input Impedance = 1MΩ || 15pF
39	LE	Min. High = Vdd-0.2V Max. Low = 0.2V	CMOS logic input Input Impedance = 1MΩ || 5pF
40	CLK	Min. High = Vdd-0.2V Max. Low = 0.2V	CMOS logic input Input Impedance = 1MΩ || 5pF
41	DATA	Min. High = Vdd-0.2V Max. Low = 0.2V	CMOS logic input Input Impedance = 1MΩ || 5pF
48	TX_IF_AGC	Min. input = 0.5V Max. input = 2.2V Gain range = 0dB to 30dB	Slope = Negative Max. TX/RX settling time = 500ns Max. VAGC settling time = 300ns Input Impedance = 1MΩ || 5pF

PS01TR01 POWER CONTROL INTERFACE SPECIFICATIONS

PE1	PE2	M(2) (PLL_PE) (Serial Bus)	Interface
0	0	1	Power Down State, PLL Registers in Save Mode, Inactive PLL, Active Serial Interface
0	1	1	Receive State, Active PLL. Receive ready in 2µS
1	0	1	Transmit State, Active PLL. Receive ready in 2µS
1	1	1	Inactive Transmit and Receive States, Active PLL, Active Serial Interface
X	X	0	Power Down State, Inactive PLL, Active Serial Interface

PS01TR01 REGISTER MAP

PLLs Programming	PLLs Programming + Operational Mode	Receive Offset Calibration + Operational Mode	Transmit Offset Calibration + Filter BW Selection	Serial Bits
0	0	1	1	LSB1
0	1	0	1	2
A(0)	RR(6)	CR(0)	CT(0)	3
A(1)	IN(0)	CR(1)	CT(1)	4
A(2)	IN(1)	CR(2)	CT(2)	5
A(3)	IN(2)	CR(3)	C4(3)	6
A(4)	IN(3)	CR(4)	CT(4)	7
B(0)	IN(4)	CR(5)	CT(5)	8
B(1)	IN(5)	CR(6)	CT(6)	9
B(2)	IR(0)	CR(7)	CT(7)	10
B(3)	IR(1)	X	X	11
B(4)	IR(2)	X	X	12
B(5)	IR(3)	X	X	13
B(6)	M(0)	X	X	14
RR(0)	M(1)	R(0)	T(0)	15
RR(1)	M(2)	R(1)	T(1)	16
RR(2)	DCT	R(2)	T(2)	17
RR(3)	DCR	R(3)	T(3)	18
RR(4)	DEF	X	X	19
RR(5)	IFT	X	X	MSB

PS01TR01 REGISTER DEFINITIONS

Bits	Description
A(0-4)	5-Bit RF PLL A-Counter
B(0-6)	7-Bit RF PLL B-Counter
RR(0-6)	7-Bit RF PLL Reference Counter
IN(0-5)	6-Bit IF PLL N-Counter
IR(0-3)	4-Bit IF PLL reference Counter
CR(0-7)	8-Bit Baseband Receive IQ Output DC Offset Cancellation Adjustment
CT(0-7)	8-Bit Baseband Transmit IQ Output DC Offset cancellation Adjustment
T(0-3)	4-Bit Transmit Filter Bandwidth Control. Range = 7 to 14MHz 3dB Bandwidth
R(0-3)	4-Bit Receive Filter Bandwidth Control. Range = 7 to 14MHz 3dB Bandwidth
DCR	Receive Output Common Mode DC Selection (0 = 1.2V or 1 = 1.7V)
DCT	Transmit Output Common Mode DC Selection (0 = 1.2V or 1 = 1.7V)

PS01TR01 POWER CONTROL INTERFACE SPECIFICATIONS

PLLs Programming	Description			
REF	Reference Crystal Frequency (0=22MHz or 1=44MHz)			
IFT	IF PLL - 0=Normal Operational Mode, 1=Test Mode			
M(0-1)	Operational Mode	M(0)	M(1)	Description
		0	0	Normal Operational State
		0	1	Reserved
		1	0	Reserved
		1	1	If Loop Back Mode - Both TX and RX in Active State
M(2)	(PLL_PE), PLL Power Enable. 1=Enable, 0=Power Down, SErial Port Always ON			

RF PLL PROGRAMMING

RFPLL Output Frequency:

The RFPLL output frequency is set by programming the RR and N_t Frequency Divider register, where

$$N_t = B \times P + A$$

P is the dual modulus prescaler and its value is 32.

The reference frequency, F_{ref}, on the REF_IN pin is divided by RR and the signal is applied to the input of the PLL's phase detector. After the PLL locks a frequency and a phase, the output frequency, f_{out}, is

$$f_{out} = \frac{f_{ref} \times N_t}{RR}$$

IF PLL Programming

The IFPLL output frequency, f_{out}, is

$$f_{out} = \frac{f_{ref} \times IN}{IR}$$

BASEBAND TRANSMIT AND RECEIVE LOW PASS FILTER PROGRAMMING

The 3dB bandwidth of the 3rd order Butterworth LPF can be programmed through the register bit T(0~3) and R(0~3). The bandwidth can be set from 7MHz to 14MHz.

R[3:0]	RX 3dB Bandwidth (MHz)	T[3:0]	TX 3dB Bandwidth (MHz)
0000	14.0	0000	14.0
1000	13.5	1000	13.5
0100	13.0	0100	13.0
1100	12.5	1100	12.5
0010	12.0	0010	12.0
0101	11.5	0101	11.5

R[3:0]	RX 3dB Bandwidth (MHz)	T[3:0]	TX 3dB Bandwidth (MHz)
0110	11.0	0110	11.0
0111	10.5	0111	10.5
1000	10.0	1000	10.0
1001	9.5	1001	9.5
1010	9.0	1010	9.0
1011	8.5	1011	8.5
1100	8.0	1100	8.0
1101	7.5	1101	7.5
1110	7.0	1110	7.0
1111	6.5	111	6.5

BASEBAND RECEIVE IQ DIFFERENTIAL OUTPUT OFFSET CORRECTION PROGRAMMING

CR[7:4]	CR[3:0]	RX Offset Compensation (mV)	CT[7:4]	CT[3:0]	TX Offset Compensation (mV)
1111	0000	-94	1111	0000	-94
1000	0000	-50	1000	0000	-50
0100	0000	-25	0100	0000	-25
0010	0000	-13	0010	0000	-13
0001	0000	-6	0001	0000	-6
0000	0000	0	0000	0000	0
0001	0001	0	0001	0001	0
1111	1111	0	1111	1111	0
0000	0001	+6	0000	0001	+6
0000	0010	+13	0000	0010	+13
0000	0100	+25	0000	0010	+25
0000	1000	+50	0000	1000	+50
0000	1111	+94	0000	1111	+94

RECEIVE IQ OUTPUT COMMON MODE SELECTION

the IFT bit allows the system designer to choose either 1.2V or 1.7V output common mode voltage. This feature enables our PS01TR01 radio to interface with various A/D converters used in common baseband chips.

IF LOOP BACK TEST MODE

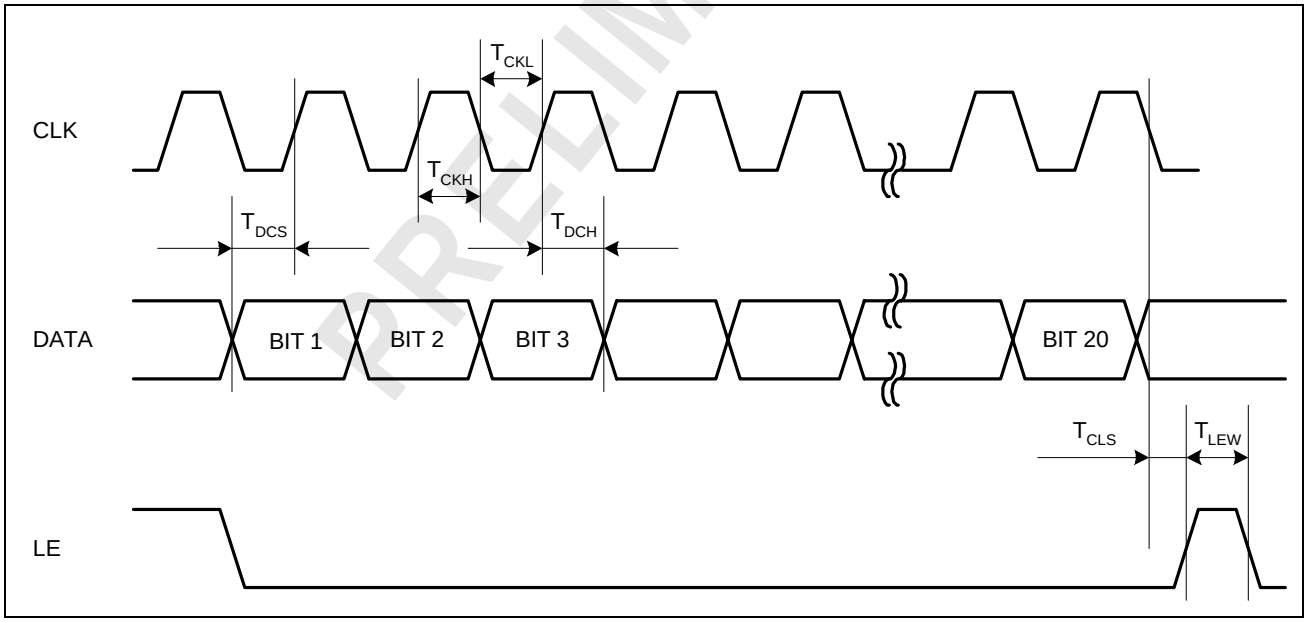
the M(0-1) bits allow the user to set the radio in a IF loop back test mode where both IF transmitter and IF receiver are enabled. This feature will be usefull for calibrating the IQ phase mimatch and DC offset generated by the radio.

POWER DOWN MODE

the M(2) register bit, when set to low, will power down all radio circuit except for the serial programming interface.

PS01TR01 PROGRAMMING INTERFACE SPECIFICATION

Function	Description	Specification		
		Min.	Max	Units
T_{DCS}	Data/CLK set up time	3	$< (T_{CLKH}+T_{CLKL})/2$	ns
T_{DCH}	Data/CLK hold time	3	$< (T_{CLKH}+T_{CLKL})/2$	ns
T_{CLKH}	Clock high time	6		ns
T_{CLKL}	Clock low time	6		ns
T_{CLS}	CLK/LE set up time	3	$< (T_{CLKH}+T_{CLKL})/2$	ns
T_{LEW}	LE Positive Width	6		ns



PSS'S RF TECHNOLOGY

PSS has developed an low cost high performance CMOS process enhancement to improve RF circuit performance. In particular, noise isolation and inductor Q are improved significantly.

Receiver LNA and Transmitter Power Amplifier Performance:

Specifications	LNA
RF frequency 1dB BW (MHz)	2400~2500
Input voltage (dBuVrms)	21~99
High Gain @ gain ctl = 1V (dB)	15
Tolerance (dB)	+/- 1(Tset<200ns)
Low Gain @ gain ctl = 2V (dB)	-15
Tolerance (dB)	+/- 2(Tset<200ns)
Gain variation (dB)	2
Isolation (dB)	20
Input Impedance (ohm)	50
Output impedance (ohm)	200
Output noise <22MHz BW> (dBuVrms)	24.4
P1dB output <high gain> (dBmVrms)	52
P1dB output <low gain> (dBmVrms)	52
OIP3 (dBmVrms)	62
Vdd (V)	2.7~3.3
Idd (mA)	10
Power supply rejection (dB)	20
RX EN response time (uS)	2
Temperature (deg. C)	-10~100

Specification	Power Amplifier	Pre-amplifier
RF frequency (MHz) 1dB BW	2400~2500	2400~2500
Output level (dBm)	1~21	33~53dBmVrms
High gain @ gain ctl = 1V (dB)	15	15
Tolerance (dB)	+/- 1	+/- 1
Isolation (dB)	20	20
Input impedance (ohm)	100	100
Output impedance (0hm)	50	100
Output noise <22MHz BW> (dBmVrms)	-18.6	-18.6
output 1dB compression (dBm)	22	10

Specification	Power Amplifier	Pre-amplifier
Vdd (V)	2.7~3.6	2.7~3.6
Idd (mA)	200	15
Power supply rejection (dB)	20	20
TX EN response time (us)	2	2
Temperature (deg C)	-10~100	-10~100

IF to BaseBand Interface Specification:

Receiver Baseband I & Q LPF	Min.	Typ.	Max.	Unit	Condition
IF frequency 3dB BW	7	10	14	MHz	Tunable
Phase mismatch		0	+/- 1	deg	+/- 1deg
Amplitude mismatch		0	+/- 1	dB	+/- 1dB
Filter type					3rd order Butterworth LPF
Output differential voltage			1.0	Vp	
Output differential voltage offset			10	mV	Auto-calibration mode
Passband flatness			0.1	dB	
3dB frequency accuracy			+/- 10	%	
Ultimate rejection		>80		dB	
Single-ended load			1MΩ, 10pF		
THD @ output			2	%	@500mVp, RL>5K & CL>15pF
Output noise (11MHz BW)			0.209	mVrms	Differential RMS voltage
Output common mode DC		1.2	1.7	V	
Input common mode DC		Vdd-0.5		V	
Vdd	2.7	3.0	3.6	V	
Idd			6	mA	
RX EN response time			2	uS	
Temperature	-10	25	100	^{o}C	

Transmitter Baseband I & Q LPF	Min.	Typ.	Max.	Unit	Condition
IF frequency 3dB BW	7	10	14	MHz	Tuable
Phase mismatch		0	+/- 1	deg	+/- 1 deg
Amplitude mismatch		0	+/- 1	dB	+/- 1 dB
Filter Type					3rd orer Butterworth LPF
Passband flatness			0.1	dB	
3dB frequency accurace			+/- 10	%	

Transmitter Baseband I & Q LPF	Min.	Typ.	Max.	Unit	Condition
Group delay flatness				ns	
Ultimate rejection		>80		dB	
Input impedance (single-ended)			1MΩ, 10pF		
Input differential voltage	50		100	mVp	
Input common mode DC	1.1	1.2	1.3	V	
Vdd	2.7	3.0	3.6	V	
Idd			3	mA	
TX EN response time			2	µs	
Temperature	-10	25	100	°C	

RECEIVER AGC CHARACTERISTICS:

The recommended LNA attenuation switch point is highly in bold.

Pin (dBm)	RFAGC (dB)	IFAGC (dB)	SNR (dB)	SIG/OIP3 (dB)	Output (mVp)
-82	15.0	60.0	10.7	-13.0	999
-80	15.0	58.0	12.7	-13.0	999
-75	15.0	53.0	17.7	-13.0	999
-70	15.0	48.0	22.7	-13.0	999
-65	15.0	43.0	27.7	-13.0	999
-60	15.0	38.0	32.7	-13.0	999
-55	15.0	33.0	37.7	-13.0	999
-50	15.0	28.0	42.7	-13.0	999
-45	15.0	23.0	47.7	-13.0	999
-40	**15.0**	**18.0**	**52.7**	**-13.0**	**999**
-35	15.0	13.0	57.5	-13.0	999
-30	15.0	8.0	62.0	-13.0	999
-25	15.0	2.7	65.7	-13.0	966
-20	15.0	-5.0	66.2	-12.4	708
-15	15.0	-10.0	66.9	-7.9	708
-55	-15.0	60.0	12.8	-16.0	707
-50	-15.0	58.0	17.8	-13.0	999
-45	**-15.0**	**53.0**	**22.8**	**-13.0**	**999**
-40	-15.0	48.0	27.8	-13.0	999
-35	-15.0	43.0	32.8	-13.0	999
-30	-15.0	38.0	37.8	-13.0	999
-25	-15.0	33.0	42.8	-13.0	999

Pin	RFAGC	IFAGC	SNR	SIG/OIP3	Output
(dBm)	(dB)	(dB)	(dB)	(dB)	(mVp)
-20	-15.0	28.0	47.8	-13.0	999
-15	-15.0	23.0	52.7	-13.0	999
-5	-15.0	13.0	62.1	-13.0	999
0	-15.0	8.0	65.9	-13.0	999
5	-15.0	2.8	68.2	-13.0	977
10	-15.0	-10.0	62.1	-12.9	398

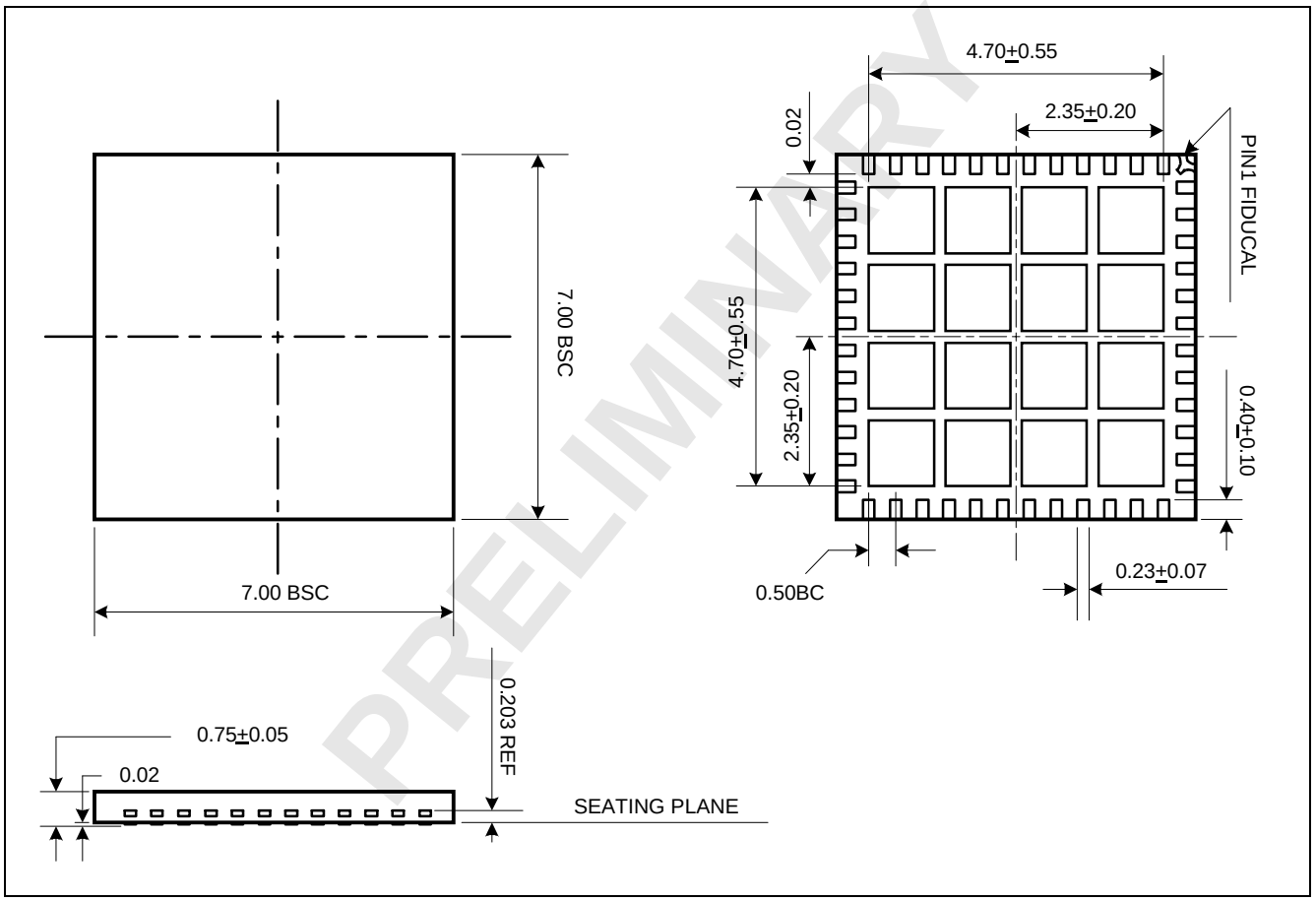


FIGURE: 48-PIN QFN

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