

**TC74HC283AP, TC74HC283AF, TC74HC283AFN**

(Note) The JEDEC SOP (FN) is not available in Japan.

**4 - BIT BINARY FULL ADDER**

The TC74HC283A is a high speed CMOS 4 - BIT BINARY FULL ADDER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Sum ( $\Sigma$ ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit.

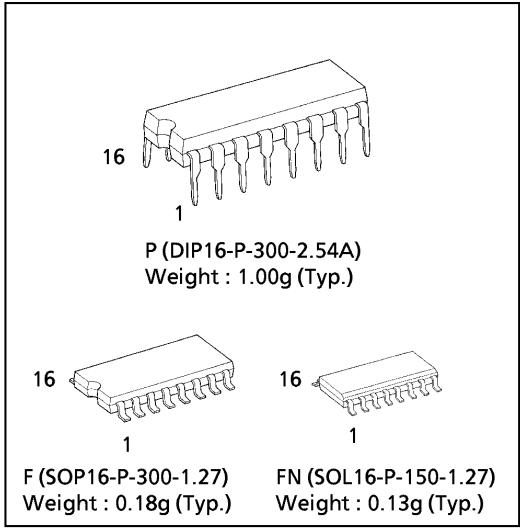
This adder features full internal look - ahead across all four bits.

A4  $\times$  n bit binary adder is easily built up by cascading the HC283A without any additional logic.

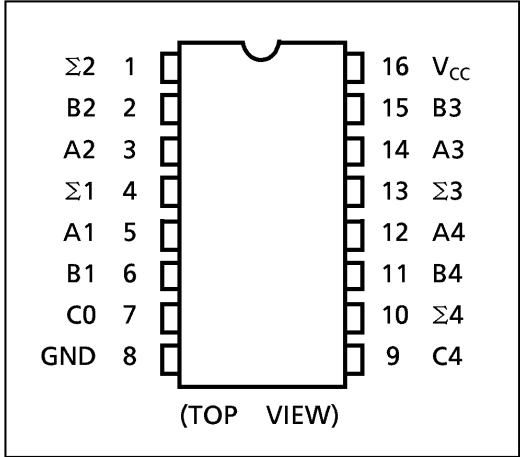
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES :**

- High Speed..... $t_{pd} = 17ns$ (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at  $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 4mA$ (Min.)
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC}$  (opr.) = 2V~6V
- Pin and Function Compatible with 74LS283



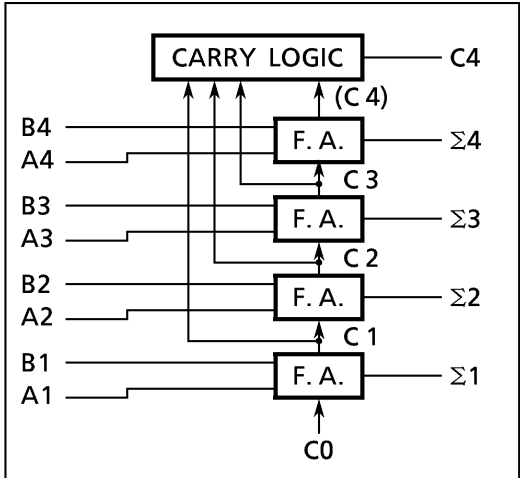
**PIN ASSIGNMENT**



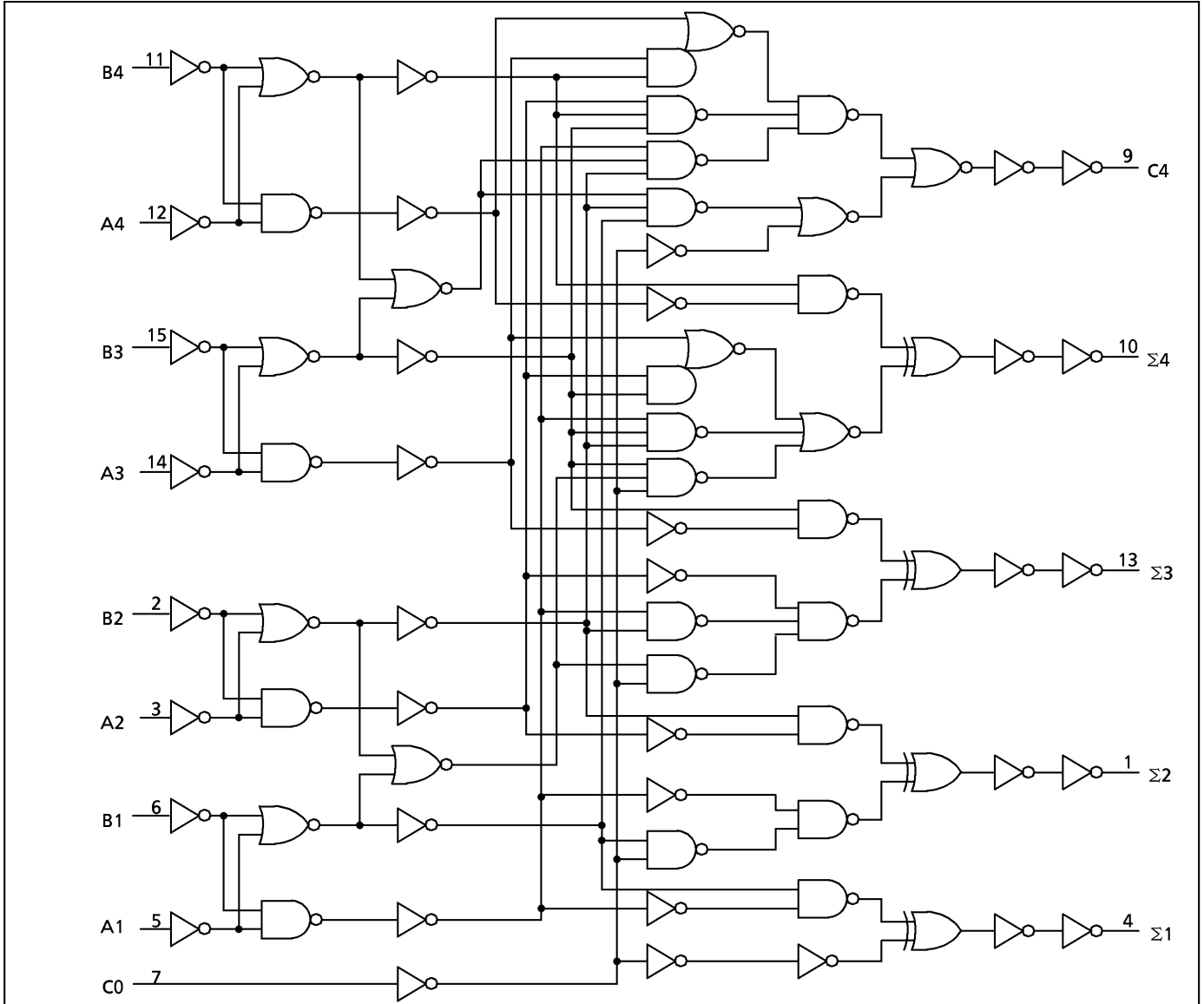
**TRUTH TABLE (1bit)**

INPUTS			OUTPUTS	
B <sub>n</sub>	A <sub>n</sub>	C <sub>n-1</sub>	$\Sigma_n$	C <sub>n</sub>
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

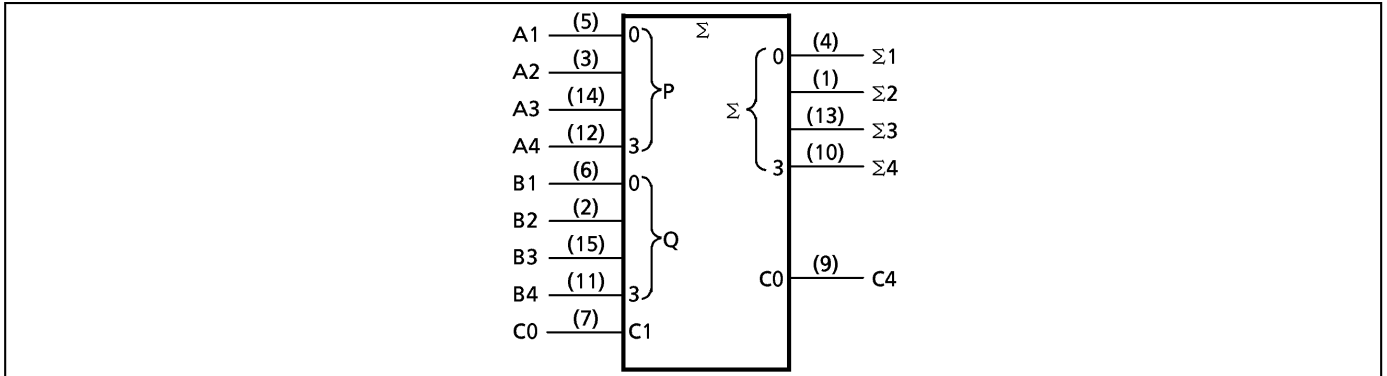
**BLOCK DIAGRAM**



**SYSTEM DIAGRAM**



**IEC LOGIC SYMBOL**



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	± 20	mA
Output Diode Current	$I_{OK}$	± 20	mA
DC Output Current	$I_{OUT}$	± 25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	± 50	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~ 1000 ( $V_{CC} = 2.0\text{V}$ ) 0~ 500 ( $V_{CC} = 4.5\text{V}$ ) 0~ 400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
		$I_{OH} = -4\text{ mA}$	4.5	4.18	4.31	—	4.13	—		
		$I_{OH} = -5.2\text{ mA}$	6.0	5.68	5.80	—	5.63	—		
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
		$I_{OL} = 4\text{ mA}$	4.5	—	0.17	0.26	—	0.33		
		$I_{OL} = 5.2\text{ mA}$	6.0	—	0.18	0.26	—	0.33		
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	± 0.1	—	± 1.0	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

**AC ELECTRICAL CHARACTERISTICS (  $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , Input  $t_r = t_f = 6\text{ns}$  )**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$ $t_{THL}$		—	4	8	ns
Propagation Delay Time ( $C0 - \Sigma n$ )	$t_{pLH}$ $t_{pHL}$		—	17	26	
Propagation Delay Time ( $C0 - C4$ )	$t_{pLH}$ $t_{pHL}$		—	17	26	
Propagation Delay Time ( $A_n, B_n - \Sigma n$ )	$t_{pLH}$ $t_{pHL}$		—	23	37	
Propagation Delay Time ( $A_n, B_n - C4$ )	$t_{pLH}$ $t_{pHL}$		—	21	34	

**AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$  )**

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(\text{V})$	$T_a = 25^\circ\text{C}$			$T_a = -40\text{--}85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time ( $C0 - \Sigma n$ )	$t_{pLH}$ $t_{pHL}$		2.0	—	60	150	—	190	
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	32	
Propagation Delay Time ( $C0 - C4$ )	$t_{pLH}$ $t_{pHL}$		2.0	—	60	150	—	190	
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	32	
Propagation Delay Time ( $A_n, B_n - \Sigma n$ )	$t_{pLH}$ $t_{pHL}$		2.0	—	95	210	—	265	
			4.5	—	27	42	—	53	
			6.0	—	22	36	—	45	
Propagation Delay Time ( $A_n, B_n - C4$ )	$t_{pLH}$ $t_{pHL}$		2.0	—	80	195	—	245	
			4.5	—	25	39	—	49	
			6.0	—	20	33	—	42	
Input Capacitance	$C_{IN}$			—	5	10	—	10	pF
Power Dissipation Capacitance	$C_{PD} (1)$			—	126	—	—	—	

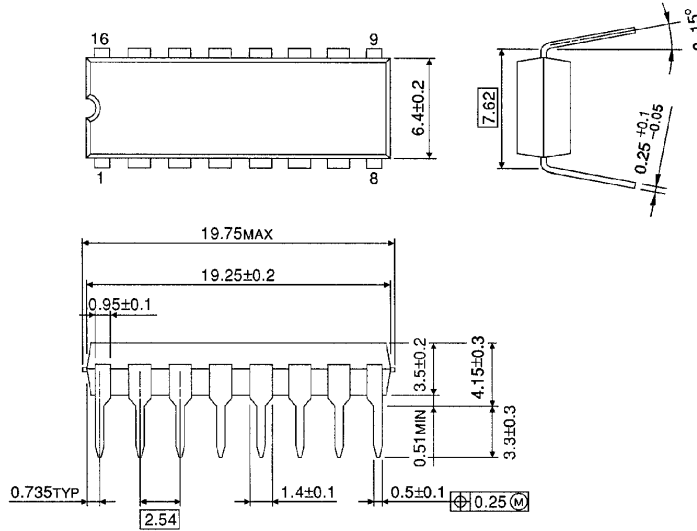
Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

**DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)**

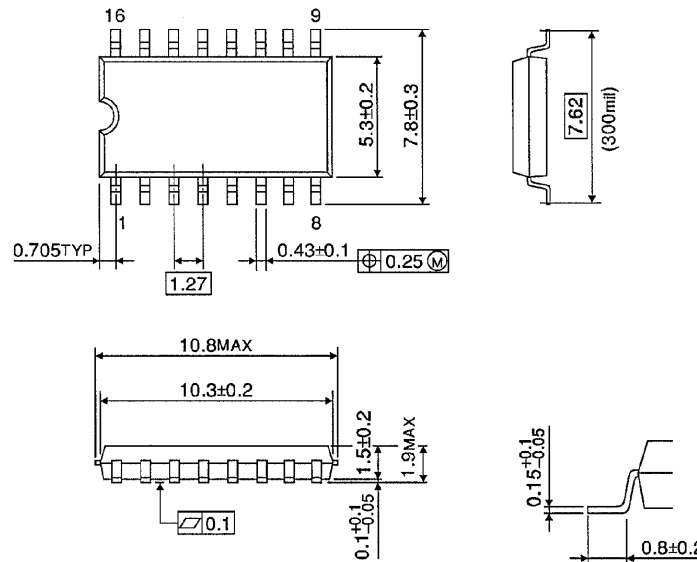
Unit in mm



Weight : 1.00g (Typ.)

**SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)**

Unit in mm

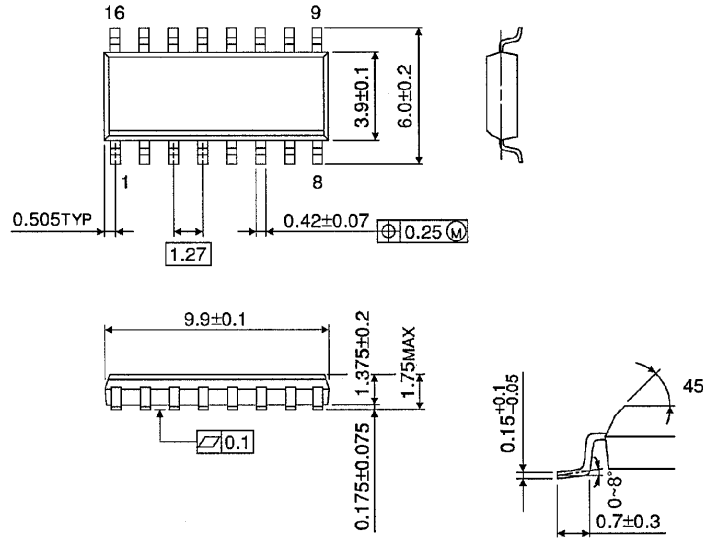


Weight : 0.18g (Typ.)

**SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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