

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

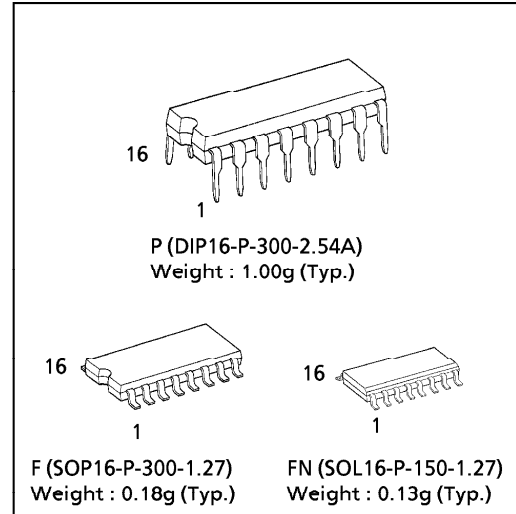
TC4021BP, TC4021BF, TC4021BFN

TC4021B 8-STAGE STATIC SHIFT REGISTER (ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT)

(Note) The JEDEC SOP (FN) is not available in Japan.

TC4021B is 8 stage parallel in/serial out shift register, which can be used also for serial in/serial out operations. In the case of parallel operation, the data of PARALLEL IN is input to each F/F asynchronously with CLOCK and the output is obtained. In the case of serial operations, each F/F is triggered by rising edge of CLOCK. (ASYNCHRONOUS PARALLEL OR SYNCHRONOUS SERIAL INPUT)

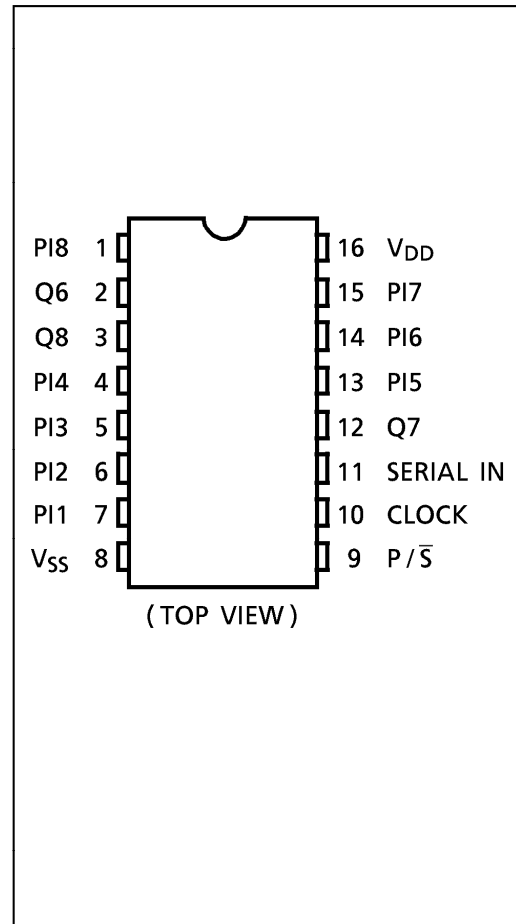
Switching of PARALLEL operation and SERIAL operation is achieved by P/ \bar{S} CONTROL input. When P/ \bar{S} CONTROL input is "H", PARALLEL operation is designated and when it is "L", SERIAL operation is designated.



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	-40~85	°C
Storage Temperature Range	T_{stg}	-65~150	°C

PIN ASSIGNMENT



TRUTH TABLE

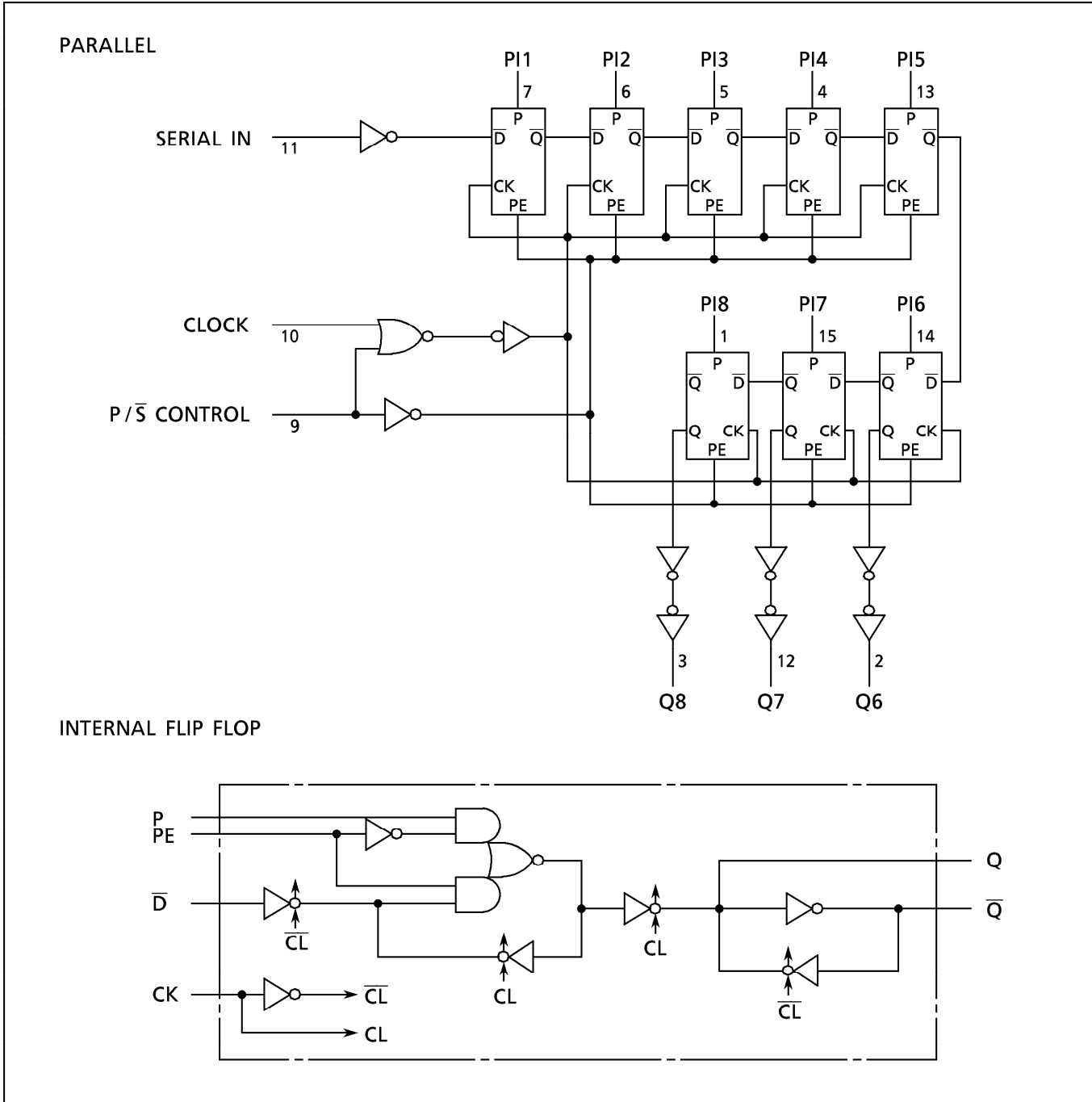
CLOCK $\Delta\Delta$	INPUTS				OUTPUTS Δ	
	P/ \bar{S}	PI1	PI _n	SI	Q1	Q _n
	L	※	※	L	L	Q _n - 1
	L	※	※	H	H	Q _n - 1
	L	※	※	※	No Change	
※	H	L	L	※	L	L
※	H	L	H	※	L	H
※	H	H	L	※	H	L
※	H	H	H	※	H	H

n : 2 ~ 8
 Δ : Q1 ~ Q5 Internal
 $\Delta\Delta$: Level Change
 ※ : Don't Care

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LOGIC DIAGRAM



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- The information contained herein is subject to change without notice.

RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	- 40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	I_{OH}	$V_{OH} = 4.6V$ $V_{OH} = 2.5V$ $V_{OH} = 9.5V$ $V_{OH} = 13.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
			5	-2.50	—	-2.10	-4.0	—	-1.70	—	
			10	-1.50	—	-1.30	-2.2	—	-1.10	—	
			15	-4.00	—	-3.40	-9.0	—	-2.80	—	
			15	-4.00	—	-3.40	-9.0	—	-2.80	—	
Output Low Current	I_{OL}	$V_{OL} = 0.4V$ $V_{OL} = 0.5V$ $V_{OL} = 1.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	0.61	—	0.51	1.5	—	0.42	—	mA
			10	1.50	—	1.30	3.8	—	1.10	—	
			15	4.00	—	3.40	15.0	—	2.80	—	
			15	4.00	—	3.40	15.0	—	2.80	—	
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5	3.5	—	3.5	2.75	—	3.5	—	V
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11.0	—	11.0	8.25	—	11.0	—	
			15	11.0	—	11.0	8.25	—	11.0	—	
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT} < 1\mu A$	5	—	1.5	—	2.25	1.5	—	1.5	V
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
Input Current	"H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	μA
	"L" Level	I_{IL}	$V_{IL} = 0V$	18	—	-0.1	—	-10^{-5}	-0.1	—	-1.0
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD} *$	5	—	5	—	0.005	5	—	150	μA
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.020	20	—	600	

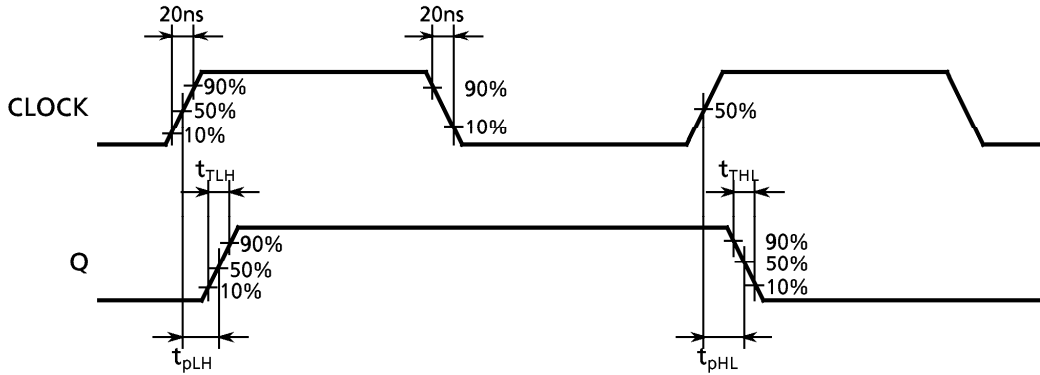
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

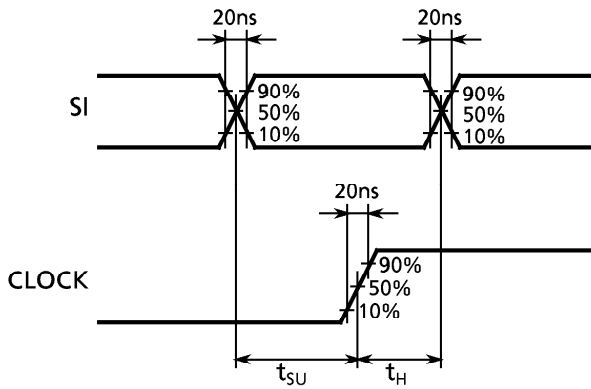
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t _{TLH}		5	—	80	200	ns
			10	—	50	100	
			15	—	40	80	
Output Transition Time (High to Low)	t _{THL}		5	—	80	200	ns
			10	—	50	100	
			15	—	40	80	
Propagation Delay Time (CLOCK - Q)	t _{pLH} t _{pHL}		5	—	150	320	ns
			10	—	65	160	
			15	—	45	120	
Propagation Delay Time (P/ \bar{S} - Q)	t _{pLH} t _{pHL}		5	—	230	460	ns
			10	—	90	180	
			15	—	60	120	
Max. Clock Frequency	f _{CL}		5	3.0	6.5	—	MHz
			10	6.0	18.0	—	
			15	8.5	24.0	—	
Min. Clock Pulse Width	t _w		5	—	80	180	ns
			10	—	30	80	
			15	—	20	50	
Max. Clock Rise Time Max. Clock Fall Time	t _{rCL} t _{fCL}		5	20.0	—	—	μ s
			10	2.5	—	—	
			15	1.0	—	—	
Min. Set-up Time (SI - CLOCK)	t _{SU}		5	—	40	120	ns
			10	—	20	80	
			15	—	15	60	
Min. Set-up Time (PI - P/ \bar{S})	t _{SU}		5	—	25	50	ns
			10	—	15	30	
			15	—	10	20	
Min. Hold Time (SI - CLOCK), (PI - P/ \bar{S})	t _H		5	—	35	70	ns
			10	—	20	40	
			15	—	15	30	
Min. Pulse Width (P/ \bar{S} - CONTROL)	t _{WH}		5	—	90	180	ns
			10	—	30	80	
			15	—	10	50	
Min. Removal Time (P/ \bar{S} - CLOCK)	t _{rem}		5	—	45	280	ns
			10	—	20	140	
			15	—	15	100	
Input Capacitance	C _{IN}			—	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

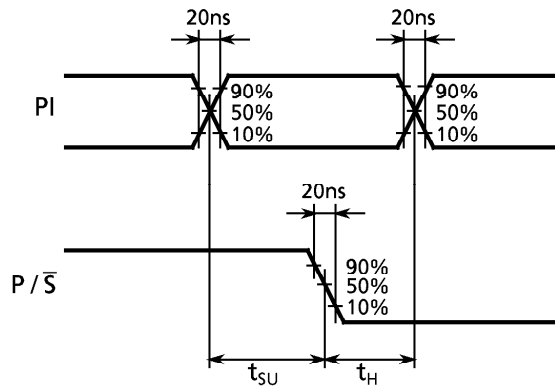
WAVEFORM 1



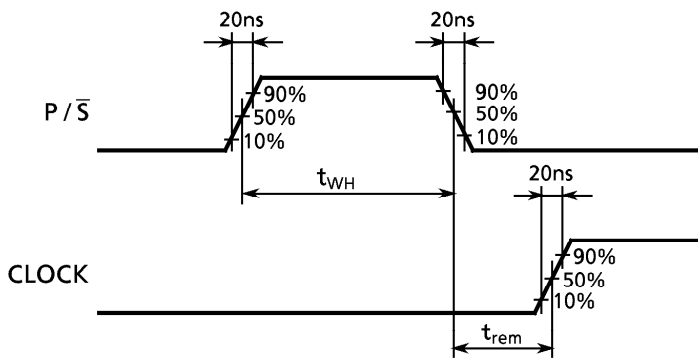
WAVEFORM 2



WAVEFORM 3



WAVEFORM 4



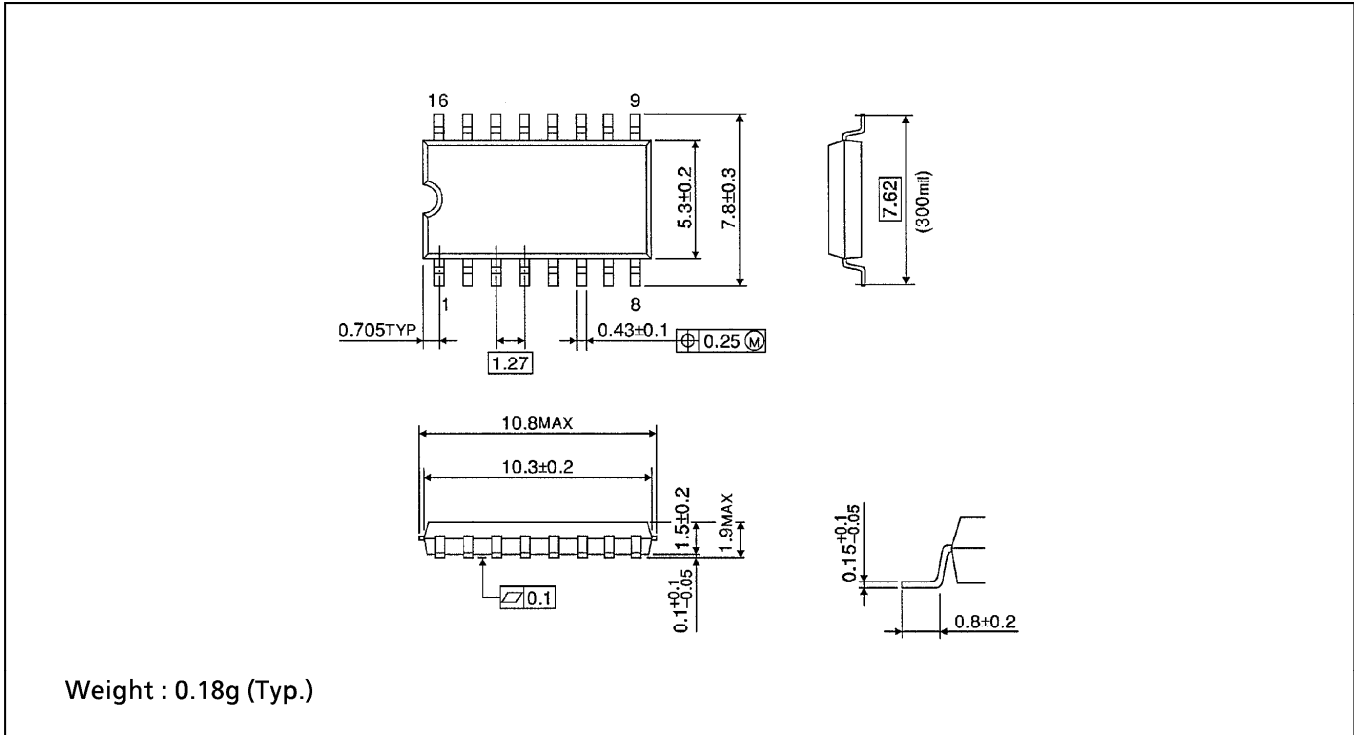
DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

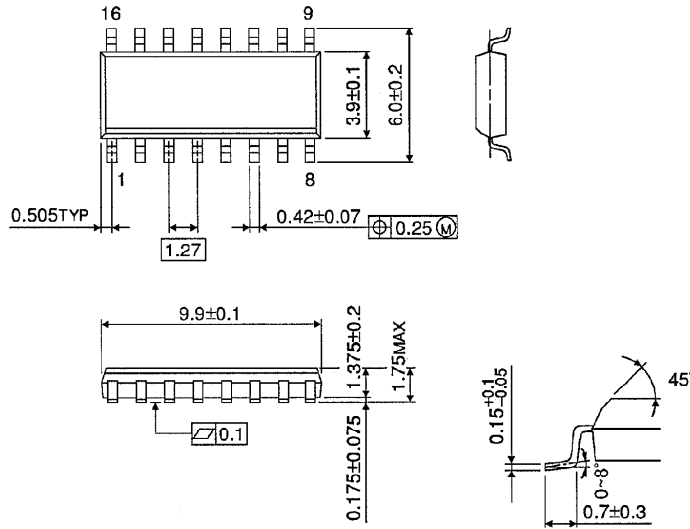
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)