- **Organization**
  - **TM2EP64DxN . . . 2097152 × 64 Bits**
  - **TM2EP72DxN . . . 2097152 × 72 Bits**
  - **TM4EP64DxN . . . 4194304 × 64 Bits**
  - **TM4EP72DxN . . . 4194304 × 72 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **TM2EP64DxN — Uses Eight 16M-Bit (2M×8-Bit) Dynamic Random Access Memories (DRAMs) in Thin Small-Outline Package (TSOP), or Small-Outline J-Lead Package (SOJ)**
- **TM2EP72DxN — Uses Nine 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ**
- **TM4EP64DxN — Uses 16 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ**
- **TM4EP72DxN — Uses 18 16M-Bit (2M×8-Bit) DRAMs in TSOP, or SOJ**
- **Performance ranges**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	EDO CYCLE t_{HPC} MIN
’xEPxxDxN-50	50 ns	13 ns	25 ns	20 ns
’xEPxxDxN-60	60 ns	15 ns	30 ns	25 ns
’xEPxxDxN-70	70 ns	18 ns	35 ns	30 ns

- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **High-Speed, Low-Noise LVTTL Interface**
- **Long Refresh Period: 32 ms (2 048 Cycles)**
- **3-State Output**
- **Extended-Data-Out (EDO) Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Serial Presence Detect (SPD) Using EEPROM**
- **Ambient Air Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**

description

The TM2EP64DPN is a 16M-byte, 168-pin, dual-in-line memory module (DIMM). The DIMM is composed of eight TMS427809A, 2097152 byte × 8-bit 2K-refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM2EP64DJN is available with an SOJ package (DZ suffix).

The TM2EP72DPN is a 16M-byte, 168-pin DIMM. The DIMM is composed of nine TMS427809A, 2097152 byte × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM2EP72DJN is available with an SOJ package (DZ suffix).

The TM4EP64DPN is a 32M-byte, 168-pin, dual-in-line memory module (DIMM). The DIMM is composed of sixteen TMS427809A, 2097152 × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. The TM4EP64DJN is available with an SOJ package (DZ suffix).

The TM4EP72DPN is a 32M-byte, 168-pin DIMM. The DIMM is composed of 18 TMS427809A, 2097152 × 8-bit 2K-refresh EDO DRAMs, mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS887). The TM4EP72DJN is available with an SOJ package (DZ suffix).

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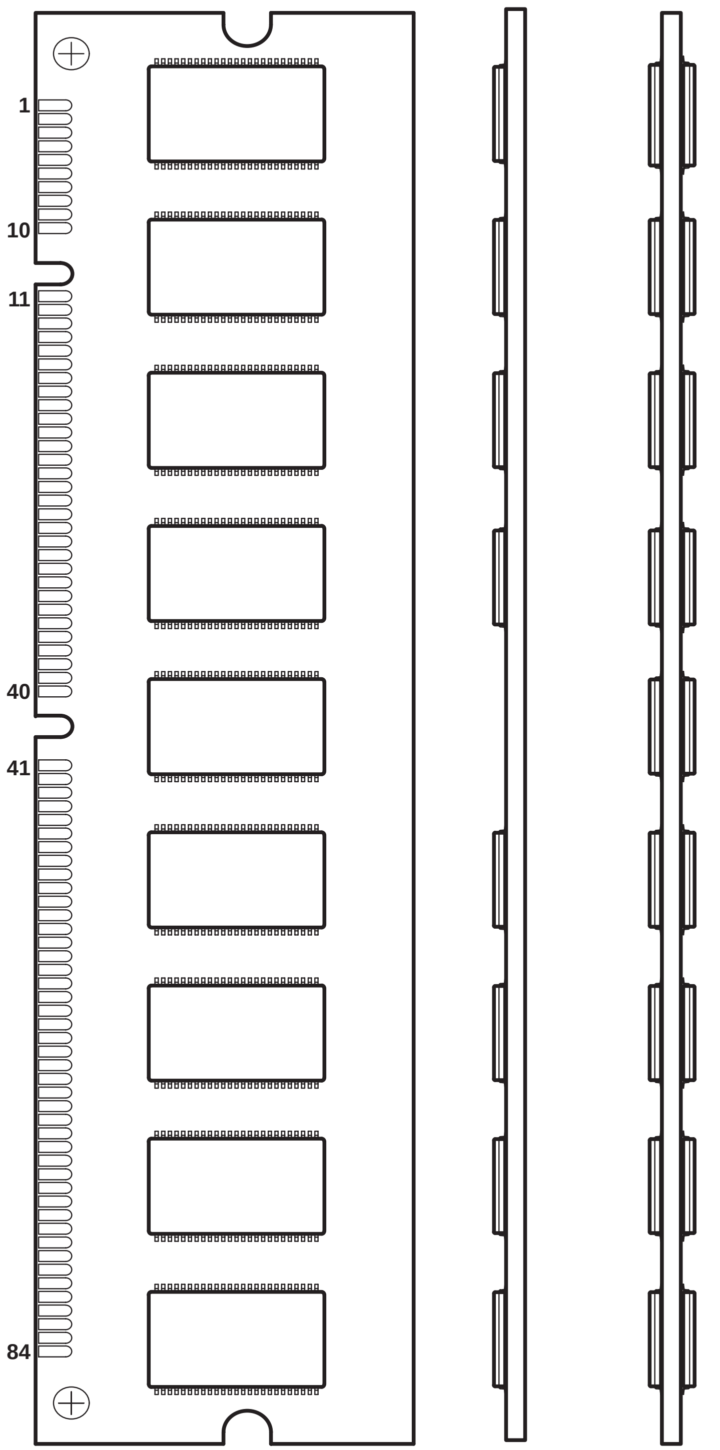
operation

The TMxEPxxDxN DIMMs operate as displayed in Table 1.

Table 1. TMxEPxxDxN DIMM Device Table

DIMM	DEVICE AND QUANTITY ( )	
TM2EP64DxN	TMS427809A (8)	Connected as shown in the functional block diagram.
TM2EP72DxN	TMS427809A (9)	
TM4EP64DxN	TMS427809A (16)	
TM4EP72DxN	TMS427809A (18)	

DUAL-IN-LINE MEMORY MODULE (TOP VIEW) **TM2EP64DPN (SIDE VIEW)** **TM4EP72DPN (SIDE VIEW)**



PIN NOMENCLATURE	
A[0:10]	Row Address Inputs
A[0:9]	Column Address Inputs
DQ[0:63]	Data In / Data Out
CB[0:7]	Check-Bit In / Check-Bit Out
$\overline{\text{CAS}}$[0:7]	Column-Address Strobe
$\overline{\text{RAS}}$[0:3]	Row-Address Strobe
$\overline{\text{WE0}}$ and $\overline{\text{WE2}}$	Write Enable
$\overline{\text{OE0}}$ and $\overline{\text{OE2}}$	Output Enable
SA[0:2]	Serial Presence Detect (SPD) Device Add Input
SDA	SPD Address / Data
SCL	SPD Clock
NC	No-Connect Pin
V_{DD}	3.3-V Supply
V_{SS}	Ground

Pin Assignments

PIN		PIN		PIN		PIN	
NO.	NAME	NO.	NAME	NO.	NAME	NO.	NAME
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	NC
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	$\overline{RAS3}$
4	DQ2	46	$\overline{CAS2}$	88	DQ34	130	$\overline{CAS6}$
5	DQ3	47	$\overline{CAS3}$	89	DQ35	131	$\overline{CAS7}$
6	V_{DD}	48	$\overline{WE2}$	90	V_{DD}	132	NC
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE0}$	69	DQ24	111	NC	153	DQ56
28	$\overline{CAS0}$	70	DQ25	112	$\overline{CAS4}$	154	DQ57
29	$\overline{CAS1}$	71	DQ26	113	$\overline{CAS5}$	155	DQ58
30	$\overline{RAS0}$	72	DQ27	114	$\overline{RAS1}$	156	DQ59
31	$\overline{OE0}$	73	V_{DD}	115	NC	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	NC	167	SA2
42	NC	84	V_{DD}	126	NC	168	V_{DD}

dual-in-line memory module and components

The dual-in-line memory module and components include:

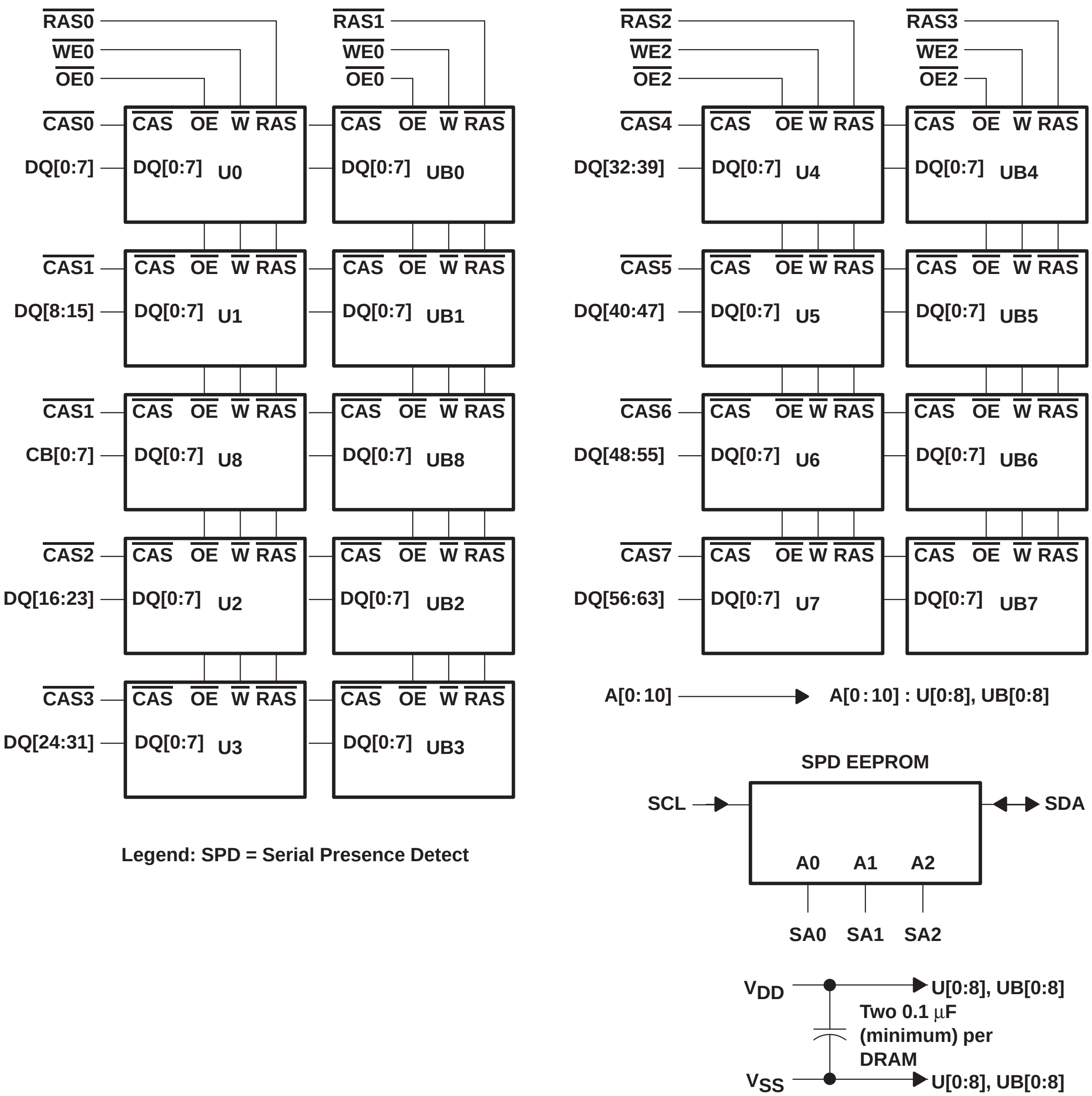
- PC substrate: 1,27 $\pm$ 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram

The following table shows the four DIMM modules and locations (Ux/UBx) that are used.

COMPONENT TABLE

MODULE	LOCATIONS USED
TM2EP64DxN	U[0:7]
TM2EP72DxN	U[0:8]
TM4EP64DxN	U[0:7], UB[0:7]
TM4EP72DxN	U[0:8], UB[0:8]



Legend: SPD = Serial Presence Detect

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} .... –0.5 V to 4.6 V
Voltage range on any pin (see Note 1) .... – 0.5 V to 4.6 V
Short-circuit output current .... 50 mA
Power dissipation: TM2EP64DxN .... 8 W
TM2EP72DxN .... 9 W
TM4EP64DxN .... 16 W
TM4EP72DxN .... 18 W
Ambient temperature range, T_A .... 0°C to 70°C
Storage temperature range, T_{stg} .... – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH-SPD}	High-level input voltage for the SPD device	2		5.5	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
T_A	Ambient temperature	0		70	°C

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		’2EP64DxN		’2EP72DxN		’4EP64DxN		’4EP72DxN		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0–A10		42		47		82		92	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$x		30		37		58		72	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$x		9		16		16		30	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$x		30		37		30		37	pF
$C_{i(W)}$	Input capacitance, $\overline{WE}$x		30		37		38		37	pF
C_o	Output capacitance		9		9		16		16	pF
$C_{i/o(SDA)}$	Input/output capacitance, SDA input		9		9		9		9	pF
$C_{i(SPD)}$	Input capacitance, SA0,SA1,SA2,SCL inputs		7		7		7		7	pF

NOTE 2: V_{DD} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TM2EP64DxN

PARAMETER		TEST CONDITIONS†		’2EP64DxN-50		’2EP64DxN-60		’2EP64DxN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD} – 0.2		V_{DD} – 0.2		V_{DD} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{\text{CASx}}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			960		800		720	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{\text{RASx}}$ and $\overline{\text{CASx}}$ high			16		16		16	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, $\overline{\text{RASx}}$ and $\overline{\text{CASx}}$ high			8		8		8	mA
I_{CC3}‡§	Average refresh current ($\overline{\text{RAS}}$-only refresh or CBR)	V_{DD} = 3.6 V, Minimum cycle, $\overline{\text{RASx}}$ cycling, $\overline{\text{CASx}}$ high ($\overline{\text{RAS}}$-only refresh), $\overline{\text{RASx}}$ low after $\overline{\text{CASx}}$ low (CBR)			960		800		720	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, $\overline{\text{RASx}}$ low, $\overline{\text{CASx}}$ cycling			880		720		640	mA

† For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{\text{RASx}}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM2EP72DxN

PARAMETER		TEST CONDITIONS†		’2EP72DxN-50		’2EP72DxN-60		’2EP72DxN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD} – 0.2		V_{DD} – 0.2		V_{DD} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{CASx}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			976		816		736	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			18		18		18	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RASx}$ and $\overline{CASx}$ high			9		9		9	mA
I_{CC3}‡§	Average refresh current ($\overline{RASx}$-only refresh or CBR)	V_{DD} = 3.6 V, Minimum cycle, $\overline{RASx}$ cycling, $\overline{CASx}$ high ($\overline{RAS}$-only refresh), $\overline{RASx}$ low after $\overline{CASx}$ low (CBR)			976		816		736	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, $\overline{RASx}$ low, $\overline{CASx}$ cycling			990		810		720	mA

† For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RASx}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM4EP64DxN

PARAMETER		TEST CONDITIONS†		’4EP64DxN-50		’4EP64DxN-60		’4EP64DxN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD} – 0.2		V_{DD} – 0.2		V_{DD} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, CASx high			± 20		± 20		± 20	µA
I_{CC1}‡§	Read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			976		816		736	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, RASx and CASx high			32		32		32	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, RASx and CASx high			16		16		16	mA
I_{CC3}‡§	Average refresh current (RASx-only refresh or CBR)	V_{DD} = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RASx low after CASx low (CBR)			976		816		736	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, RASx low, CASx cycling			896		736		656	mA

† For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while RASx = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)

TM4EP72DxN

PARAMETER		TEST CONDITIONS†		’4EP72DxN-50		’4EP72DxN-60		’4EP72DxN-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{DD} – 0.2		V_{DD} – 0.2		V_{DD} – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	V
I_I	Input current (leakage)	V_{DD} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{DD}			± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{DD} = 3.6 V, V_O = 0 V to V_{DD}, $\overline{\text{CASx}}$ high			± 20		± 20		± 20	µA
I_{CC1}‡§	Read- or write-cycle current	V_{DD} = 3.6 V, Minimum cycle			1098		918		828	mA
I_{CC2}	Standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{\text{RASx}}$ and $\overline{\text{CASx}}$ high			36		36		36	mA
		V_{IH} = V_{DD} – 0.2 V (LVCMOS), After one memory cycle, $\overline{\text{RASx}}$ and $\overline{\text{CASx}}$ high			18		18		18	mA
I_{CC3}‡§	Average refresh current ($\overline{\text{RASx}}$-only refresh or CBR)	V_{DD} = 3.6 V, Minimum cycle, $\overline{\text{RASx}}$ cycling, $\overline{\text{CASx}}$ high ($\overline{\text{RAS}}$-only refresh), $\overline{\text{RASx}}$ low after $\overline{\text{CASx}}$ low (CBR)			1098		918		828	mA
I_{CC4}‡¶	Average EDO current	V_{DD} = 3.6 V, t_{HPC} = MIN, $\overline{\text{RASx}}$ low, $\overline{\text{CASx}}$ cycling			1008		828		738	mA

† For conditions shown as MIN / MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{\text{RASx}}$ = V_{IL}
¶ Measured with a maximum of one address change during each EDO cycle, t_{HPC}

switching characteristics over recommended ranges of supply voltage and ambient temperature (see Note 3)

PARAMETER		’xEP64DxN-50 ’xEP72DxN-50		’xEP64DxN-60 ’xEP72DxN-60		’xEP64DxN-70 ’xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 4)		25		30		35	ns
t_{CAC}	Access time from $\overline{CAS}$x (see Note 4)		13		15		18	ns
t_{CPA}	Access time from $\overline{CAS}$x precharge (see Note 4)		28		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$x (see Note 4)		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$x (see Note 4)		13		15		18	ns
t_{CLZ}	Delay time, $\overline{CAS}$x to output in low impedance	0		0		0		ns
t_{REZ}	Output buffer turn off delay from $\overline{RAS}$x (see Note 5)	3	13	3	15	3	18	ns
t_{CEZ}	Output buffer turn off delay from $\overline{CAS}$x (see Note 5)	3	13	3	15	3	18	ns
t_{OEZ}	Output buffer turn off delay from $\overline{OE}$x (see Note 5)	3	13	3	15	3	18	ns
t_{WEZ}	Output buffer turn off delay from $\overline{WE}$x (see Note 5)	3	13	3	15	3	18	ns

NOTES: 3. With ac parameters, it is assumed that t_T = 2 ns.
4. Access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
5. The maximum values of t_{REZ}, t_{CEZ}, t_{OEZ}, and t_{WEZ} are specified when the outputs are no longer driven. Data-in should not be driven until one of the applicable maximum values is satisfied.

EDO timing requirements (see Note 3)

		’xEP64DxN-50 ’xEP72DxN-50		’xEP64DxN-60 ’xEP72DxN-60		’xEP64DxN-70 ’xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode, read-write	20		25		30		ns
t_{PRWC}	Cycle time, EDO read-write	57		68		78		ns
t_{CSH}	Delay time, $\overline{RAS}$x active to $\overline{CAS}$x precharge	40		48		58		ns
t_{CHO}	Hold time, $\overline{OE}$x from $\overline{CAS}$x	7		10		10		ns
t_{DOH}	Hold time, output from $\overline{CAS}$x	5		5		5		ns
t_{OEP}	Precharge time, $\overline{OE}$x	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{CAS}$x active	8	10 000	10	10 000	12	10 000	ns
t_{WPE}	Pulse duration, $\overline{WE}$x active (output disable only)	7		7		7		ns
t_{CP}	Pulse duration, $\overline{CAS}$x precharge	8		10		10		ns
t_{OCH}	Setup time, $\overline{OE}$x before $\overline{CAS}$x	8		10		10		ns
t_{OEP}	Precharge time, $\overline{OE}$x	5		5		5		ns

NOTE 3: With ac parameters, it is assumed that t_T = 2 ns.

ac timing requirements

		'xEP64DxN-50 'xEP72DxN-50		'xEP64DxN-60 'xEP72DxN-60		'xEP64DxN-70 'xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write	84		104		124		ns
t_{RWC}	Cycle time, read-write	111		135		160		ns
t_{RASP}	Pulse duration, $\overline{\text{RASx}}$ active, fast page mode (see Note 6)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{\text{RASx}}$ active, non-page mode (see Note 6)	50	10 000	60	10 000	70	10 000	ns
t_{RP}	Pulse duration, $\overline{\text{RASx}}$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	8		10		10		ns
t_{RASS}	Pulse duration, $\overline{\text{RASx}}$ active, self refresh (see Note 7)	100		100		100		µs
t_{RPS}	Pulse duration, $\overline{\text{RASx}}$ precharge after self refresh	90		110		130		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 8)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{\text{CASx}}$ precharge	8		10		12		ns
t_{RWL}	Setup time, write command before $\overline{\text{RASx}}$ precharge	8		10		12		ns
t_{WCS}	Setup time, write command before $\overline{\text{CASx}}$ active (early-write only)	0		0		0		ns
t_{WRP}	Setup time, $\overline{\text{WEx}}$ high before $\overline{\text{RASx}}$ low (CBR refresh only)	10		10		10		ns
t_{CSR}	Setup time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	8		10		12		ns
t_{DH}	Hold time, data in (see Note 8)	8		10		12		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{\text{CASx}}$ (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{\text{RASx}}$ (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{\text{CASx}}$ active (early-write only)	8		10		12		ns
t_{ROH}	Hold time, $\overline{\text{RASx}}$ referenced to $\overline{\text{OEx}}$	8		10		10		ns
t_{WRH}	Hold time, $\overline{\text{WEx}}$ high after $\overline{\text{RASx}}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (CBR refresh only)	10		10		10		ns
t_{OEH}	Hold time, $\overline{\text{OEx}}$ command	13		15		18		ns
t_{RHCP}	Hold time, $\overline{\text{RASx}}$ active from $\overline{\text{CASx}}$ precharge	28		35		40		ns
t_{CHS}	Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RASx}}$ (self refresh only)	– 50		– 50		– 50		ns
t_{AWD}	Delay time, column address to write command (read-write only)	42		49		57		ns
t_{CRP}	Delay time, $\overline{\text{CASx}}$ precharge to $\overline{\text{RASx}}$	5		5		5		ns

NOTES: 6. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
7. During the period of 10 µs $\leq t_{RASS} \leq$ 100 µs, the device is in a transition state from normal-operation mode to self-refresh mode.
8. Referenced to the later of $\overline{\text{CASx}}$ or $\overline{\text{WEx}}$ in write operations
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

ac timing requirements (continued)

		’xEP64DxN-50 ’xEP72DxN-50		’xEP64DxN-60 ’xEP72DxN-60		’xEP64DxN-70 ’xEP72DxN-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CWD}	Delay time, $\overline{CAS}$x to write command (read-write only)	30		34		40		ns
t_{OED}	Delay time, $\overline{OE}$x to data in	13		15		18		ns
t_{RAD}	Delay time, $\overline{RAS}$x to column address (see Note 10)	10	25	12	30	12	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$x precharge	25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$x precharge	18		20		25		ns
t_{RCD}	Delay time, $\overline{RAS}$x to $\overline{CAS}$x (see Note 10)	12	37	14	45	14	52	ns
t_{RPC}	Delay time, $\overline{RAS}$x precharge to $\overline{CAS}$x	5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$x active to $\overline{RAS}$x precharge	8		10		12		ns
t_{RWD}	Delay time, $\overline{RAS}$x to write command (read-write only)	67		79		92		ns
t_{CPW}	Delay time, $\overline{CAS}$x precharge to write command (read-write only)	45		54		62		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	2	30	2	30	2	30	ns

NOTE 10: The maximum value is specified only to ensure access time.

serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, DRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments module comply with the current JEDEC SPD Standard. Please see the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 2 – TM2EP64DxN　　Table 3 – TM2EP72DxN
Table 4 – TM4EP64DxN　　Table 5 – TM4EP72DxN

Table 2. Serial Presence Detect Data for the TM2EP64DxN

BYTE NO.	FUNCTION DESCRIBED	’2EP64DxN-50		’2EP64DxN-60		’2EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	DIMM configuration type (non-parity, parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh rate / type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N / A	00h	N / A	00h	N / A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 – 62	41	29h	53	35h	66	42h
64–71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h

serial presence detect (continued)

Table 2. Serial Presence Detect Data for the TM2EP64DxN (Continued)

BYTE NO.	FUNCTION DESCRIBED	’2EP64DxN-50		’2EP64DxN-60		’2EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator’s specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 3. Serial Presence Detect Data for the TM2EP72DxN

BYTE NO.	FUNCTION DESCRIBED	’2EP72DxN-50		’2EP72DxN-60		’2EP72DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h	1 bank	01h
6	Data width of this assembly	72 bits	48h	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	DIMM configuration type (non-parity, parity, ECC)	ECC	02h	ECC	02h	ECC	02h
12	Refresh rate / type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h	x8	08h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 – 62	59	3Bh	71	47h	84	54h
64–71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator’s specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 4. Serial Presence Detect Data for the TM4EP64DxN

BYTE NO.	FUNCTION DESCRIBED	’4EP64DxN-50		’4EP64DxN-60		’4EP64DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	DIMM configuration type (non-parity, parity, ECC)	Non-Parity	00h	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h	N/A	00h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0–62	42	2Ah	54	36h	67	43h
64–71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator’s specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

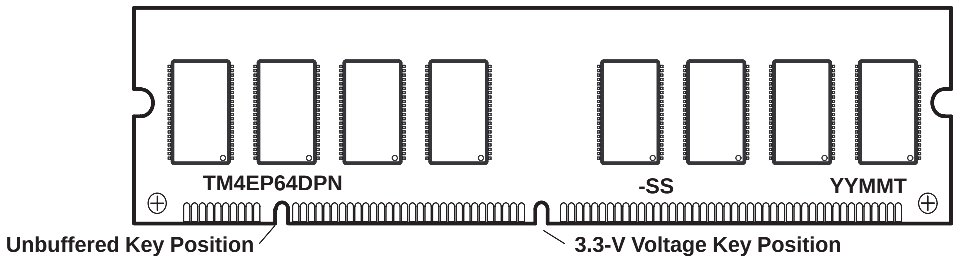
serial presence detect (continued)

Table 5. Serial Presence Detect for the TM4EP72DxN

BYTE NO.	FUNCTION DESCRIBED	’4EP72DxN-50		’4EP72DxN-60		’4EP72DxN-70	
		ITEM	DATA	ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM)	EDO	02h	EDO	02h	EDO	02h
3	Number of row addresses on this assembly	11	0Bh	11	0Bh	11	0Bh
4	Number of column addresses on this assembly	10	0Ah	10	0Ah	10	0Ah
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h	2 banks	02h
6	Data width of this assembly	72 bits	48h	72 bits	48h	72 bits	48h
7	Data width continuation		00h		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h	LVTTL	01h
9	$\overline{\text{RAS}}$x access time of module	t_{RAC} = 50 ns	32h	t_{RAC} = 60 ns	3Ch	t_{RAC} = 70 ns	46h
10	$\overline{\text{CAS}}$x access time of module	t_{CAC} = 13 ns	0Dh	t_{CAC} = 15 ns	0Fh	t_{CAC} = 18 ns	12h
11	DIMM configuration type (non-parity, parity, ECC)	ECC	02h	ECC	02h	ECC	02h
12	Refresh rate / type	15.6 µs	00h	15.6 µs	00h	15.6 µs	00h
13	DRAM width, primary DRAM	x8	08h	x8	08h	x8	08h
14	Error-checking SDRAM data width	x8	08h	x8	08h	x8	08h
62	SPD revision	Rev. 1	01h	Rev. 1	01h	Rev. 1	01h
63	Checksum for bytes 0 – 62	60	3Ch	72	48h	85	55h
64–71	Manufacturer’s JEDEC ID code per JEP-106E	97h	9700...00h	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD		TBD	
73–90	Manufacturer’s part number†	TBD		TBD		TBD	
91	Die revision code†	TBD		TBD		TBD	
92	PCB revision code†	TBD		TBD		TBD	
93–94	Manufacturing date†	TBD		TBD		TBD	
95–98	Assembly serial number†	TBD		TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD		TBD	
126–127	Vendor specific data†	TBD		TBD		TBD	
128–166	System integrator’s specific data‡	TBD		TBD		TBD	
167–255	Open						

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

device symbolization (TM4EP64DPN illustrated)

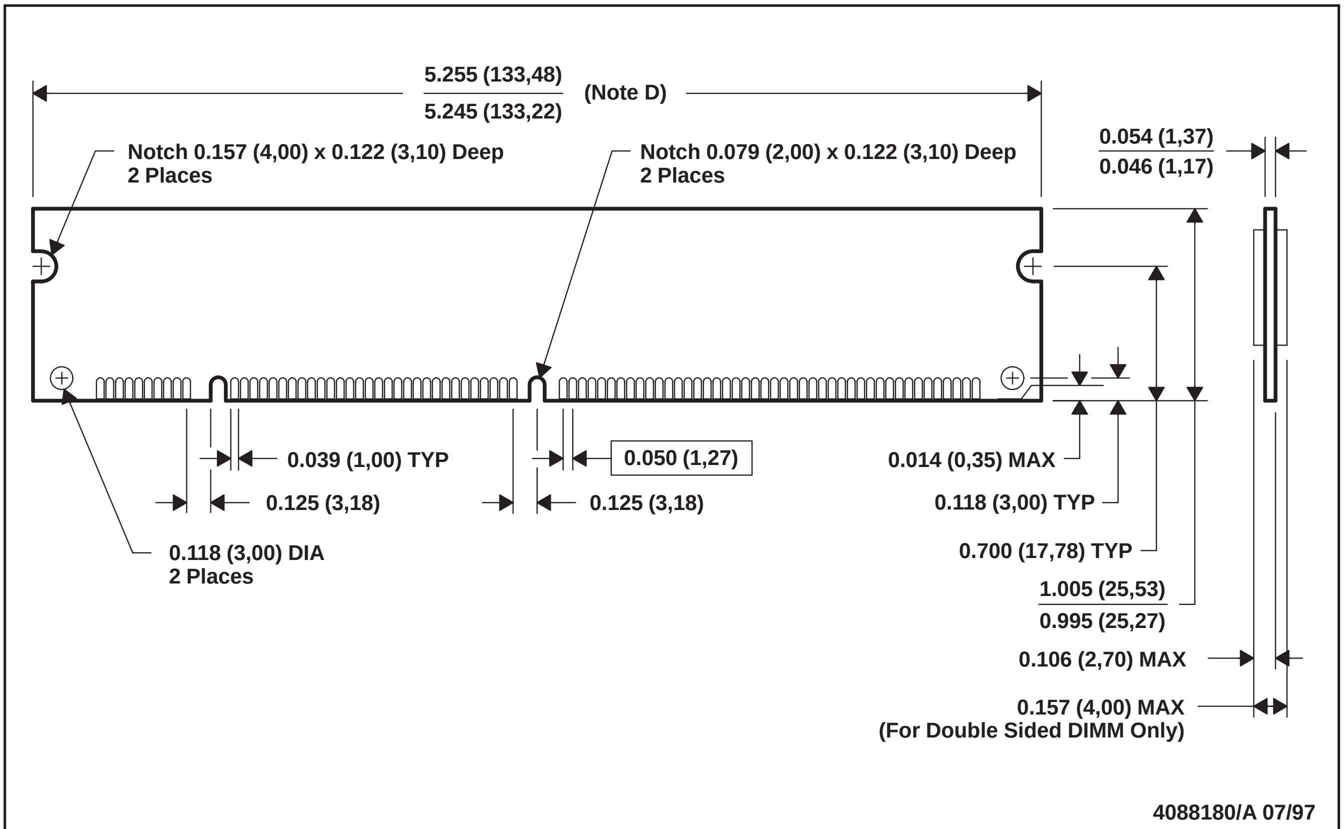


YY	=	Year Code
MM	=	Month Code
T	=	Assembly Site Code
-SS	=	Speed Code

NOTE A: Location of symbolization may vary.

MECHANICAL DATA

BR (R-PDIM-N168) **DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-161
D. Dimension includes de-panelization variations; applies between notch and tab edge.
E. Outline may vary above notches to allow router/panelization irregularities.

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