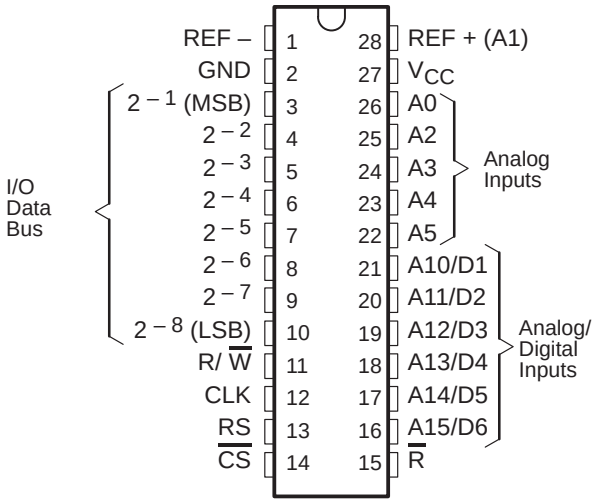
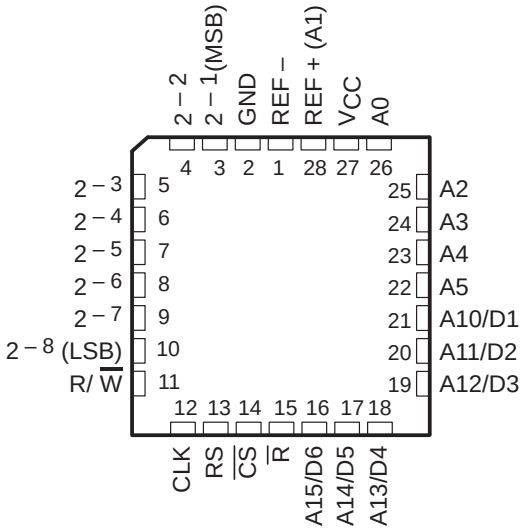
- **LinCMOS™ Technology**
- **8-Bit Resolution**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Ratiometric Conversion**
- **Access Plus Conversion Time:**
  **TLC532A . . . 15 μs Max**
  **TLC533A . . . 30 μs Max**
- **3-State, Bidirectional I/O Data Bus**
- **5 Analog and 6 Dual-Purpose Inputs**
- **On-Chip 12-Channel Analog Multiplexer**
- **Three On-Chip 16-Bit Data Registers**
- **Software Compatible With Larger TL530 and TL531 (21-Input Versions)**
- **On-Chip Sample-and-Hold Circuit**
- **Single 5-V Supply Operation**
- **Low Power Consumption . . . 6.5 mW Typ**
- **Improved Direct Replacements for Texas Instruments TL532 and TL533, National Semiconductor ADC0829, and Motorola MC14442**

**N PACKAGE**
**(TOP VIEW)**




**FN PACKAGE**
**(TOP VIEW)**




## description

The TLC532A and TLC533A are monolithic LinCMOS™ peripheral integrated circuits each designed to interface a microprocessor for analog data acquisition. These devices are complete peripheral data acquisition systems on a single chip and can convert analog signals to digital data from up to 11 external analog terminals. Each device operates from a single 5-V supply and contains a 12-channel analog multiplexer, and 8-bit ratiometric analog-to-digital (A/D) converter, a sample-and-hold circuit, three 16-bit registers, and microprocessor-compatible control circuitry. Additional features include a built-in self-test, sixmultipurpose (analog or digital) inputs, five external analog inputs, and an 8-pin input/output (I/O) data port. The three on-chip data registers store the control data, the conversion results, and the input digital data that can be accessed via the microprocessor data bus in two bytes

**FUNCTION TABLE**

| ADDRESS/CONTROL | | | | | DISCRIPTION |
|---|---|---|---|---|---|
| R/$\overline{W}$ | RS | $\overline{CS}$ | $\overline{R}$ | CLK | |
| X | X | X | L† | | Reset |
| L | H | L | H | ↓ | Write bus data to control register |
| H | L | L | H | ↑ | Read data from analog conversion register |
| H | H | L | H | ↑ | Read data from digital register |
| X | X | H | H | X | No response |

H=High-level, L = Low-level, X = Irrelevant
↓=High-to-low transition, ↑ = Low-to-high transition

† For proper operation, RESET must be low for at least three lock cycles.

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## description (continued)

(most-significant byte first). In this manner, a microprocessor can access up to 11 external analog inputs or 6 digital signals and the positive reference voltage that may be used for self-test. The A/D conversion uses the successive-approximation technique and switched-capacitor circuitry. This method eliminates the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Any one of 11 analog inputs (or self-test) can be converted to an 8-bit digital word and stored within 10 μs for the TLC532A or 20 μs for theTLC533A after instructions from the microprocessor are recognized. The on-chip sample-and-hold circuit automatically minimizes errors due to noise on the analog inputs. Furthermore, differential high-impedance reference inputs are available to help isolate the analog circuitry from the logic and supply noises while easing ratiometric conversion and scaling.

The TLC532AI and TLC533AI are characterized for operation from – 40°C to 85°C. The TLC532AM and TLC533AM are available in both the N and FN plastic packages and are characterized for operation from – 55°C to 125°C.

## functional description

The TLC532A and TLC533A provide direct interface to a microprocessor-based system. Control of the TLC532A and TLC533A is handled via the 8-line TTL-compatible 3-state data bus, the three control inputs (R/$\overline{W}$, RS, and $\overline{CS}$), and the CLK input. Each device contains three 16-bit internal registers — the control register, the analog conversion data register, and the digital data register.

A high level at the R/$\overline{W}$ input and a low level at the $\overline{CS}$ input set the device to output data on the 8-line data bus for the processor to read. A low level at the R/$\overline{W}$ input and a low level at the $\overline{CS}$ input set the device to receive instructions into the internal control register on the 8-line data bus from the processor. When the device is in the read mode and the RS input is low, the processor reads the data contained in the analog conversion data register. However, when the RS input is high, the processor reads the data contained in the digital-data register.

The control register is a write-only register into which the microprocessor writes command instructions for the device to start A/D conversion and to select the analog channel to be converted. The analog conversion data register is a read-only register that contains the current converter status and most recent conversion results. The digital data register is also a read-only register that holds the digital input logic levels from the six dual-purpose inputs.

Internally each device contains a byte pointer that selects the appropriate byte during two cycles of the CLK input in a normal 16-bit microprocessor instruction. The internal pointer automatically points to the most significant (MS) byte after the first complete clock cycle any time that the $\overline{CS}$ is at the high level for at least one clock cycle. The device treats the next signal on the 8-line data bus as the MS byte. A low level at the $\overline{CS}$ input activates the inputs and outputs and an internal function decoder. However, no data is transferred until the CLK goes high. The internal byte pointer first points to the MS byte of the selected register during the first clock cycle. After the first clock cycle in which the MS byte is accessed, the internal pointer switches to the LS byte and remains there for as long as $\overline{CS}$ is low. The MS byte of any register may be accessed by either an 8-bit or a 16-bit microprocessor instruction; however, the LS byte may only be accessed by a 16-bit microprocessor instruction.

Normally, a 2-byte word is written or read from the controlling processor, but a single byte can be read by the processor by manipulating the $\overline{CS}$ input. This can be used to read conversion status from the analog conversion data register or the digital multipurpose input levels from the digital data register. The format and content of each 2-byte word is shown in Figures 1 through 3.

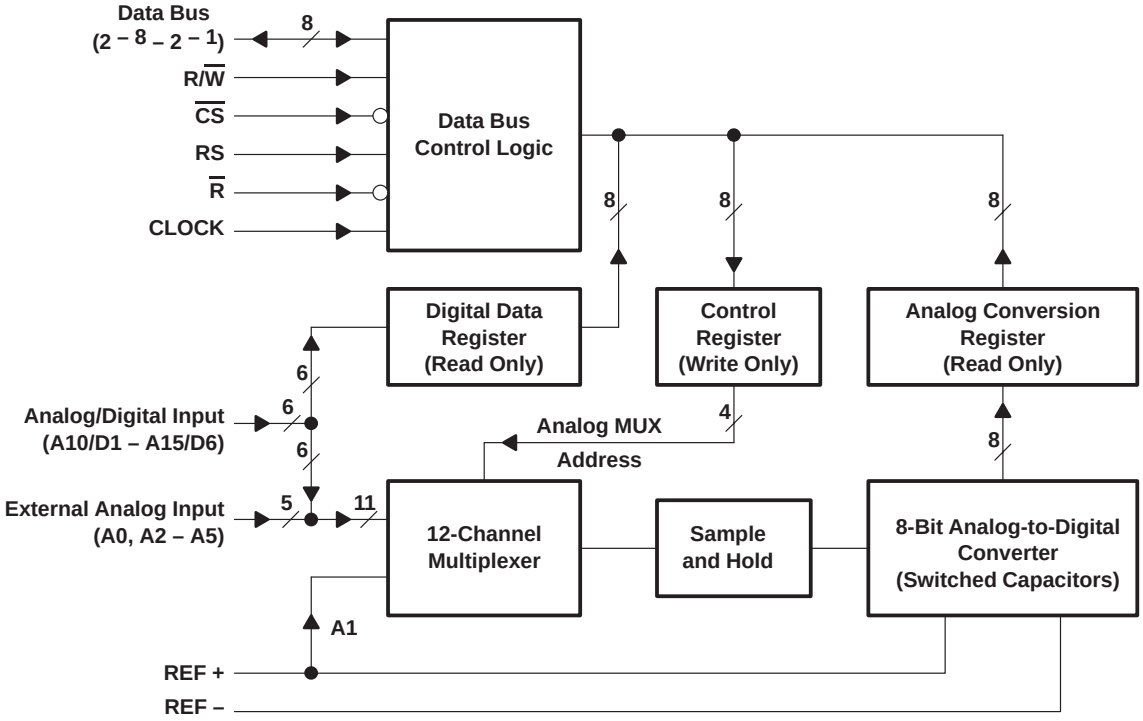
## functional description (continued)

A conversion cycle starts after a 2-byte instruction is written to the control register and the start conversion (SC) bit is a logic high. This 2-byte instruction also selects the input analog channel to be converted. The status (EOC) bit in the analog conversion data register is reset, and it remains reset until the conversion is complete, at which time the status bit is set again. After conversion, the results are loaded into the analog conversion data register. These results remain in the analog conversion data register until the next conversion cycle is complete. If a new conversion command is entered into the control register while the conversion cycle is in progress, the on-going conversion is aborted and a new channel acquisition cycle begins immediately.

The reset input $\overline{R}$ allows the device to be externally forced to a known state. When a low level is applied to the $\overline{R}$ input for a minimum of three clock periods, the SC bit is cleared. The A/D converter is then idled and all the outputs are placed in the high-impedance off-state. However, the content of the analog conversion data register is not affected by the $\overline{R}$ input going to a low level.

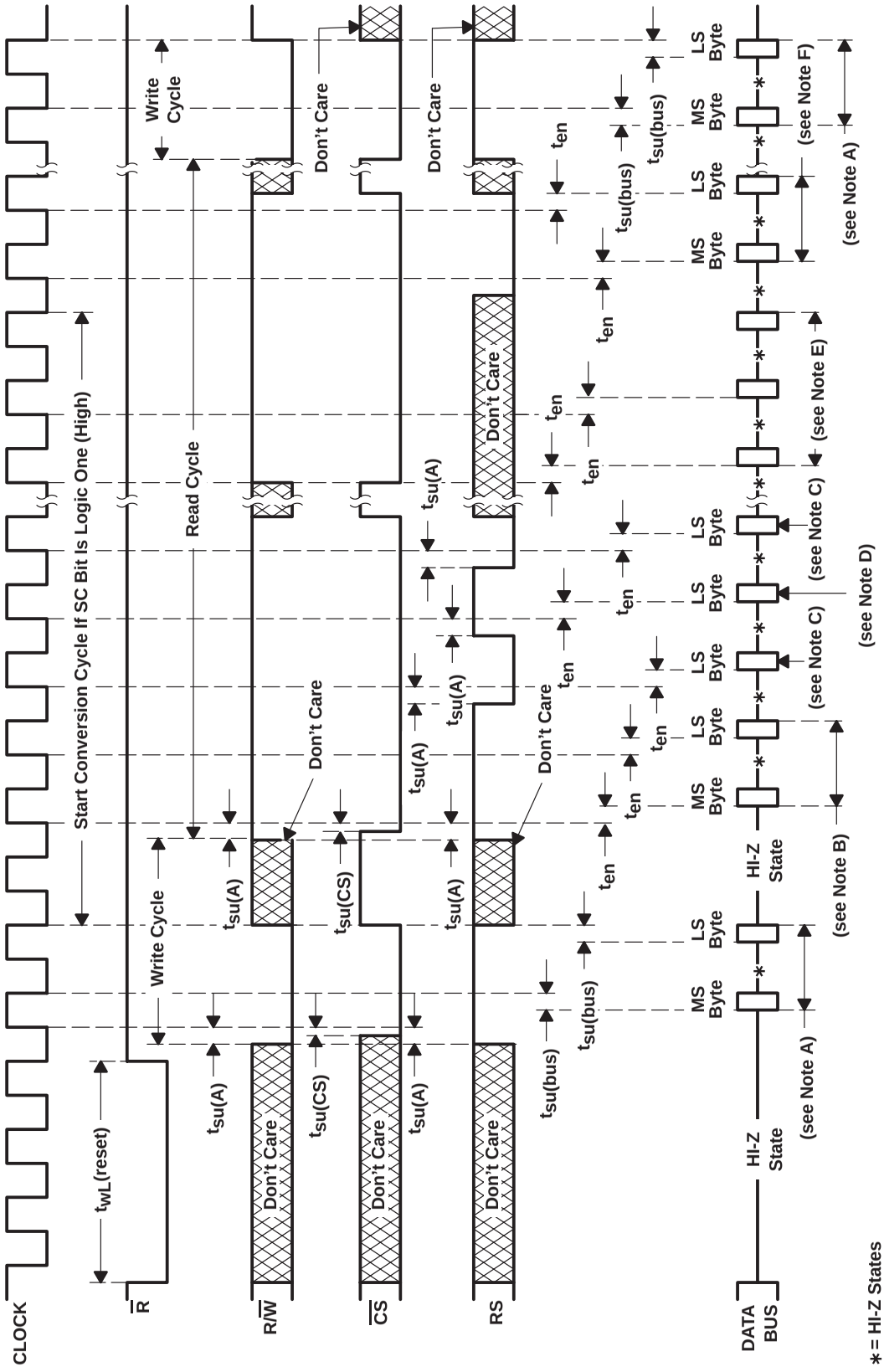
Detailed information on interfacing to most popular microprocessors is readily available from the factory.

## functional block diagram



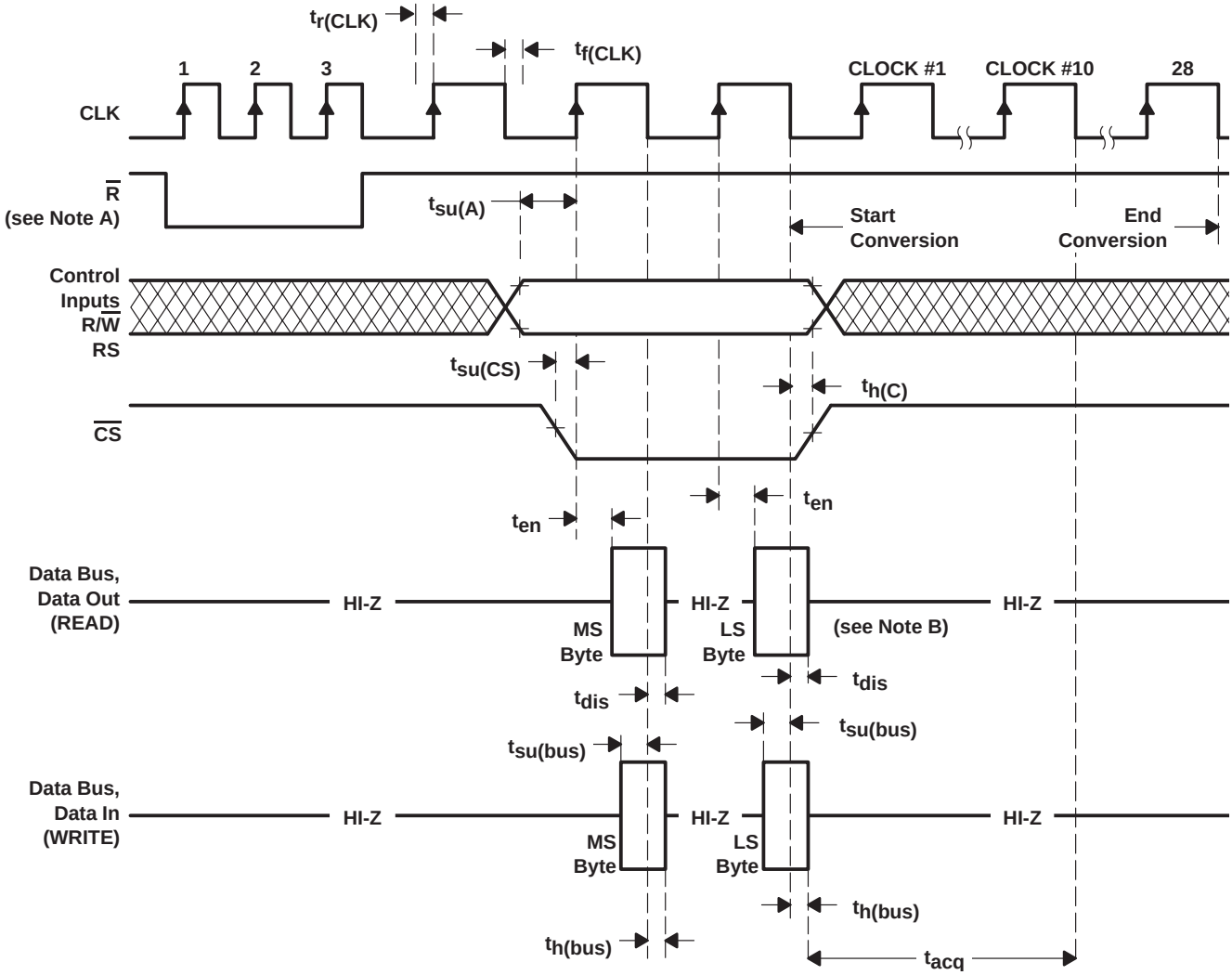
## PARAMETER MEASUREMENT INFORMATION

### typical operating sequence



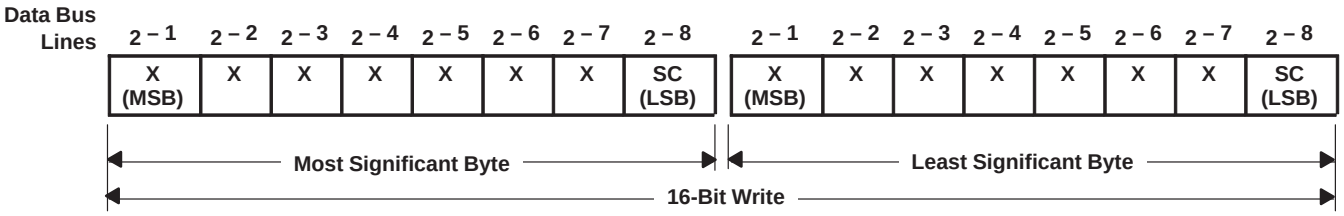

NOTES: A. This is a 16-bit input instruction from the microprocessor being sent to the control data register.
B. This is the 2-byte (16-bit) content of the digital data register being sent to the microprocessor.
C. This is the LS byte (8-bit) content of the analog conversion data register being sent to the microprocessor.
D. This is the LS byte (8-bit) content of the digital data register being sent to the microprocessor.
E. These are MS byte (8-bit), LS byte (8-bit), and LS byte (8-bit) content of the analog conversion data register or digital data register being sent to the microprocessor.
F. This is the 2-byte (16-bit) content of the analog conversion data register being sent to the microprocessor.

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The reset pulse ($\overline{R}$ low) is required only during powerup.
B. The most significant byte output of Data Out occurs when CLK is high. When CLK is low, Data Out is in the high-impedance (off) state. When CLK goes high again, the least significant byte is placed on the data bus. At this point, the least significant byte remains on the bus for as long as CLK is kept high.

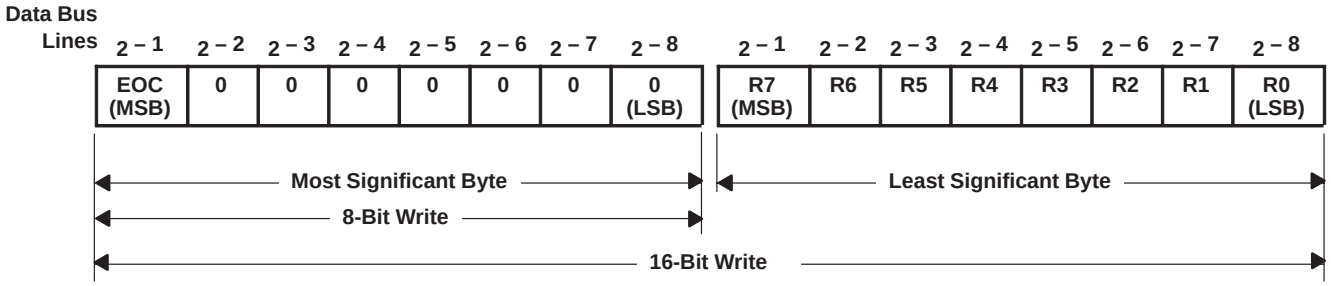
**Figure 1. Read or Write Cycle Voltage Waveforms**




Unused Bits (X) – The MS byte bits $2^{-1}$ through $2^{-7}$ and LS byte bits $2^{-1}$ through $2^{-4}$ of the control register are not used internally.
Start Conversion (SC) – When the SC bit in the MS byte is set to a logical 1, analog-to-digital conversion on the specified analog channel begins immediately after the completion of the control register write.
Analog Multiplex Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below:

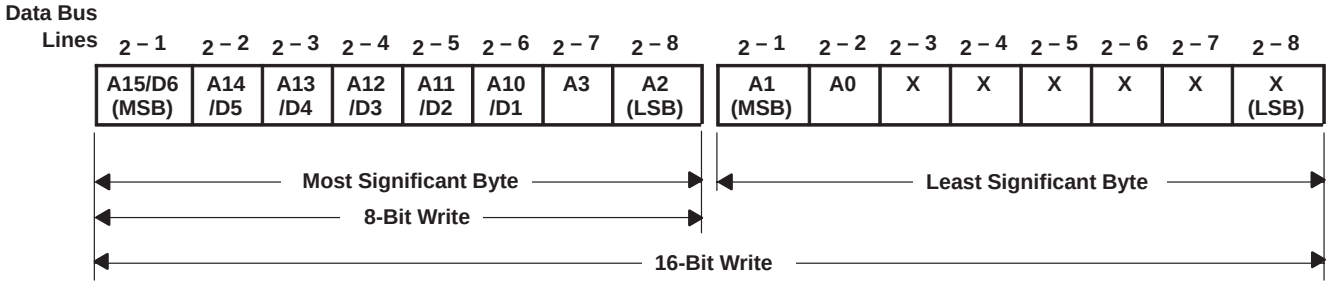
| Hexadecimal Address (A3 = MSB) | Channel Select |
|---|---|
| 0 | A0 |
| 1 | REF + (A1) |
| 2-5 | A2-A5 |
| 6-9 (not used) | |
| A-F | A10-A15 |

**Figure 2. Word Format and Content for Control Register 2-Byte Write**




A/D Status (EOC) – The A/D status end-of-conversion (EOC) bit is set whenever an analog-to-digital conversion is successfully completed by the A/D converter. The status bit is cleared by a 16-bit write from the microprocessor to the control register. The remainder of the bits in the MS byte of the analog conversion data register are always reset to logical 0 to simplify microprocessor interrogation of the A/D converter status.
A/D Result (R0-R7) – The LS byte of the analog conversion data register contains the result of the analog-to-digita

**Figure 3. Word Format and Content for Analog Conversion Data Register 1-Byte and 2-Byte Read**




Shared Digital Port (A10/D1-A15/D6) – The voltage present on these pins is interpreted as a digital signal, and the corresponding states are read from these bits. A digital value is given for each pin even if some or all of these pins are being used as analog inputs.
Analog Multiplexer Address (A0-A3) – The address of the selected analog channel presently addressed is given by these bits.
Unused Bits (X) – LS byte bits $2^{-3}$ through $2^{-8}$ of the digital data register are not used.

**Figure 4. Word Format And Content For Digital Data Register 1-Byte and 2-Byte Read**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . – 0.3 V to 6.5 V
Input voltage range: $V_{REF+}$ . . . . . $V_{REF–}$ to $V_{CC}$ + 0.3 V
$V_{REF–}$ . . . . . – 0.3 V to $V_{REF+}$
All other inputs . . . . . – 0.3 V to $V_{CC}$ + 0.3 V
Input current, $I_I$ (any input) . . . . . ± 10 V
Total input current, (all inputs) . . . . . ± 20 mA
Operating free-air temperature range TLC532AI, TLC533AI . . . . . – 40°C to 85°C
TLC532AM, TLC533AM . . . . . – 55°C to 1255°C
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 10 seconds: FN package . . . . . 260°C

† Stresses beyond those under absolute maximum ratings may causr permanent damage to the device. This is a stress rating only, and functional operation of the devise at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

### recommended operating conditions

| | | TLC532A | | | TLC533A | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.75 | 5 | 5.5 | 4.75 | 5 | 5.5 | V |
| Positive reference voltage, $V_{REF+}$ See Note 2 | | 2.5 | $V_{CC}$ | $V_{CC}$ + 0.1 | 2.5 | $V_{CC}$ | $V_{CC}$ + 0.1 | V |
| Negative reference voltage, $V_{REF–}$ See Note 2 | | – 0.1 | 0 | 2.5 | – 0.1 | 0 | 2.5 | V |
| Differential reference voltage, $V_{REF+} – V_{REF–}$ | | 1 | $V_{CC}$ | $V_{CC}$ + 0.2 | 1 | $V_{CC}$ | $V_{CC}$ + 0.2 | V |
| High-level input voltage, $V_{IH}$ | Clock input | $V_{CC}$ – 0.8 | | | $V_{CC}$ – 0.8 | | | V |
| | All other digital inputs | 2 | | | 2 | | | |
| Low-level input voltage, $V_{IL}$ | Any digital input | | | 0.8 | | | 0.8 | V |
| Clock frequency, $f_{CLK}$ | | 0.1 | 2 | 2.048 | 0.1 | 1.048 | 1.06 | MHz |
| Setup time, $\overline{CS}$ low before CLK ↑, $t_{su(CS)}$ | | 75 | | | 100 | | | ns |
| Setup time, Address (R/$\overline{W}$ and RS) before CLK ↑, $t_{su(A)}$ | | 100 | | | 145 | | | ns |
| Setup time, Data bus input before start conversion, $t_{su(bus)}$ | | 140 | | | 185 | | | ns |
| Hold time, Control (R/$\overline{W}$, RS, and CS) after start conversion, $t_{h(C)}$ | | 10 | | | 20 | | | ns |
| Hold time, Data bus input after start conversion, $t_{h(bus)}$ | | 15 | | | 20 | | | ns |
| Pulse duration of control during read, $t_{w(C)}$ | | 305 | | | 575 | | | ns |
| Pulse druation, reset low, $t_{wL(reset)}$ | | 3 | | | 3 | | | Clock Cycles |
| Pulse duration, clock high, $t_{w(CLKH)}$ | | 230 | | | 440 | | | ns |
| Pulse duration,clock low, $t_{w(CLKL)}$ | | 200 | | | 410 | | | ns |
| Clock rise time, $t_{r(CLK)}$ | | | | 15 | | | 25 | ns |
| Clock fall time, $t_{f(CLK)}$ | | | | 16 | | | 30 | ns |
| Operating free-air temperature, $T_A$ | TLC__AM | – 55 | | 125 | – 55 | | 125 | °C |
| | TLC__AI | – 40 | | 85 | – 40 | | 85 | |

NOTE 2: Analog input voltages greater than or equal to that applied to the REF+ terminal convert to all ones (11111111), while input voltages equal to or less than that applied to the REF– terminal convert to all zeros (00000000). For proper operation, the positive reference voltage, $V_{REF+}$, must be at least 1 V greater than the negative reference voltage, $V_{REF–}$. In addition, unadjusted errors may increase as the differential reference voltage, $V_{REF+} – V_{REF–}$, falls below 4.75 V.

## electrical characteristics over recommended operating free-air temperature range, $V_{REF+} = V_{CC}$, $V_{REF-}$ at ground, $f_{CLK}$ = 2 MHz (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = – 1.6 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current | Any digital or Clock input | $V_{IH}$ = 5.5 V | | | 10 | µA |
| | | Any control input | | | | 1 | |
| $I_{IL}$ | Low-level input current | Any digital or Clock input | $V_{IL}$ = 0 | | | – 10 | µA |
| | | Any control input | | | | – 1 | |
| $I_{OZ}$ | Off-state (high-impdance state) output current | | $V_O = V_{CC}$ | | | 10 | µA |
| | | | $V_O$ = 0 | | | – 10 | |
| $I_I$ | Analog input current (see Note 3) | | $V_I$ = 0 to $V_{CC}$ | | | ±500 | nA |
| | Leakage current between selected channel and all other analog channels | | $V_I$ = 0 to $V_{CC}$, Clock input at 0 V | | | ±400 | nA |
| $C_i$ | Input capacitance | Digital pins 3 thru 10 | | | 4 | 30 | pF |
| | | Any other input pin | | | 2 | 15 | |
| $I_{CC} + I_{REF+}$ | Supply current plus reference current | | $V_{CC} = V_{REF+}$ = 5.5 V, Outputs open | | 1.5 | 3 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = 5.5 V | | 1.4 | 2 | mA |

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

## operating chacteristics over recommended ranges $V_{CC}$, $V_{REF+}$, and operating free-air temperature, $V_{REF-}$ at ground, $f_{clock}$ = 2 MHz (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Linearity error (see Note 4) | | | | | ±0.5 | LSB |
| | Zero error (see Note 5) | | | | | ±0.5 | LSB |
| | Full-scale error (see Note 5) | | | | | ±0.5 | LSB |
| | Total unadjusted error (see Note 6) | | | | | ±0.5 | LSB |
| | Absolute accuracy error (see Note 7) | | | | | ±1 | LSB |
| $t_{conv}$ | Conversion time (including channel acquisition time) | | | | 30 | | Clock Cycles |
| $t_{acq}$ | Channel acquisition time prior to starting conversion | | | | 10 | | Clock Cycles |
| $t_{en}$ | Data output enable time (see Note 8) | | $C_L$ = 50 pF, $R_L$ = 3 kΩ | | | 250 | ns |
| $t_{dis}$ | Data output disable time | | $C_L$ = 50 pF, $R_L$ = 3 kΩ | 10 | | | ns |
| $t_r$(bus) | Data output rise time | High-impedance to high level | $C_L$ = 50 pF, $R_L$ = 3 kΩ | | | 150 | ns |
| | | Low-to-high level | | | | 300 | |
| $t_f$(bus) | Data output fall time | High-impedance to low level | $C_L$ = 50 pF, $R_L$ = 3 kΩ | | | 150 | ns |
| | | High-to-low level | | | | 300 | |

† Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

NOTES: 4. Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6. Total unadjusted error is the sum of liinearity, zero, and full-scale errors.
7. Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters' finite resolution.
8. If chip-select setup time, $t_{su(CS)}$, is less than 0.14 µs, the effective data output enable time, $t_{en}$, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 µs.

## electrical characteristics over recommended ranges $V_{CC}$, $V_{REF+}$, and operating free-air temperature, $V_{REF-}$ at ground, $f_{CLK}$ = 1.048 MHz (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = – 1.6 mA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| $I_{IH}$ | High-level input current | Any digital or Clock input | $V_{IH}$ = 5.5 V | | | 10 | µA |
| | | Any control input | | | | 1 | |
| $I_{IL}$ | Low-level input current | Any digital or Clock input | $V_{IL}$ = 0 | | | – 10 | µA |
| | | Any control input | | | | – 1 | |
| $I_{OZ}$ | Off-state (high-impdance state) output current | | $V_O = V_{CC}$ | | | 10 | µA |
| | | | $V_O$ = 0 | | | – 10 | |
| $I_I$ | Analog input current (see Note 3) | | $V_I$ = 0 to $V_{CC}$ | | | ±500 | nA |
| | Leakage current between selected channel and all other analog channels | | $V_I$ = 0 to $V_{CC}$, Clock input at 0 V | | | ±400 | nA |
| $C_i$ | Input capacitance | Digital pins 3 thru 10 | | | 4 | 30 | pF |
| | | Any other input pin | | | 2 | 15 | |
| $I_{CC} + I_{REF+}$ | Supply current plus reference current | | $V_{CC} = V_{REF+}$ = 5.5 V, Outputs open | | 1.5 | 3 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = 5.5 V | | 1.2 | 2 | mA |

NOTE 3: Analog input current is an average of the current flowing into a selected analog channel input during one full conversion cycle.

## operating chacteristics over recommended operating free-air temperature range, $V_{REF+} = V_{CC}$, $V_{REF-}$ at ground, $f_{CLK}$ = 1.048 MHz (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Linearity error (see Note 4) | | | | | ±0.5 | LSB |
| | Zero error (see Note 5) | | | | | ±0.5 | LSB |
| | Full-scale error (see Note 5) | | | | | ±0.5 | LSB |
| | Total unadjusted error (see Note 6) | | | | | ±0.5 | LSB |
| | Absolute accuracy error (see Note 7) | | | | | ±1 | LSB |
| $t_{conv}$ | Conversion time (including channel acquisition time) | | | | 30 | | Clock Cycles |
| $t_{acq}$ | Channel acquisition time prior to starting conversion | | | | 10 | | Clock Cycles |
| $t_{en}$ | Data output enable time See Note 8 | | $C_L$ = 50 pF, $R_L$ = 3 kΩ | | | 335 | ns |
| $t_{dis}$ | Data output disable time | | $C_L$ = 50 pF, $R_L$ = 3 kΩ | 10 | | | ns |
| $t_r$(bus) | Data bus output rise time | High-impedance to high level | $C_L$ = 50 pF, $R_L$ = 3 kΩ | | | 150 | ns |
| | | Low-to-high level | | | | 300 | |
| $t_f$(bus) | Data bus output fall time | High-impedance to low level | $C_L$ = 50 pF, $R_L$ = 3 kΩ | | | 150 | ns |
| | | High-to-low level | | | | 300 | |

† Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

NOTES: 4 Linearity error is the deviation from the best straight line through the A/D transfer characteristics.
5 Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
6 Total unadjusted error is the sum of liinearity, zero, and full-scale errors.
7 Absolute accuracy error is the maximum difference between an analog value and the nominal midstep value within any step. This includes all errors including inherent quantization error, which is the ±0.5 LSB uncertainty caused by the A/D converters' finite resolution.
8 If chip-select setup time, $t_{su(CS)}$, is less than 0.14 µs, the effective data output enable time, $t_{en}$, may extend such that $t_{su(CS)} + t_{en}$ is equal to a maximum of 0.475 µs.

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