

SN54HCT273, SN74HCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS068C – NOVEMBER 1988 – REVISED MAY 1997

- Inputs Are TTL-Voltage Compatible
- Contain Eight D-Type Flip-Flops
- Direct Clear Input
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

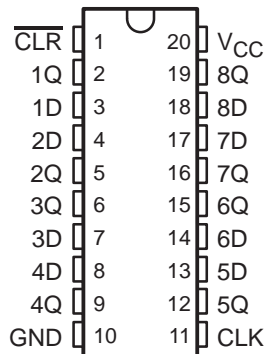
description

These devices are positive-edge-triggered D-type flip-flops with a common enable input. The 'HCT273 are similar to the 'HCT377, but feature a common clear enable ($\overline{\text{CLR}}$) input instead of a latched clock.

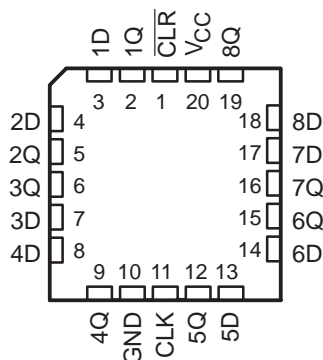
Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. The circuits are designed to prevent false clocking by transitions at $\overline{\text{CLR}}$.

The SN54HCT273 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT273 is characterized for operation from -40°C to 85°C .

SN54HCT273 . . . J OR W PACKAGE
SN74HCT273 . . . DW, N, OR PW PACKAGE
(TOP VIEW)



SN54HCT273 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀



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 **TEXAS
INSTRUMENTS**

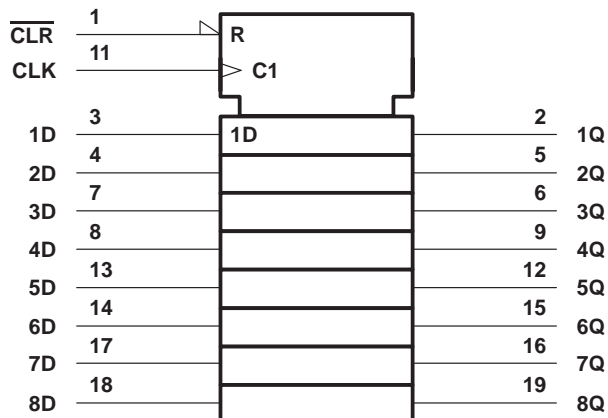
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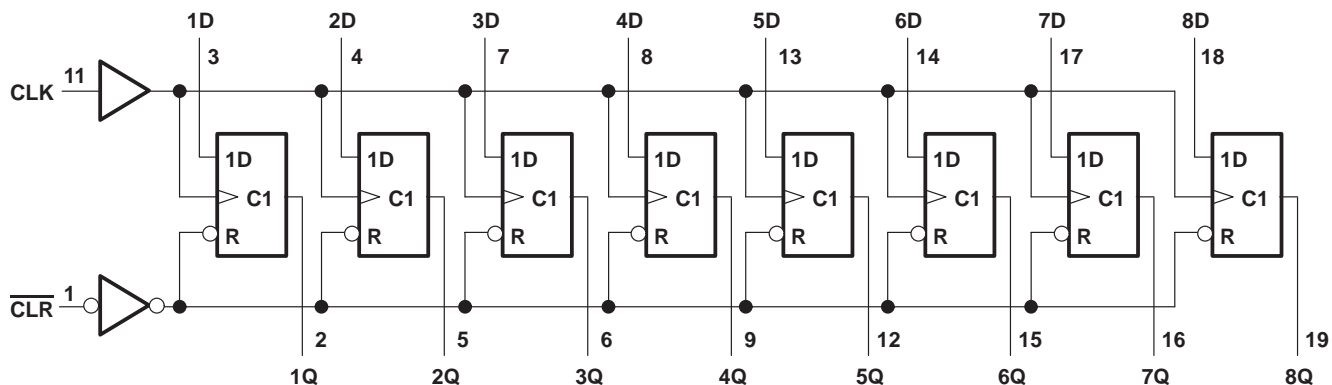
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logic symbol†

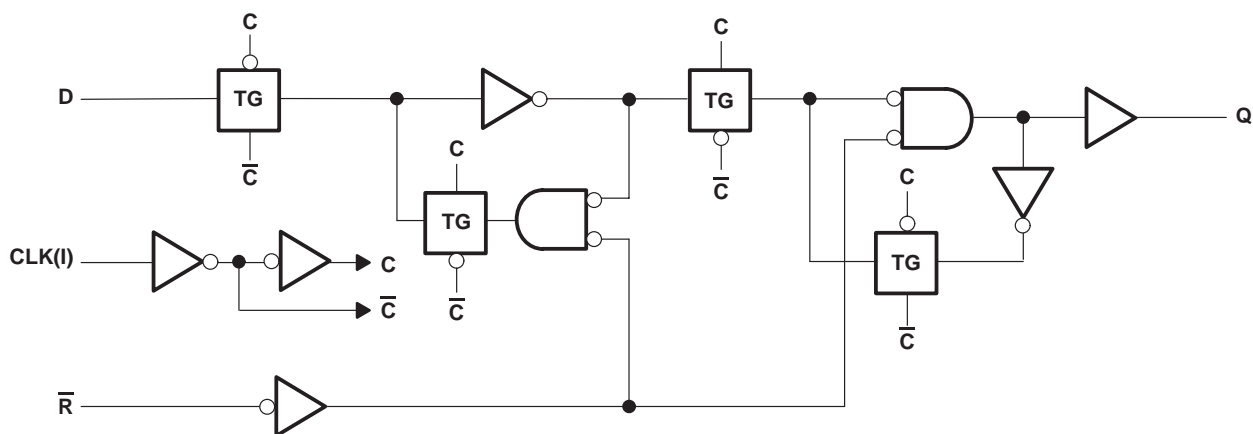


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



logic diagram, each flip-flop (positive logic)



SN54HCT273, SN74HCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JE51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54HCT273			SN74HCT273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0			V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	0			500			ns
T_A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT273		SN74HCT273		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$	4.5 V	4.4	4.499	4.4	4.4		V	
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.30	3.7	3.84			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$	4.5 V		0.001	0.1	0.1	0.1	V	
		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26	0.4	0.33		
I_I	$V_I = V_{CC}$ or 0	5.5 V		± 0.1	± 100	± 1000	± 1000	nA		
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V			8	160	80	μA		
ΔI_{CC}^\ddagger	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}	5.5 V		1.4	2.4	3	2.9	mA		
C_i		4.5 V to 5.5 V		3	10	10	10	pF		

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HCT273		SN74HCT273		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	4.5 V	0	25	0	16	0	20	MHz
		5.5 V	0	28	0	19	0	23	
t _w	Pulse duration	CLK high or low	4.5 V	20	30	25			ns
			5.5 V	18	25	22			
	CLR low	4.5 V	16	24	20				
		5.5 V	14	20	17				
t _{su}	Setup time before CLK↑	Data	4.5 V	20	30	25		ns	
			5.5 V	17	25	21			
	CLR inactive	4.5 V	20	30	25				
		5.5 V	17	25	21				
t _h	Hold time data after CLK↑	4.5 V	0	0	0		ns		
		5.5 V	0	0	0				

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54HCT273				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
f _{max}			4.5 V	25	31		16	MHz	
			5.5 V	28	37		19		
t _{pd}	CLR	Any	4.5 V		15	34		50	ns
			5.5 V		12	29		42	
t _{PHL}	CLR	Any	4.5 V		17	15		50	ns
			5.5 V		15	34		42	
t _t		Any	4.5 V		8	18		22	ns
			5.5 V		7	19		21	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74HCT273				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
f _{max}			4.5 V	25	31		20	MHz	
			5.5 V	28	37		23		
t _{pd}	CLR	Any	4.5 V		15	34		42	ns
			5.5 V		12	29		36	
t _{PHL}	CLR	Any	4.5 V		17	34		42	ns
			5.5 V		15	29		36	
t _t		Any	4.5 V		8	15		19	ns
			5.5 V		7	14		17	

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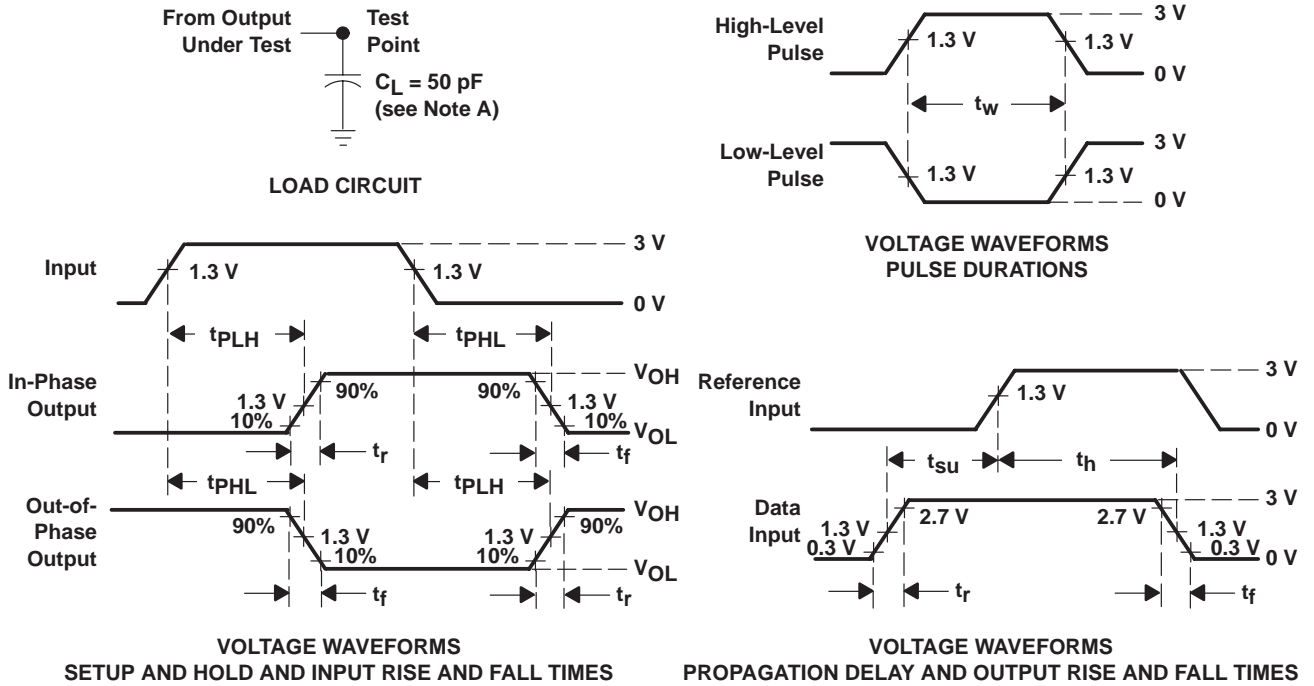


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operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	30	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.
 D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 E. t_{pLH} and t_{pHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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