

# SN54HC74, SN74HC74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

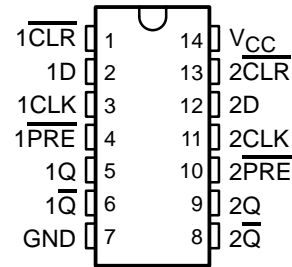
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 40- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 15$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max

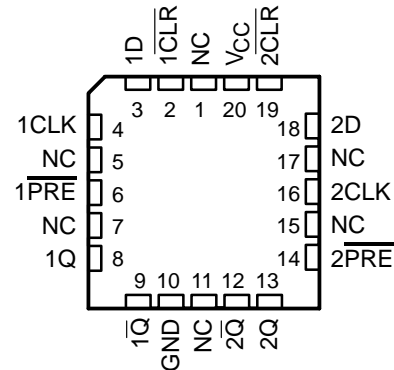
## description/ordering information

The 'HC74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ( $\overline{PRE}$ ) or clear ( $\overline{CLR}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{PRE}$  and  $\overline{CLR}$  are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

SN54HC74 . . . J OR W PACKAGE  
SN74HC74 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HC74 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC74N	SN74HC74N
	SOIC – D	Tube of 50	SN74HC74D	HC74
		Reel of 2500	SN74HC74DR	
		Reel of 250	SN74HC74DT	
	SOP – NS	Reel of 2000	SN74HC74NSR	HC74
	SSOP – DB	Reel of 2000	SN74HC74DBR	HC74
	TSSOP – PW	Tube of 90	SN74HC74PW	HC74
Reel of 2000		SN74HC74PWR		
Reel of 250		SN74HC74PWT		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC74J	SNJ54HC74J
	CFP – W	Tube of 150	SNJ54HC74W	SNJ54HC74W
	LCCC – FK	Tube of 55	SNJ54HC74FK	SNJ54HC74FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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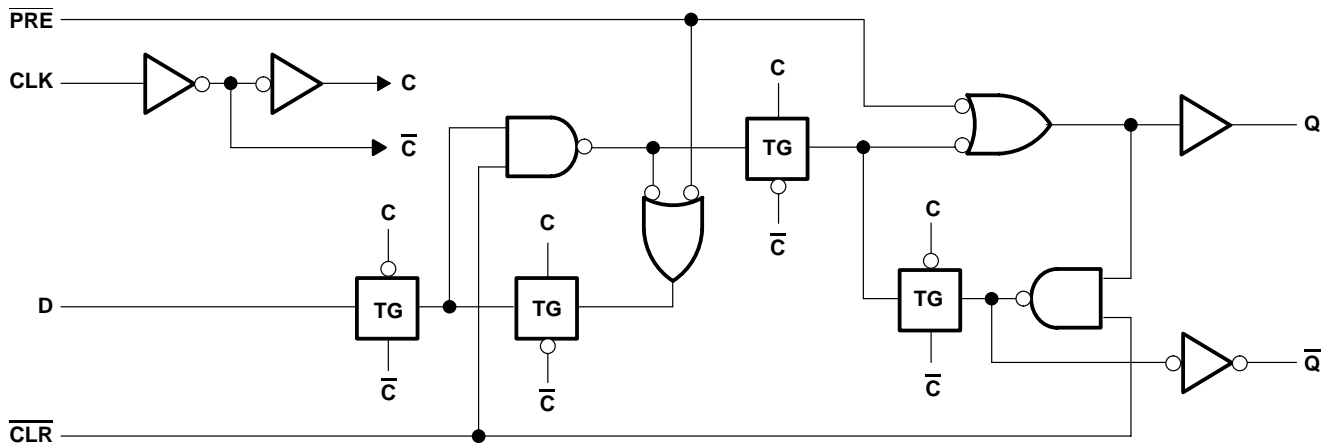
SCLS094D – DECEMBER 1982 – REVISED JULY 2003

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>

† This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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SCLS094D – DECEMBER 1982 – REVISED JULY 2003

## recommended operating conditions (see Note 3)

		SN54HC74			SN74HC74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5	1.5		V	
		V <sub>CC</sub> = 4.5 V		3.15	3.15			
		V <sub>CC</sub> = 6 V		4.2	4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V			0.5		0.5	V
		V <sub>CC</sub> = 4.5 V			1.35		1.35	
		V <sub>CC</sub> = 6 V			1.8		1.8	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 2 V			1000		1000	ns
		V <sub>CC</sub> = 4.5 V			500		500	
		V <sub>CC</sub> = 6 V			400		400	
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC74		SN74HC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			4		80		40	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF



# SN54HC74, SN74HC74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SCLS094D – DECEMBER 1982 – REVISED JULY 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC74		SN74HC74		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency	2 V	6		4.2		5		MHz	
		4.5 V	31		21		25			
		6 V	0	36	0	25	0	29		
t <sub>w</sub>	Pulse duration	PRE or CLR low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
	CLK high or low	2 V	80		120		100			
		4.5 V	16		24		20			
		6 V	14		20		17			
t <sub>su</sub>	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
	PRE or CLR inactive	2 V	25		40		30			
		4.5 V	5		8		6			
		6 V	4		7		5			
t <sub>h</sub>	Hold time, data after CLK↑	2 V	0		0		0		ns	
		4.5 V	0		0		0			
		6 V	0		0		0			

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC74		SN74HC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	10		4.2		5	MHz	
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t <sub>pd</sub>	PRE or CLR	Q or Q̄	2 V		70	230		345		290	ns
			4.5 V		20	46		69		58	
			6 V		15	39		59		49	
	CLK	Q or Q̄	2 V		70	175		250		220	
			4.5 V		20	35		50		44	
			6 V		15	30		42		37	
t <sub>t</sub>		Q or Q̄	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T<sub>A</sub> = 25°C

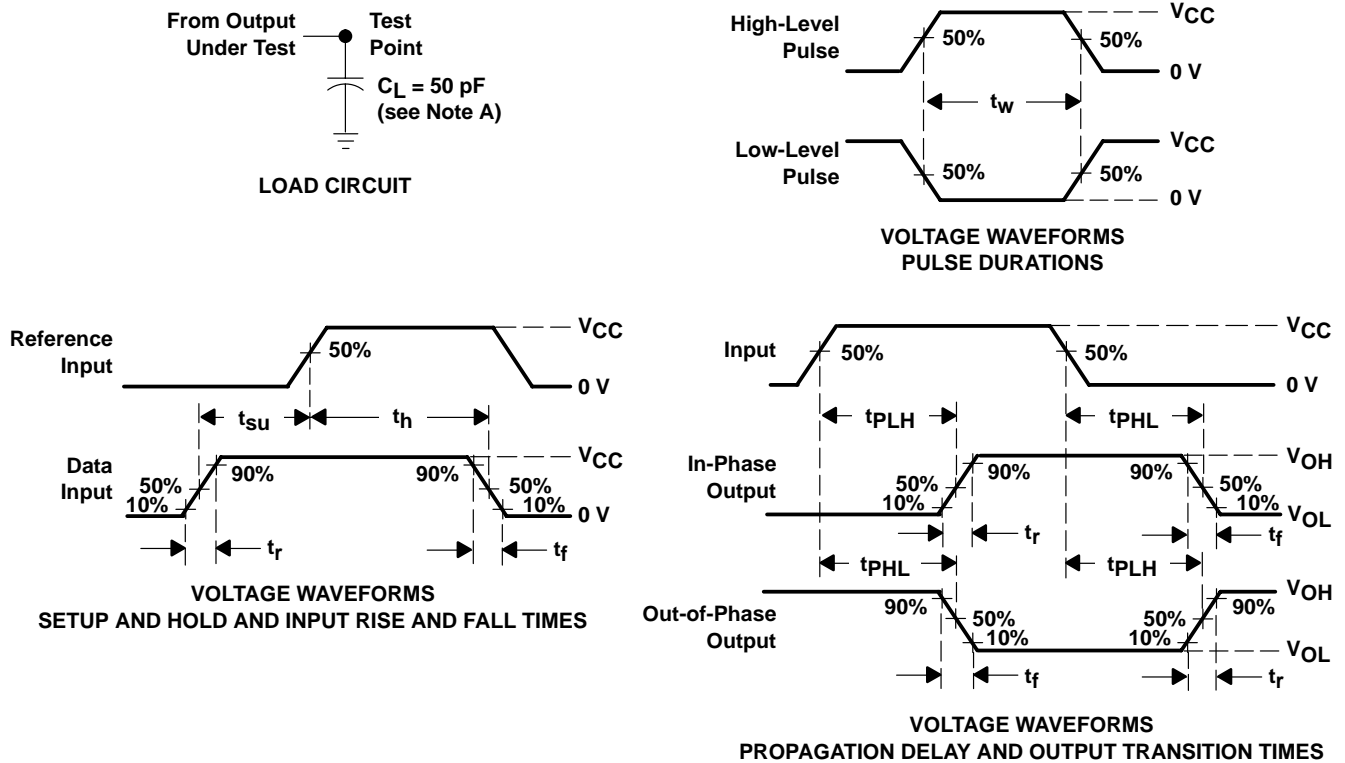
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per flip-flop	No load	35	pF



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SCLS094D – DECEMBER 1982 – REVISED JULY 2003

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

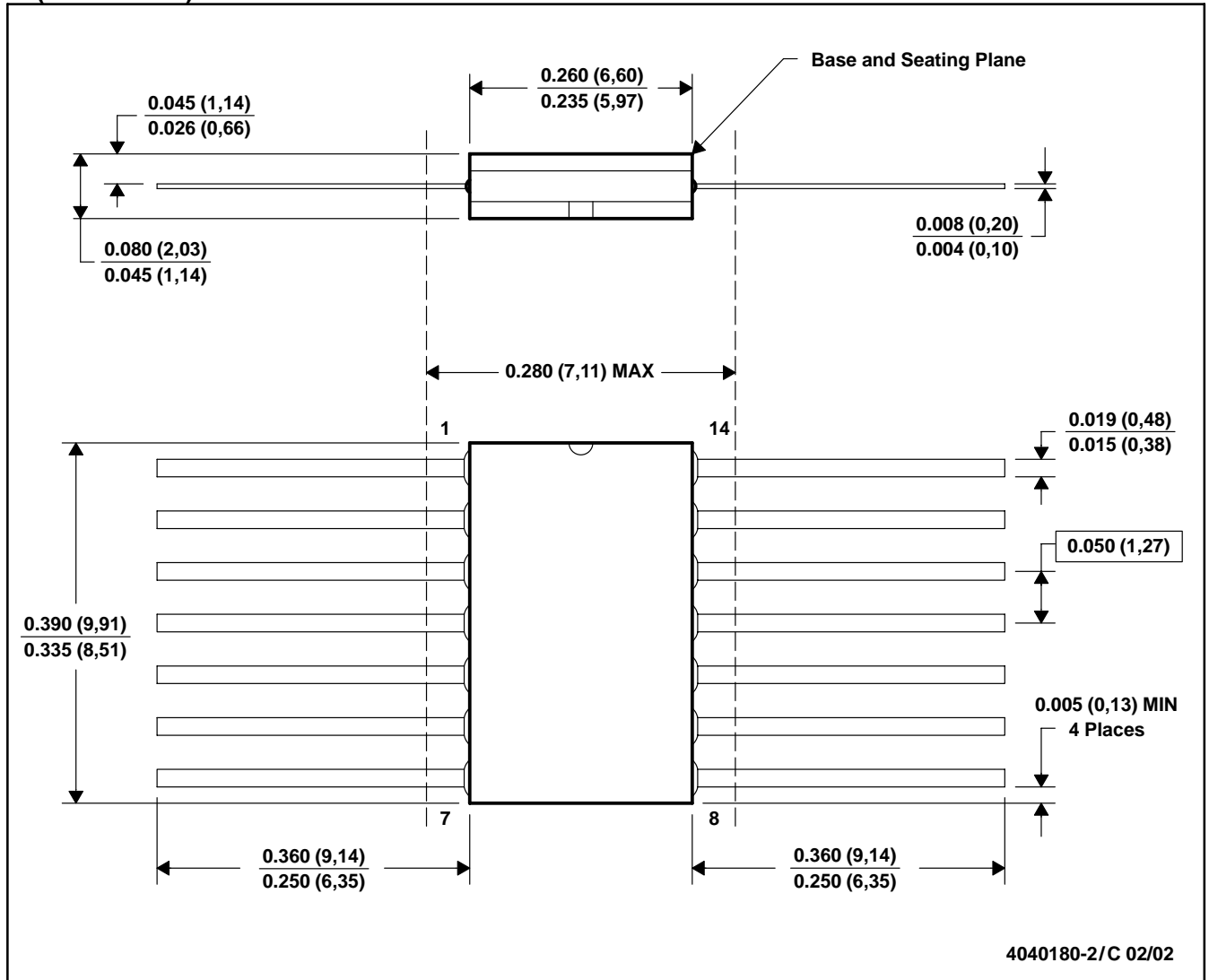


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

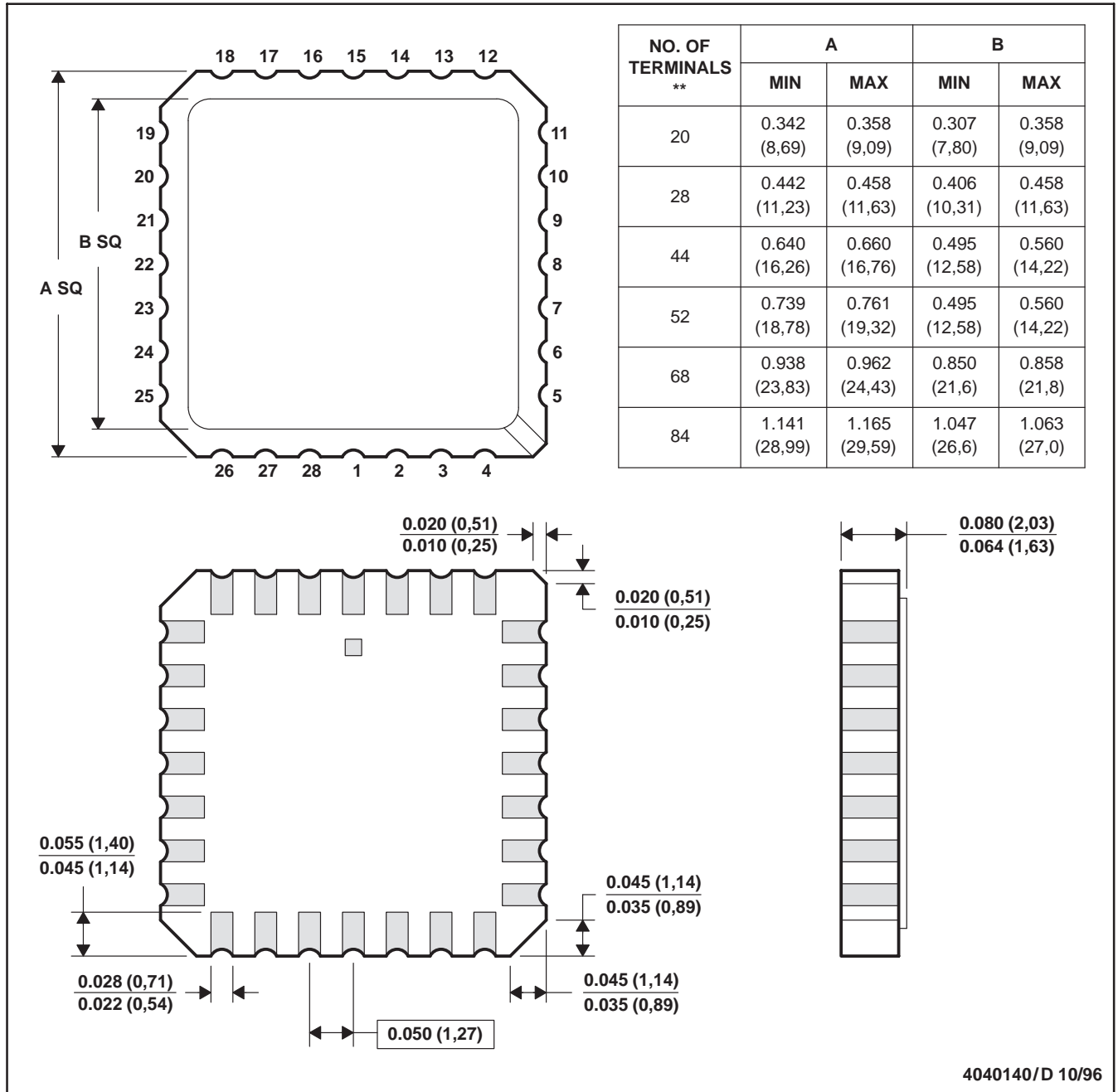


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



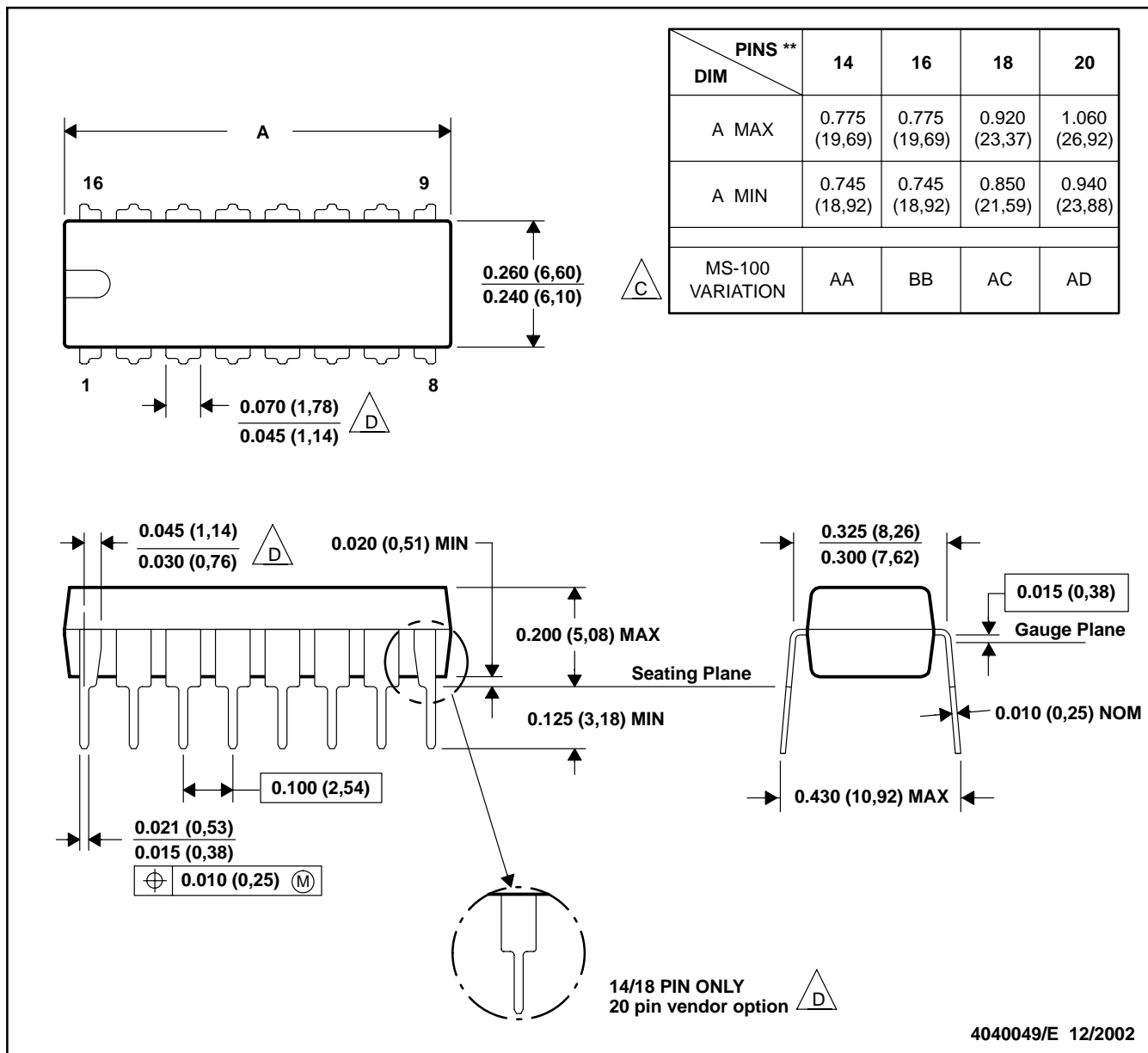
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

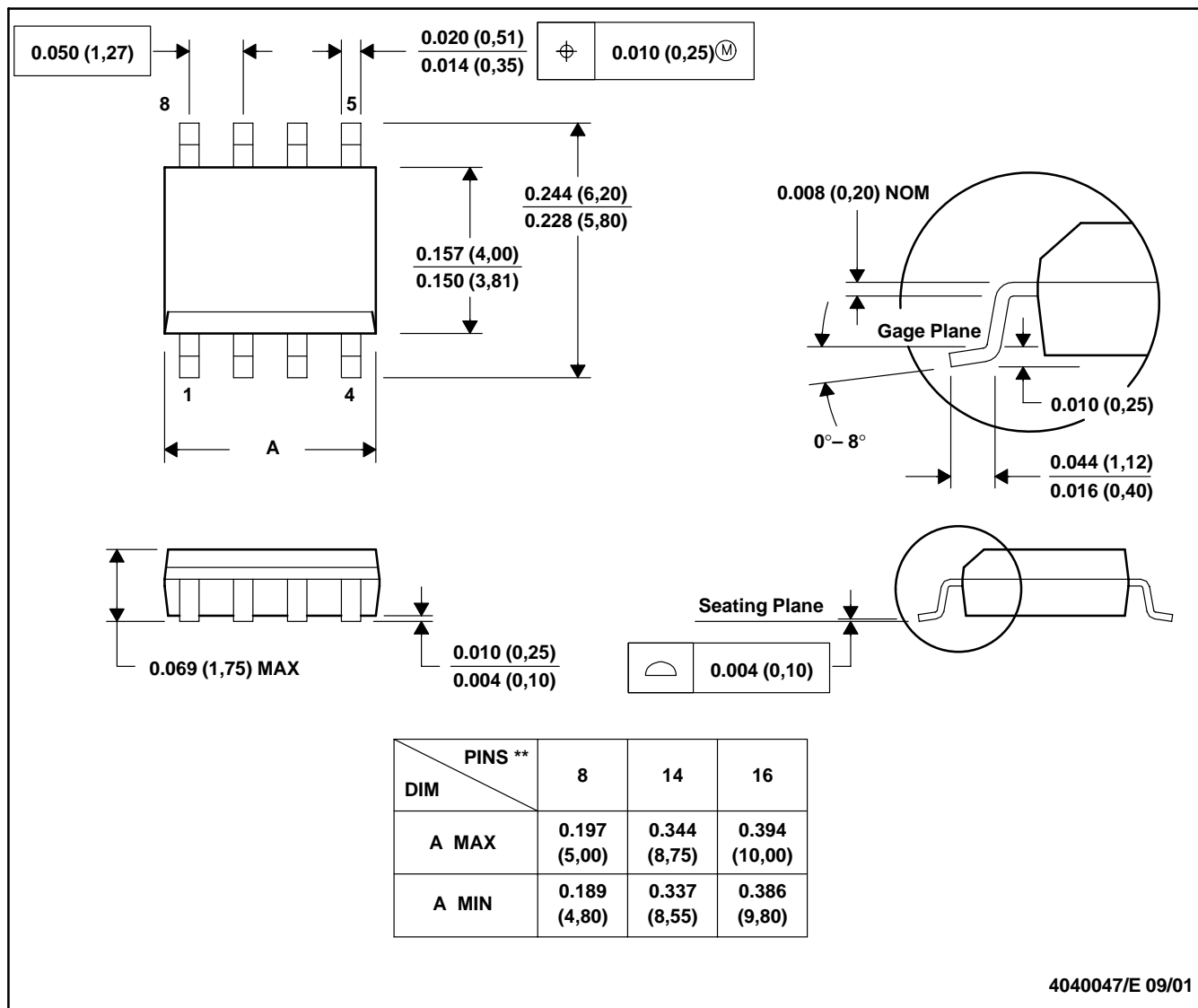


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



4040047/E 09/01

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

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