

**SN54AHC05, SN74AHC05**  
**HEX INVERTERS**  
**WITH OPEN-DRAIN OUTPUTS**  
 SCLS357F – MAY 1997 – REVISED JANUARY 2000

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Operating Range 2-V to 5.5-V V<sub>CC</sub>**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs**

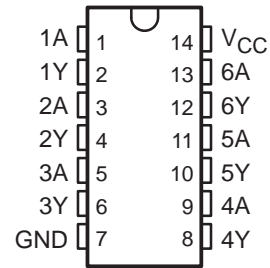
**description**

The 'AHC05 devices contain six independent inverters. These devices perform the Boolean function  $Y = \bar{A}$ .

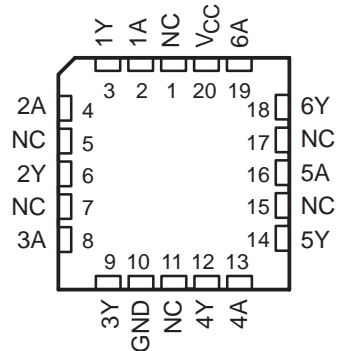
The open-drain outputs require pullup resistors to perform correctly. They can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The SN54AHC05 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AHC05 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**SN54AHC05 . . . J OR W PACKAGE**  
**SN74AHC05 . . . D, DB, DGV, N, OR PW PACKAGE**  
**(TOP VIEW)**



**SN54AHC05 . . . FK PACKAGE**  
**(TOP VIEW)**



NC – No internal connection

**FUNCTION TABLE**  
**(each inverter)**

INPUT A	OUTPUT Y
H	L
L	H



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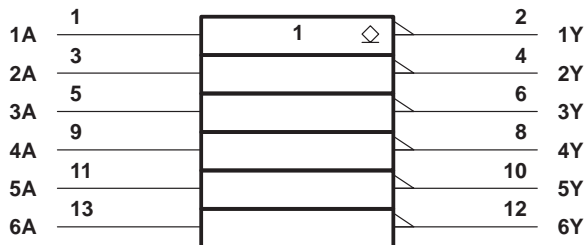


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**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, N, PW, and W packages.

**logic diagram, each inverter (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package .....	86°C/W
DB package .....	96°C/W
DGV package .....	127°C/W
N package .....	80°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions (see Note 3)**

		SN54AHC05		SN74AHC05		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5		V
		V <sub>CC</sub> = 3 V		2.1		
		V <sub>CC</sub> = 5.5 V		3.85		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		V
		V <sub>CC</sub> = 3 V		0.9		
		V <sub>CC</sub> = 5.5 V		1.65		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		μA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4		
		V <sub>CC</sub> = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100		ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC05		SN74AHC05		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	0.1	0.1	V	
		3 V			0.1	0.1	0.1			
		4.5 V			0.1	0.1	0.1			
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.5	0.44			
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.5	0.44			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1	±1*	±1	μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2	20	20	μA		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10		10	pF		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54AHC05		SN74AHC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLZ</sub>	A	Y	C <sub>L</sub> = 15 pF		2.9**	7.1**	1**	8.5**	1	8.5	ns
t <sub>PZL</sub>					4**	7.1**	1**	8.5**	1	8.5	
t <sub>PLZ</sub>	A	Y	C <sub>L</sub> = 50 pF		4.7	10.6	1	12	1	12	ns
t <sub>PZL</sub>					5.8	10.6	1	12	1	12	

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC05		SN74AHC05		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLZ}$	A	Y	$C_L = 15\text{ pF}$	2.2*	5.5*	1*	6.5*	1	6.5	ns	
$t_{PZL}$				2.9*	5.5*	1*	6.5*	1	6.5		
$t_{PLZ}$	A	Y	$C_L = 50\text{ pF}$	3.4	7.5	1	8.5	1	8.5	ns	
$t_{PZL}$				4.2	7.5	1	8.5	1	8.5		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

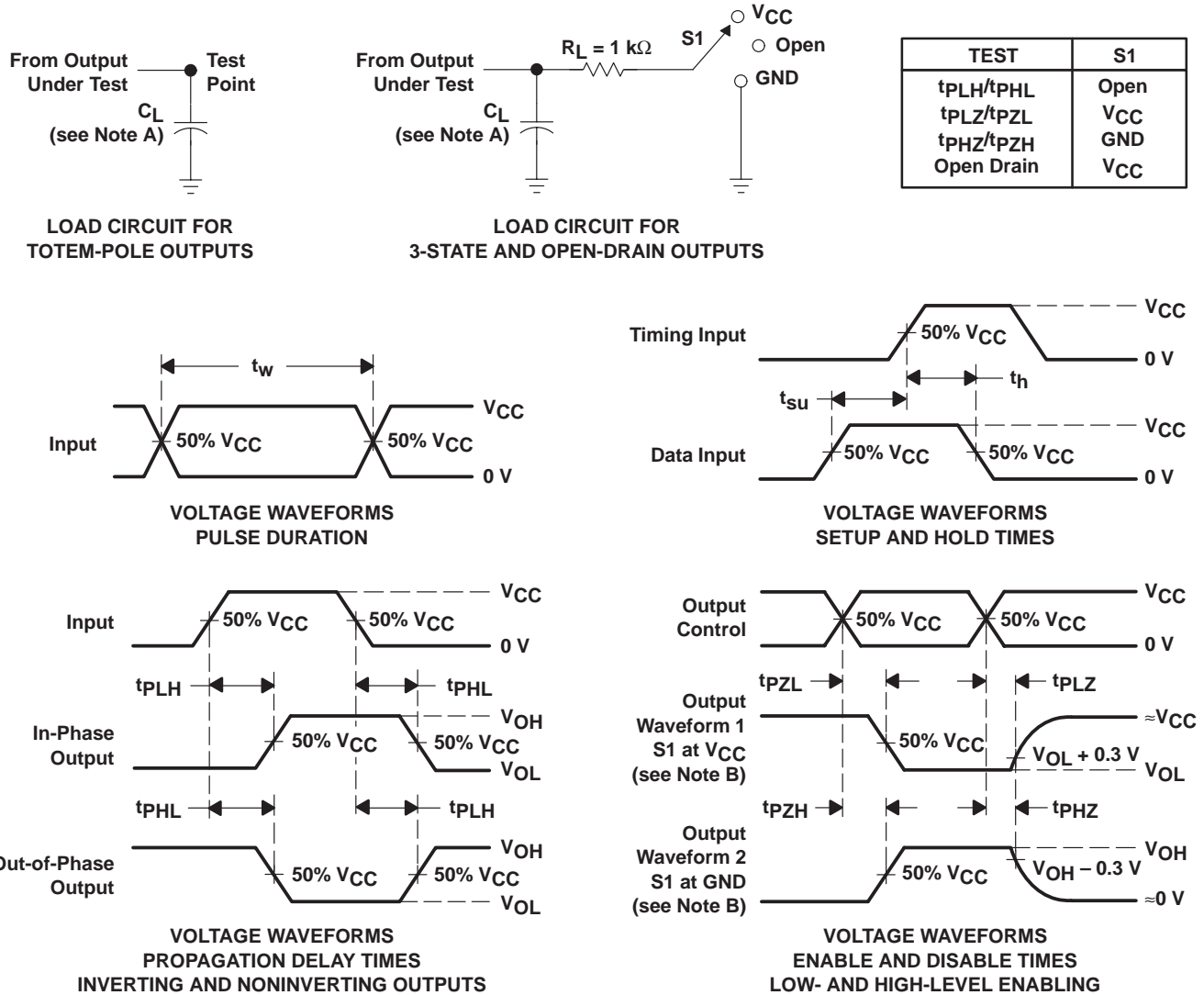
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	3	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 3 ns, t<sub>f</sub> ≤ 3 ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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