

# CD74HC109, CD74HCT109

## Dual J-K̄ Flip-Flop with Set and Reset Positive-Edge Trigger

### Features

- Asynchronous Set and Reset
- Schmitt Trigger Clock Inputs
- Typical Propagation Delay = 18ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Typical  $f_{MAX} = 60MHz$  at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$

at  $V_{CC} = 5V$

- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC109 and CD74HCT109 are dual J-K̄ flip-flops with set and reset. The flip-flop changes state with the positive transition of Clock (1CP and 2CP).

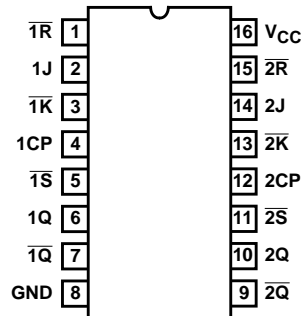
The flip-flop is set and reset by active-low  $\bar{S}$  and  $\bar{R}$ , respectively. A low on both the set and reset inputs simultaneously will force both Q and  $\bar{Q}$  outputs high. However, both set and reset going high simultaneously results in an unpredictable output condition.

### Ordering Information

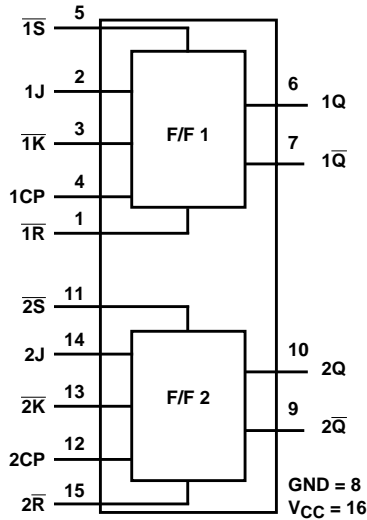
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.

### Pinout

CD74HC109, CD74HCT109  
(PDIP, SOIC)  
TOP VIEW



**Functional Diagram**



**TRUTH TABLE**

INPUTS					OUTPUTS	
$\bar{S}$	$\bar{R}$	CP	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 3)	H (Note 3)
H	H	$\uparrow$	L	L	L	H
H	H	$\uparrow$	H	L	Toggle	
H	H	$\uparrow$	L	H	No Change	
H	H	$\uparrow$	H	H	H	$\bar{L}$
H	H	L	X	X	No Change	

**NOTES:**

H= High Level (Steady State)

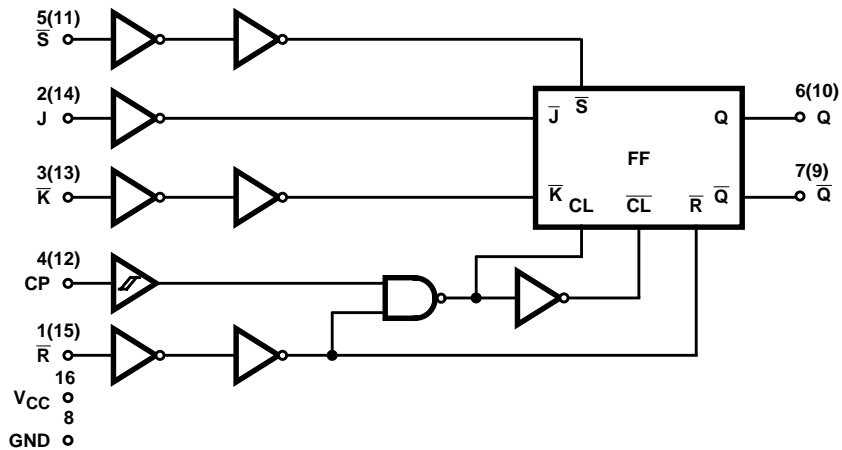
L= Low Level (Steady State)

X= Don't Care

$\uparrow$ = Low-to-High Transition

3. Unpredictable and unstable condition if both  $\bar{S}$  and  $\bar{R}$  go high simultaneously.

**Logic Diagram**



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## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	160
Maximum Junction Temperature (Hermetic Package or Die) . . .	$175^{\circ}C$
Maximum Junction Temperature (Plastic Package) .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	$.2V$ to $6V$
HCT Types .....	$4.5V$ to $5.5V$
DC Input or Output Voltage, $V_I, V_O$ .....	$0V$ to $V_{CC}$
$C_P$ Input Rise and Fall Time, $t_r, t_f$	
2V .....	$1.0ms$ (Max)
4.5V .....	$1.0ms$ (Max)
6V .....	$1.0ms$ (Max)
Input Rise and Fall Time (All Inputs Except $C_P$ ), $t_r, t_f$	
2V .....	$1000ns$ (Max)
4.5V .....	$500ns$ (Max)
6V .....	$400ns$ (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>													
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
				4.5	4.4	-	-	4.4	-	4.4	-	V	
				6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V	
				-4	4.5	3.96	-	-	3.84	-	3.7	-	V
				-5.2	6	5.48	-	-	5.34	-	5.2	-	V

## CD74HC109, CD74HCT109

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS	
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
				4.5	-	-	0.1	-	0.1	-	0.1	V	
				6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-	-	-	-	-	-	-	-	-	V	
				4	4.5	-	-	0.26	-	0.33	-	0.4	V
				5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	6	-	-	4	-	40	-	80	μA	
<b>HCT TYPES</b>													
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V	
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V	
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-	4.5	4.4	-	-	4.4	-	4.4	-	V	
High Level Output Voltage TTL Loads			-0.02	4.5	3.98	-	-	3.84	-	3.7	-	V	
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-4	4.5	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads			0.02	4.5	-	-	0.26	-	0.33	-	0.4	V	
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	4	5.5	-	-	±0.1	-	±1	-	±1	μA	
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	4	-	40	-	80	μA	
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 5)	V <sub>CC</sub> - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA	

NOTE:

5. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
All	0.3

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

## CD74HC109, CD74HCT109

### Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Setup Time J, $\bar{K}$ , to CP	t <sub>SU</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Hold Time J, $\bar{K}$ , to CP	t <sub>H</sub>	-	2	5	-	-	5	-	5	-	ns
			4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns
Removal Time $\bar{R}$ , $\bar{S}$ , to CP	t <sub>REM</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Pulse Width CP, $\bar{R}$ , $\bar{S}$	t <sub>W</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
CP Frequency	f <sub>MAX</sub>	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
			6	35	-	-	29	-	23	-	MHz
<b>HCT TYPES</b>											
Setup Time J, $\bar{K}$ to CP	t <sub>SU</sub>	-	4.5	18	-	-	23	-	27	-	ns
Hold Time J, $\bar{K}$ to CP	t <sub>H</sub>	-	4.5	3	-	-	3	-	3	-	ns
Removal Time $\bar{R}$ , $\bar{S}$ , to CP	t <sub>REM</sub>	-	4.5	18	-	-	23	-	27	-	ns
Pulse Width CP, $\bar{R}$ , $\bar{S}$	t <sub>W</sub>	-	4.5	18	-	-	23	-	27	-	ns
CP Frequency	f <sub>MAX</sub>	-	4.5	27	-	-	22	-	18	-	MHz

### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay, CP → Q, $\bar{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	175	-	220	-	265	ns
		C <sub>L</sub> = 50pF	4.5	-	-	35	-	44	-	53	ns
		C <sub>L</sub> = 15pF	5	-	14	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	30	-	37	-	45	ns
Propagation Delay, $\bar{S}$ → Q	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	120	-	150	-	180	ns
		C <sub>L</sub> = 50pF	4.5	-	-	24	-	30	-	36	ns
		C <sub>L</sub> = 15pF	5	-	9	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	20	-	26	-	31	ns
Propagation Delay, $\bar{S}$ → $\bar{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	155	-	195	-	235	ns
		C <sub>L</sub> = 50pF	4.5	-	-	31	-	39	-	47	ns
		C <sub>L</sub> = 15pF	5	-	13	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	26	-	33	-	40	ns

## CD74HC109, CD74HCT109

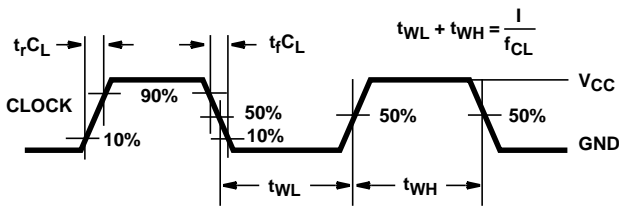
### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, $\bar{R} \rightarrow Q$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	185	-	230	-	280	ns
		$C_L = 50\text{pF}$	4.5	-	-	37	-	46	-	56	ns
		$C_L = 15\text{pF}$	5	-	15	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	31	-	39	-	48	ns
Propagation Delay, $\bar{R} \rightarrow \bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	170	-	215	-	255	ns
		$C_L = 50\text{pF}$	4.5	-	-	34	-	43	-	51	ns
		$C_L = 15\text{pF}$	5	-	14	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	29	-	37	-	43	ns
Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
		$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
		$C_L = 50\text{pF}$	6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
CP Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	5	-	60	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	-	30	-	-	-	-	-	pF
<b>HCT TYPES</b>											
Propagation Delay, $CP \rightarrow Q, \bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
Propagation Delay, $\bar{S} \rightarrow Q$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	30	-	38	-	45	ns
		$C_L = 15\text{pF}$	5	-	12	-	-	-	-	-	ns
Propagation Delay, $\bar{S} \rightarrow \bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	45	-	56	-	68	ns
		$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
Propagation Delay, $\bar{R} \rightarrow Q$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	45	-	56	-	68	ns
		$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
Propagation Delay, $\bar{R} \rightarrow \bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	37	-	46	-	56	ns
		$C_L = 15\text{pF}$	5	-	15	-	-	-	-	-	ns
Transition Time (Figure 5)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
CP Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	5	-	54	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	-	33	-	-	-	-	-	pF

**NOTES:**

6.  $C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.
7.  $P_D = C_{PD} V_{CC}^2 f_i + \sum C_L f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 7. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 8. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

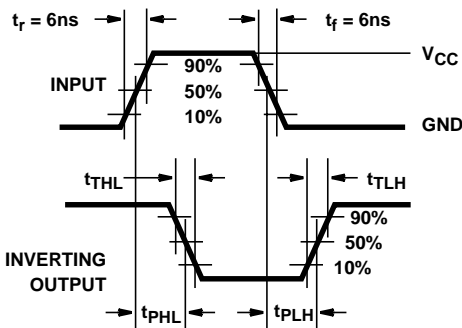


FIGURE 9. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 10. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

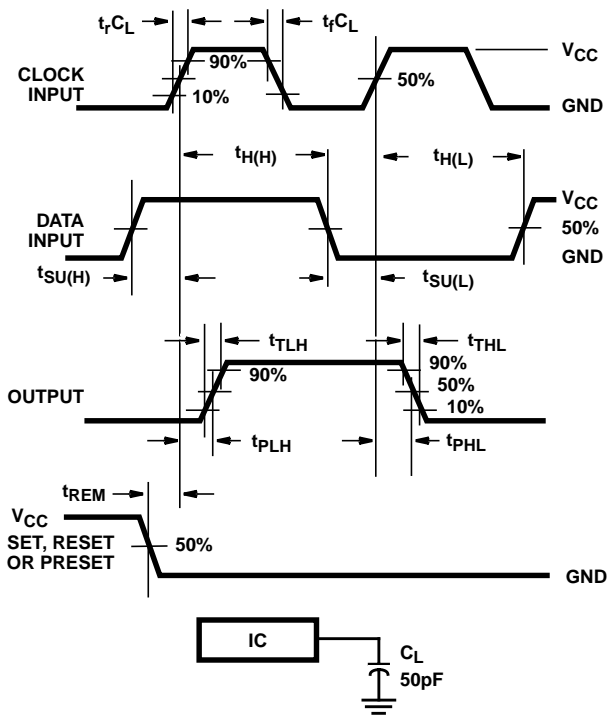


FIGURE 11. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

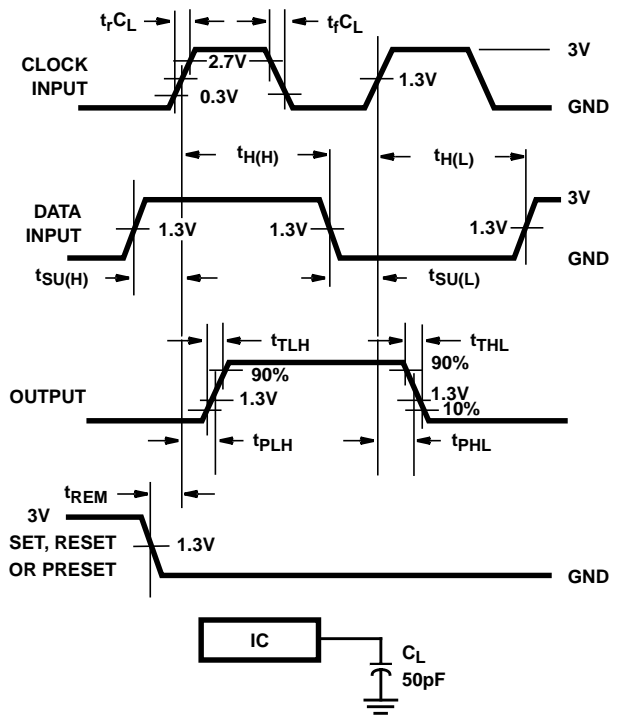


FIGURE 12. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

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