

CD74AC257, CD74ACT257, CD74ACT258

Quad 2-Input Multiplexer with Three-State Outputs

Features

- CD74AC257, CD74ACT257 Non-Inverting Outputs
 - CD74ACT258 Inverting Outputs
 - Buffered Inputs
 - Typical Propagation Delay
 - 4.4ns at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 50pF$
 - Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
 - SCR-Latchup-Resistant CMOS Process and Circuit Design
 - Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
 - Balanced Propagation Delays
 - AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
 - $\pm 24mA$ Output Drive Current
 - Fanout to 15 FAST™ ICs
- Drives 50Ω Transmission Lines

Description

The CD74AC257, CD74ACT257 and CD74ACT258 are quad 2-input multiplexers with three-state outputs that utilize the Harris Advanced CMOS Logic technology. Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable (\overline{OE}) is active LOW. When \overline{OE} is HIGH, all of the outputs (Y or \overline{Y}) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the CD74AC257, CD74ACT257 and CD74ACT258. The state of the Select input determines the particular register from which the data comes. The CD74AC257, CD74ACT257 and CD74ACT258 can also be used as function generators.

Ordering Information

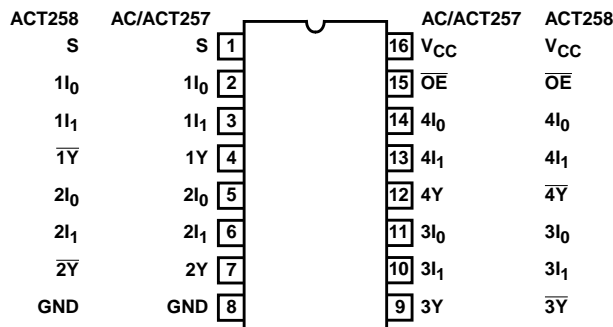
| PART NUMBER | TEMP. RANGE ($^{\circ}C$) | PACKAGE | PKG. NO. |
|-------------|---|------------|----------|
| CD74AC257E | 0 to 70 $^{\circ}C$, -40 to 85, -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74ACT257E | 0 to 70 $^{\circ}C$, -40 to 85, -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74ACT258E | 0 to 70 $^{\circ}C$, -40 to 85, -55 to 125 | 16 Ld PDIP | E16.3 |
| CD74AC257M | 0 to 70 $^{\circ}C$, -40 to 85, -55 to 125 | 16 Ld SOIC | M16.15 |
| CD74ACT257M | 0 to 70 $^{\circ}C$, -40 to 85, -55 to 125 | 16 Ld SOIC | M16.15 |
| CD74ACT258M | 0 to 70 $^{\circ}C$, -40 to 85, -55 to 125 | 16 Ld SOIC | M16.15 |

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

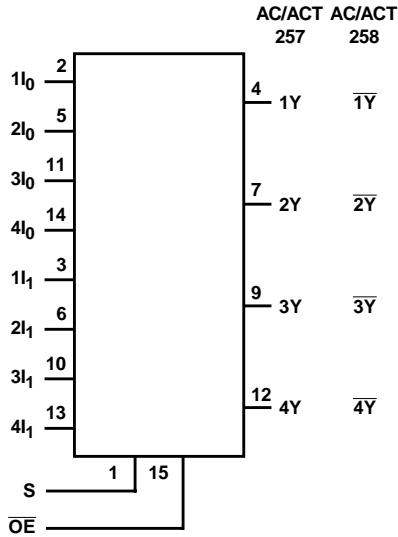
Pinout

CD74AC257, CD74ACT257, CD74ACT258
(PDIP, SOIC)
TOP VIEW



CD74AC257, CD74ACT257, CD74ACT258

Functional Diagram



TRUTH TABLE

| OUTPUT ENABLE | SELECT INPUT | DATA INPUTS | | 257 OUTPUTS | 258 OUTPUTS |
|-----------------|--------------|-------------|-------|-------------|----------------|
| \overline{OE} | S | I_0 | I_1 | Y | \overline{Y} |
| H | X | X | X | Z | Z |
| L | L | L | X | L | H |
| L | L | H | X | H | L |
| L | H | X | L | L | H |
| L | H | X | H | H | L |

H = High level voltage, L = Low level voltage, Z = High impedance (off) state, X = Don't Care

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Absolute Maximum Ratings

| | |
|---|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 6V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 50mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 50mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3) | $\pm 100mA$ |

Thermal Information

| | |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 5) | θ_{JA} ($^{\circ}C/W$) |
| PDIP Package | — |
| SOIC Package | — |
| Maximum Junction Temperature (Plastic Package) | $150^{\circ}C$ |
| Maximum Storage Temperature Range | $-65^{\circ}C$ to $150^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | $300^{\circ}C$ |

Operating Conditions

| | |
|---|----------------------------------|
| Temperature Range, T_A | $-55^{\circ}C$ to $125^{\circ}C$ |
| Supply Voltage Range, V_{CC} (Note 4) | |
| AC Types | 1.5V to 5.5V |
| ACT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I , V_O | 0V to V_{CC} |
| Input Rise and Fall Slew Rate, dt/dv | |
| AC Types, 1.5V to 3V | 50ns (Max) |
| AC Types, 3.6V to 5.5V | 20ns (Max) |
| ACT Types, 4.5V to 5.5V | 10ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25 $^{\circ}C$ | | -40 $^{\circ}C$ TO 85 $^{\circ}C$ | | -55 $^{\circ}C$ TO 125 $^{\circ}C$ | | UNITS |
|---------------------------|----------|----------------------|--------------------|--------------|----------------|------|-----------------------------------|------|------------------------------------|------|-------|
| | | V_I (V) | I_O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| AC TYPES | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 1.5 | 1.2 | - | 1.2 | - | 1.2 | - | V |
| | | | | 3 | 2.1 | - | 2.1 | - | 2.1 | - | V |
| | | | | 5.5 | 3.85 | - | 3.85 | - | 3.85 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 1.5 | - | 0.3 | - | 0.3 | - | 0.3 | V |
| | | | | 3 | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | | | 5.5 | - | 1.65 | - | 1.65 | - | 1.65 | V |
| High Level Output Voltage | V_{OH} | V_{IH} or V_{IL} | -0.05 | 1.5 | 1.4 | - | 1.4 | - | 1.4 | - | V |
| | | | -0.05 | 3 | 2.9 | - | 2.9 | - | 2.9 | - | V |
| | | | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -4 | 3 | 2.58 | - | 2.48 | - | 2.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |

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DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|------------------|---|---------------------|---------------------|------|------|---------------|------|----------------|------|-------|
| | | V _I (V) | I _O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 1.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 3 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 12 | 3 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| ACT TYPES | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | V _{OH} | V _{IH} or V _{IL} | -0.05 | 4.5 | 4.4 | - | 4.4 | - | 4.4 | - | V |
| | | | -24 | 4.5 | 3.94 | - | 3.8 | - | 3.7 | - | V |
| | | | -75 (Note 6, 7) | 5.5 | - | - | 3.85 | - | - | - | V |
| | | | -50 (Note 6, 7) | 5.5 | - | - | - | - | 3.85 | - | V |
| Low Level Output Voltage | V _{OL} | V _{IH} or V _{IL} | 0.05 | 4.5 | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 24 | 4.5 | - | 0.36 | - | 0.44 | - | 0.5 | V |
| | | | 75 (Note 6, 7) | 5.5 | - | - | - | 1.65 | - | - | V |
| | | | 50 (Note 6, 7) | 5.5 | - | - | - | - | - | 1.65 | V |
| Input Leakage Current | I _I | V _{CC} or GND | - | 5.5 | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Three-State or Leakage Current | I _{OZ} | V _{IH} or V _{IL} V _O = V _{CC} or GND | - | 5.5 | - | ±0.5 | - | ±5 | - | ±10 | µA |
| Quiescent Supply Current MSI | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | 8 | - | 80 | - | 160 | µA |
| Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load | ΔI _{CC} | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 2.4 | - | 2.8 | - | 3 | mA |

NOTES:

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

CD74AC257, CD74ACT257, CD74ACT258

ACT Input Load Table

| INPUT | UNIT LOAD |
|-------|-----------|
| Data | 0.83 |
| S | 1.27 |
| OE | 1.27 |

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input $t_r, t_f = 3ns, C_L = 50pF$ (Worst Case)

| PARAMETER | SYMBOL | V _{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|--|--|---------------------|---------------|-----|------|----------------|-----|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| ACT TYPES | | | | | | | | | |
| Propagation Delay, In to Y CD74AC/ACT257 | t _{PLH} , t _{PHL} | 1.5 | - | - | 106 | - | - | 117 | ns |
| | | 3.3 (Note 9) | 3.3 | - | 11.8 | 3.3 | - | 13 | ns |
| | | 5 (Note 10) | 2.4 | - | 8.5 | 2.3 | - | 9.3 | ns |
| Propagation Delay, S to Y CD74AC/ACT257 | t _{PLH} , t _{PHL} | 1.5 | - | - | 153 | - | - | 168 | ns |
| | | 3.3 | 4.8 | - | 17.1 | 4.7 | - | 18.8 | ns |
| | | 5 | 3.5 | - | 12.2 | 3.4 | - | 13.4 | ns |
| Propagation Delay, OE to Y CD74AC/ACT257 | t _{PLZ} , t _{PHZ} , t _{PZL} , t _{PZH} | 1.5 | - | - | 167 | - | - | 184 | ns |
| | | 3.3 | 5.3 | - | 18.7 | 5.2 | - | 20.6 | ns |
| | | 5 | 3.8 | - | 13.4 | 3.7 | - | 14.7 | ns |
| Propagation Delay, In to Y CD74AC/ACT258 | t _{PLH} , t _{PHL} | 1.5 | - | - | 91 | - | - | 100 | ns |
| | | 3.3 | 2.9 | - | 10.2 | 2.8 | - | 11.2 | ns |
| | | 5 | 2.1 | - | 7.3 | 2 | - | 8 | ns |
| Propagation Delay, S to Y CD74AC/ACT258 | t _{PLH} , t _{PHL} | 1.5 | - | - | 153 | - | - | 168 | ns |
| | | 3.3 | 4.8 | - | 17.1 | 4.7 | - | 18.8 | ns |
| | | 5 | 3.5 | - | 12.2 | 3.4 | - | 13.4 | ns |
| Propagation Delay, OE to Y CD74AC/ACT258 | t _{PLZ} , t _{PHZ} , t _{PZL} , t _{PZH} | 1.5 | - | - | 167 | - | - | 184 | ns |
| | | 3.3 | 5.3 | - | 18.7 | 5.2 | - | 20.6 | ns |
| | | 5 | 3.8 | - | 13.4 | 3.7 | - | 14.7 | ns |
| Three-State Output Capacitance | C _O | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | C _I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C _{PD} (Note 11) | - | - | 130 | - | - | 130 | - | pF |
| ACT TYPES | | | | | | | | | |
| Propagation Delay, In to Y CD74AC/ACT257 | t _{PLH} , t _{PHL} | 5 (Note 10) | 2.8 | - | 9.7 | 2.7 | - | 10.7 | ns |
| Propagation Delay, S to Y CD74AC/ACT257 | t _{PLH} , t _{PHL} | 5 | 4 | - | 14 | 3.9 | - | 15.4 | ns |

CD74AC257, CD74ACT257, CD74ACT258

Switching Specifications Input $t_r, t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case) (Continued)

| PARAMETER | SYMBOL | V_{CC} (V) | -40°C TO 85°C | | | -55°C TO 125°C | | | UNITS |
|---|--------------------------------------|--------------|---------------|-----|------|----------------|-----|------|-------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Propagation Delay, \overline{OE} to Y CD74AC/ACT257 | $t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}$ | 5 | 4.1 | - | 14.6 | 4 | - | 16.1 | ns |
| Propagation Delay, In to \overline{Y} CD74AC/ACT258 | t_{PLH}, t_{PHL} | 5 | 2.4 | - | 8.5 | 2.3 | - | 9.3 | ns |
| Propagation Delay, S to \overline{Y} CD74AC/ACT258 | t_{PLH}, t_{PHL} | 5 | 4 | - | 14 | 3.9 | - | 15.4 | ns |
| Propagation Delay, \overline{OE} to \overline{Y} CD74AC/ACT258 | $t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}$ | 5 | 4.1 | - | 14.6 | 4 | - | 16.1 | ns |
| Three-State Output Capacitance | C_O | - | - | - | 15 | - | - | 15 | pF |
| Input Capacitance | C_I | - | - | - | 10 | - | - | 10 | pF |
| Power Dissipation Capacitance | C_{PD} (Note 11) | - | - | 130 | - | - | 130 | - | pF |

NOTES:

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per multiplexer.
 AC: $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$
 ACT: $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

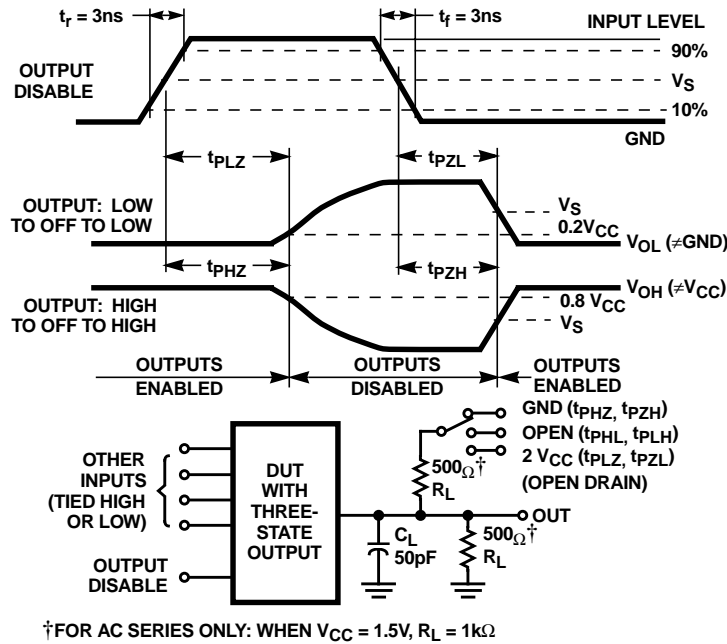


FIGURE 1. THREE-STATE PROPAGATION DELAY TIMES AND TEST CIRCUIT

CD74AC257, CD74ACT257, CD74ACT258

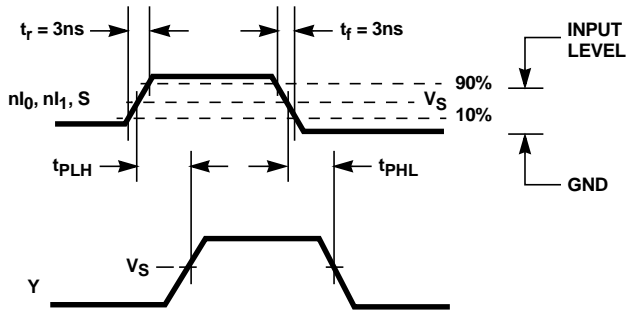


FIGURE 2. INPUTS OR SELECT TO OUTPUT PROPAGATION DELAYS (AC/ACT257)

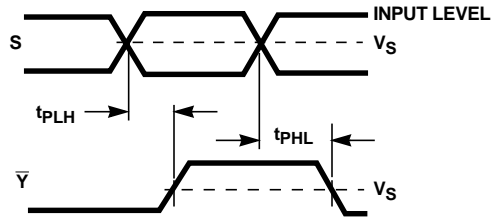
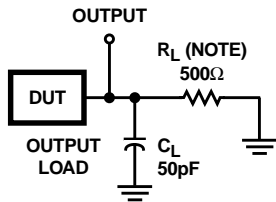


FIGURE 3. SELECT TO OUTPUT PROPAGATION DELAYS (ACT258)



NOTE: For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

| | CD74AC | CD74ACT |
|---------------------------------|--------------|--------------|
| Input Level | V_{CC} | 3V |
| Input Switching Voltage, V_S | $0.5 V_{CC}$ | 1.5V |
| Output Switching Voltage, V_S | $0.5 V_{CC}$ | $0.5 V_{CC}$ |

FIGURE 4. PROPAGATION DELAY TIMES

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