VOLTAGE PROTECTION FOR 2-, 3-, OR 4-CELL Li-Ion BATTERIES (2nd-LEVEL PROTECTION)

FEATURES

- **2-, 3-, or 4-Cell Secondary Protection**
- **Low Power Consumption I_{CC} < 2 µA [$VCELL_{(ALL)}$ < $V_{(PROTECT)}$]**
- **Fixed High Accuracy Overvoltage Protection Threshold**
  - **bq29410 = 4.35 V**
  - **bq29411 = 4.40 V**
  - **bq29412 = 4.45 V**
- **Programmable Delay Time of Detection**
- **High Power Supply Ripple Rejection**
- **Stable During Pulse Charge Operation**

APPLICATIONS

- **2nd-Level Overvoltage Protection in Li-Ion Battery Packs in:**
  - **Notebook Computers**
  - **Portable Instrumentation**
  - **Portable Equipment**

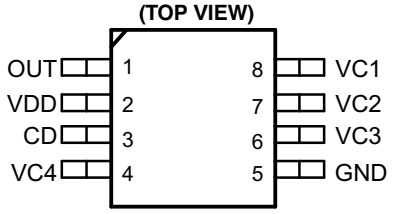
DESCRIPTION

The bq2941x is a secondary overvoltage protection IC for 2-, 3-, or 4-cell lithium-ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit. It includes a programmable delay circuit for overvoltage detection time.

FUNCTION

Each cell in a multiple-cell pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq2941x device starts charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes from a low level to a high level.

DCT PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

ORDERING INFORMATION(1)

T_A	$V_{(PROTECT)}$(2)	PACKAGE(3)			
		MSOP (DCT3)	SYMBOL	PW	
–40°C to 110°C	4.35 V	bq29410DCT3R	CJG	bq29410PW	bq29410PWR
	4.40 V	bq29411DCT3R	CJH	bq29411PW	bq29411PWR
	4.45 V	bq29412DCT3R	CJJ	bq29412PW	bq29412PWR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Contact your local Texas Instruments representative or sales office for alternative overvoltage threshold options.
(3) The "R" suffix indicates tape-and-reel packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

		UNIT
Supply voltage range	VDD	–0.3 V to 28 V
Input voltage range	VC1, VC2, VC3, VC4	–0.3 V to 28 V
	VC1 TO VC2, VC2 TO VC3, VC3 TO VC4, VC4 TO GND	–0.3 V to 8 V
Output voltage range	OUT	–0.3 V to 28 V
	CD	–0.3 V to 28 V
Continuous total power dissipation		See Dissipation Rating Table
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature (soldering, 10 s)		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground of this device except the differential voltage of VC1-VC2, VC2-VC3, VC3-VC4, and VC4-GND.

PACKAGE DISSIPATION RATINGS

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCT	412 mW	3.3 mW/°C	264 mW	214 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4		25	V
V_I	Input voltage range	VC1, VC2, VC3, VC4	0		V_{DD}	V
		VCn – VC (n=1), (n=1, 2, 3), VC4 – GND	0		5	
$t_{d(CD)}$	Delay time capacitance			0.22		µF
R_{IN}	Voltage-monitor filter resistance		100	1k		Ω
C_{IN}	Voltage-monitor filter capacitance		0.01	0.1		µF
R_{VD}	Supply-voltage filter resistance		0		1	kΩ
C_{VD}	Supply-voltage filter capacitance			0.1		µF
T_A	Operating ambient temperature range		–40		110	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{(OA)}$	Overvoltage detection accuracy	T_A = 25°C		25	35	mV
		T_A = –20°C to 85°C		25	50	
		T_A = –40°C to 110°C			80	
$V_{(PROTECT)}$	Overvoltage detection voltage(1)	bq29410		4.35		V
		bq29411		4.40		
		bq29412		4.45		
V_{hys}	Overvoltage detection hysteresis(1)			300		mV
I_{IN}	Input current	V2, V3 , VC4 input ,V_{DD} = VC1 VC1 = VC2 = VC3 = VC4 = 3.5 V (see Figure 1)			0.3	µA
t_{D1}	Overvoltage detection delay time	V_{DD} = VC1, CD = 0.22 µF	1	1.5	2	S
$I_{(CD\_dis)}$	CD GND clamp current	V_{DD} = VC1, CD = 1 V	5	12		µA
I_{CC}	Supply current	V_{DD} = VC1, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V (see Figure 1)		2	3	µA
		V_{DD} = VC1, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 2.3 V (see Figure 1)		1.5	2.5	
I_{OH}	High-level output current	OUT = 3 V, V_{DD} = VC1, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 4.5 V	–1			mA
I_{OL}	Low-level output current	OUT = 0.1 V, V_{DD} = VC1, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V	5			µA

(1) Levels of the overvoltage detection and the hysteresis can be adjusted. For assistance, contact a Texas Instruments sales representative.

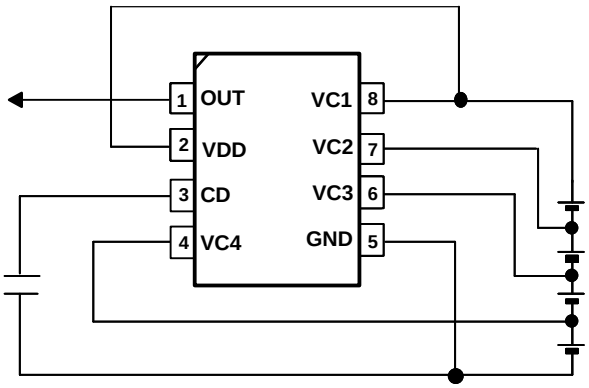
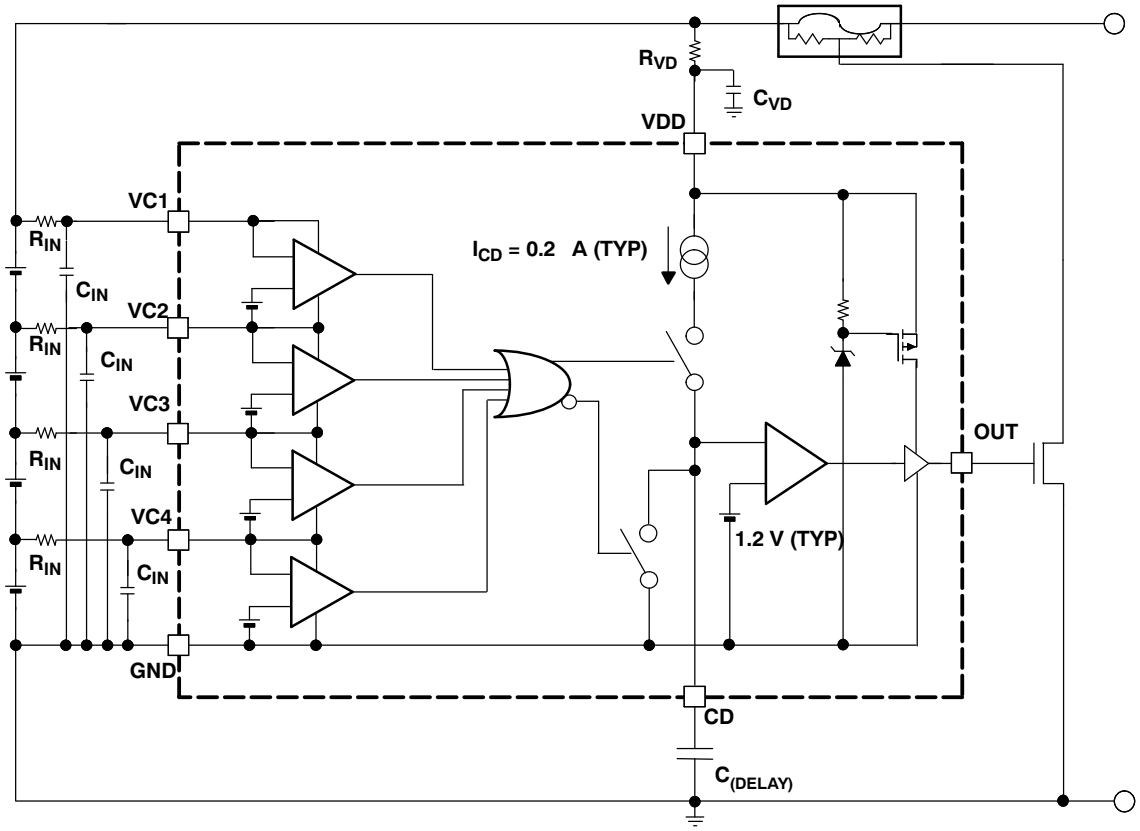


Figure 1. I_{CC}, I_{IN} Measurement (DCT Package)

Terminal Functions

TERMINAL			DESCRIPTION
MSOP (DCT)	TSSOP (PW)	NAME	
8	1	VC1	Sense voltage input for most positive cell
7	2	VC2	Sense voltage input for second most positive cell
6	3	VC3	Sense voltage input for third most positive cell
5	4	GND	Ground pin
4	5	VC4	Sense voltage input for least positive cell
3	6	CD	An external capacitor is connected to determine the programmable delay time
2	7	VDD	Power supply
1	8	OUT	Output

FUNCTIONAL BLOCK DIAGRAM



OVERVOLTAGE PROTECTION

When one of the cell voltages exceeds $V_{(PROTECT)}$, an internal current source begins to charge the capacitor, $C_{(DELAY)}$, connected to the CD pin. If the voltage at the CD pin, $V_{CD,}$ reaches 1.2 V, the OUT pin is activated and transitions high. An externally connected NCH FET is activiated and blows the external fuse in the positive battery rail; see the functional block diagram.

If all cell voltages fall below $V_{(PROTECT)}$ before the voltage at pin CD reaches 1.2 V, the delay time does not run out. An internal switch clamps the CD pin to GND and discharges the capacitor, $C_{(DELAY)}$, and secures the full delay time for the next occurring overvoltage event.

Once the pin OUT is activated, it transitions back from high to low after all battery cells reach $V_{(PROTECT)} - V_{hys.}$

DELAY TIME CALCULATION

The delay time is calculated as follows:

$$t_d = \frac{\left[1.2\ V \times C_{(DELAY)}\right]}{I_{CD}}$$

$$C_{(DELAY)} = \frac{\left[t_d \times I_{CD}\right]}{1.2\ V}$$

Where $I_{(CD)}$ = CD current source = 0.18 µA

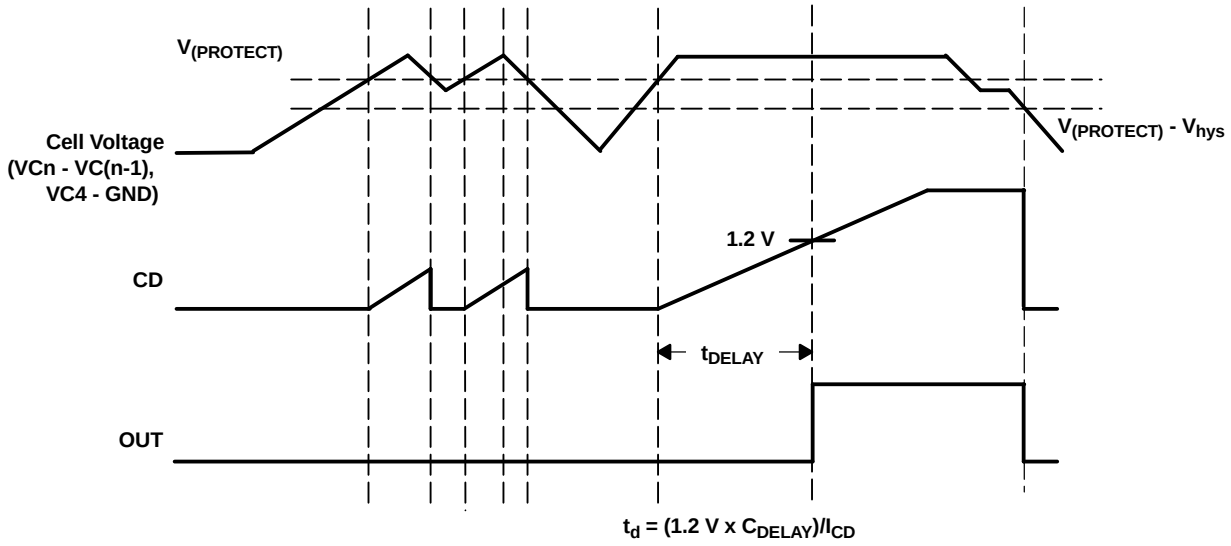


Figure 2. Timing for Overvoltage Sensing

APPLICATION INFORMATION

BATTERY CONNECTIONS

The following diagrams show the DCT package device in different cell configurations.

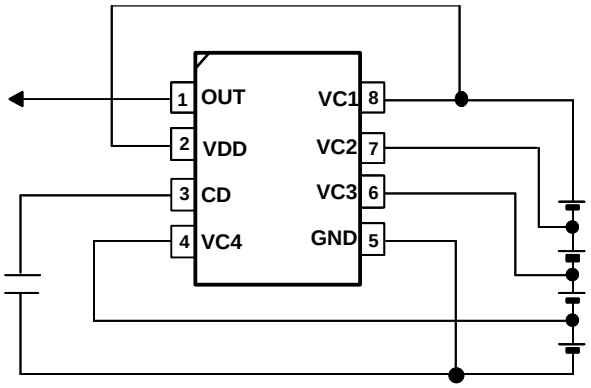


Figure 3. 4-Series Cell Configuration

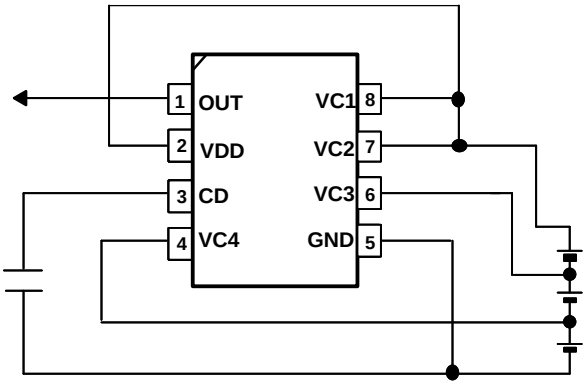


Figure 4. 3-Series Cell Configuration (Connect together VC1 and VC2)

APPLICATION INFORMATION (continued)

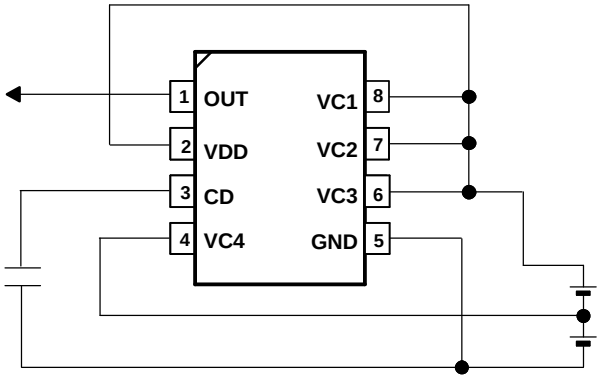


Figure 5. 2-Series Cell Configuration

CELL CONNECTIONS

To prevent incorrect output activation, the following connection sequences must be used.

4-Series Cell Configuration

- VC1(=VDD) → VC2 → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC2 → VC1(=VDD)

3-Series Cell Configuration

- VC1(=VC2=VDD) → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC1(=VC2=VDD)

2-Series Cell Configuration

- VC1(=VC2=VC3=VDD) → VC4 → GND or
- GND → VC4 → VC1(=VC2=VC3=VDD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ29412DCT3R	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-250C-UNLIM

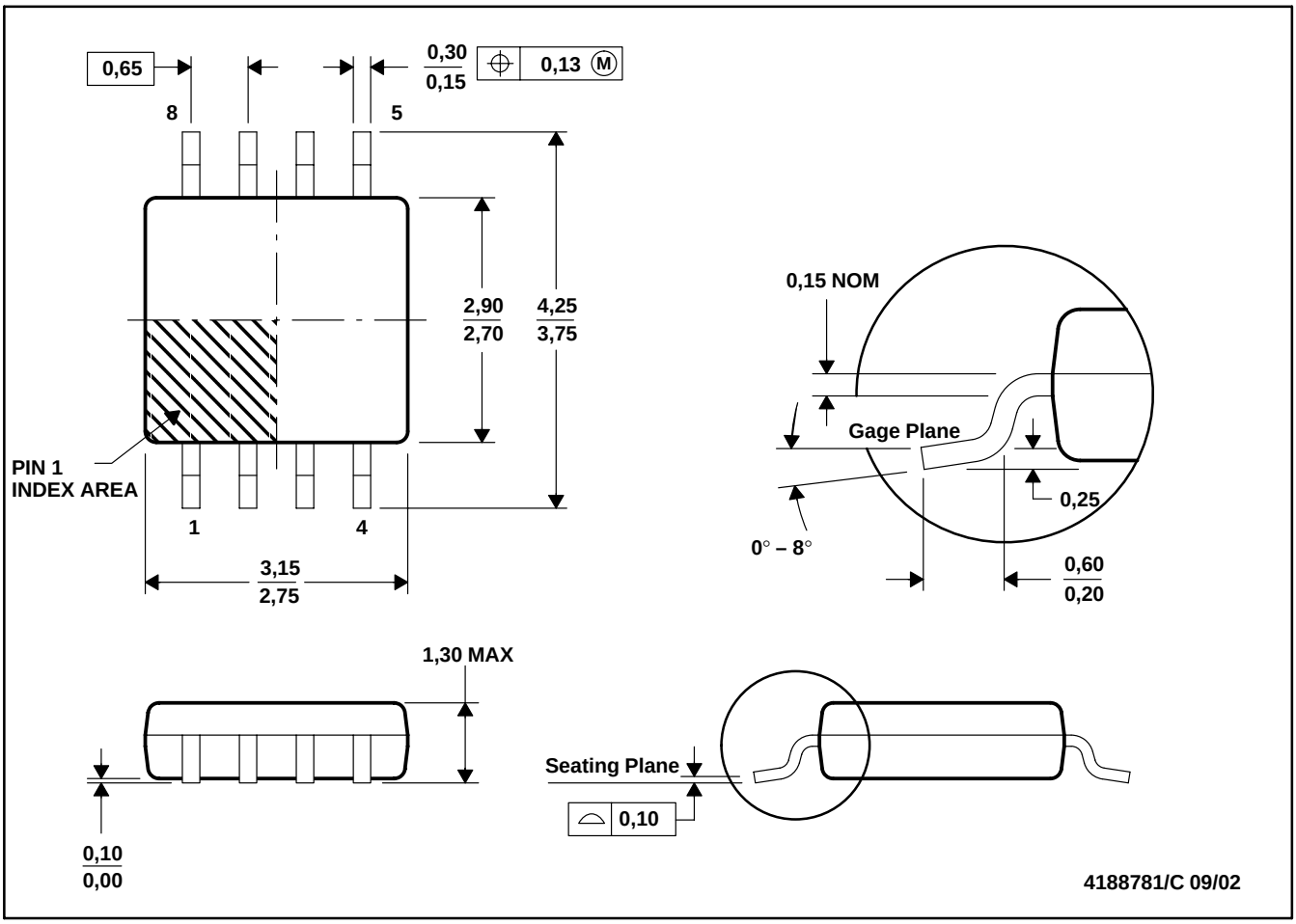
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MPDS049B – MAY 1999 – REVISED OCTOBER 2002

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

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