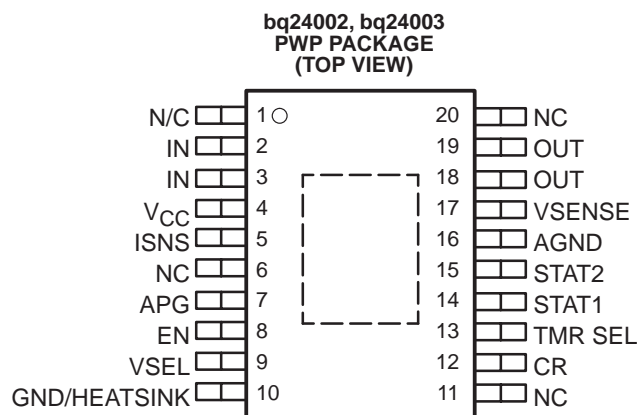
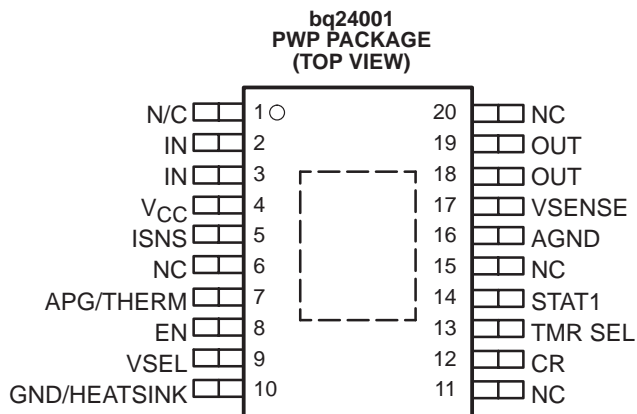


- **Highly Integrated Solution With FET Pass Transistor and Reverse-Blocking Schottky and thermal Protection**
- **Integrated Voltage and Current Regulation with Programmable Charge Current**
- **High Accuracy Voltage Regulation ( $\pm 1\%$ )**
- **Ideal for Linear Charger Designs for Single-Cell Li-Ion Packs With Coke or Graphite Anodes**
- **Up to 1.2-A Continuous Charge Current With Low Dropout Voltage**
- **Safety-Charge Timer During Preconditioning and Fast Charge**
- **Integrated Cell Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage of Charge**
- **Optional Temperature or Input-Power Monitoring Before and During Charge**
- **Various Charge-Status Output Options for Driving Single, Double, or Bicolor LEDs or Host-Processor Interface**
- **Charge Termination By Minimum Current and Time**
- **Low-Power Sleep Mode**
- **Packaging: 20-Lead TSSOP PowerPAD**



## description

The bq2400x series ICs are advanced Li-Ion linear charge management devices for highly integrated and space-limited applications. They combine high-accuracy current and voltage regulation, FET pass-transistor and reverse-blocking Schottky, battery conditioning, temperature, or input-power monitoring, charge termination, charge-status indication, and charge timer in a small, 20-lead TSSOP PowerPAD package.

The bq2400x continuously measures battery temperature using an external thermistor. For safety reasons, the bq2400x inhibits charge until the battery temperature is within the user-defined thresholds. Alternatively, the user can monitor the input voltage to qualify charge. The bq2400x series then charge the battery in three phases: preconditioning, constant current, and constant voltage. If the battery voltage is below the internal low-voltage threshold, the bq2400x uses trickle-charge to condition the battery. A preconditioning timer is provided for additional safety. Following preconditioning, the bq2400x applies a constant-charge current to the battery. An external sense-resistor sets the magnitude of the current. The constant-current phase is maintained until the battery reaches the charge-regulation voltage. The bq2400x then transitions to the constant voltage phase. The user can configure the device for cells with either coke or graphite anodes. The accuracy of the voltage regulation is better than  $\pm 1\%$  over the operating junction temperature and supply voltage range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS**  
**INSTRUMENTS**

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**bq24001, bq24002, bq24003**  
**SINGLE-CELL ADVANCED LINEAR LI-ION CHARGE**  
**MANAGEMENT IC WITH INTEGRATED POWER FET**

SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

**description (continued)**

Charge is terminated by either of the following methods:

- Maximum time
- Minimum current detection

The bq2400x automatically restarts the charge if the battery voltage falls below an internal recharge threshold.

As shown in the following table, the bq2400x series ICs are available in 3 charge-status configuration options.

**AVAILABLE OPTIONS**

T <sub>J</sub>	PACKAGE	Charge Status Configuration
	20-Pin HTTSOP PowerPAD™ (PWP)	
-40°C to 125°C	bq24001	Single LED
	bq24002	2 LEDs
	bq24003	Bicolor LED

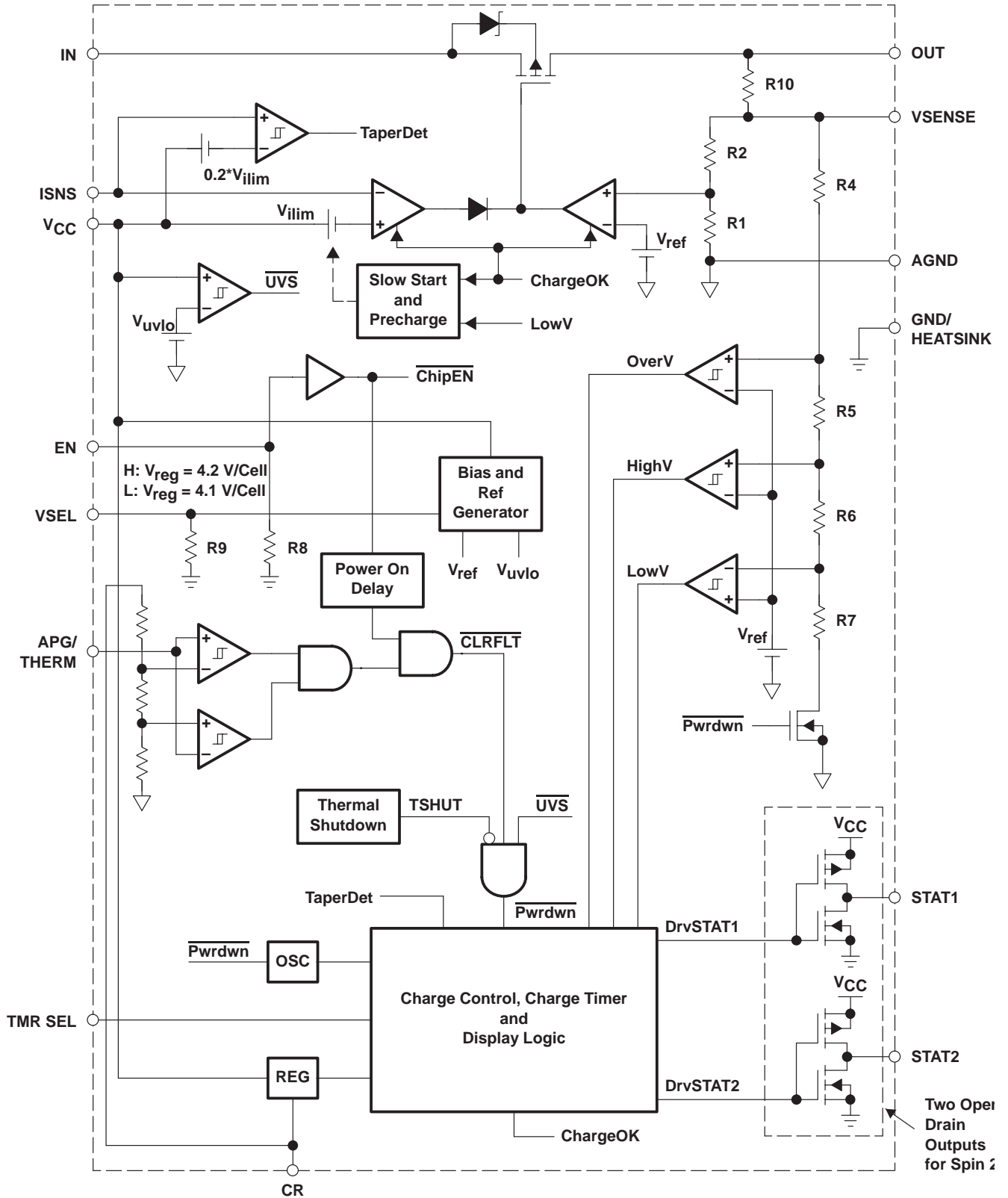
**Terminal Functions**

TERMINAL		I/O	DESCRIPTION
NAME	No.		
AGND	16		Ground pin; connect close to the negative battery terminal for remote sensing.
APG/THERM	7	I	Adapter power good input/Thermistor sense
CR	12	I	Internal regulator bypass capacitor
EN	8	I	Active-high enable input with internal pull down. Low-Iq stand-by mode active when EN is low.
GND/HEATSINK	10		Ground pin, connect to PowerPAD heat-sink layout pattern
IN	2,3	I	Input voltage
ISNS	5	I	Current sense input
NC	1,6,11 15,20		No connect
OUT	18,19	O	Charge current output
STAT1	14	O	Display output 1
STAT2	15	O	Display output 2 (for bq24002 and bq24003 only)
TMR SEL	13	I	User selectable total charge timer
VCC	4	I	Supply voltage
VSEL	9	I	Voltage INPUT 2–4.1-V or 4.2 V regulation options
VSENSE	17	I	Remote voltage sense input regulation



bq24001, bq24002, bq24003  
**SINGLE-CELL ADVANCED LINEAR LI-ION CHARGE  
 MANAGEMENT IC WITH INTEGRATED POWER FET**  
 SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

functional block diagram



**bq24001, bq24002, bq24003**  
**SINGLE-CELL ADVANCED LINEAR LI-ION CHARGE**  
**MANAGEMENT IC WITH INTEGRATED POWER FET**

SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage (V <sub>CC</sub> with respect to GND)	13.5 V
Input voltage (IN, ISNS, EN, APG/THERM/CR/STAT1/STAT2, VSENSE, TMR SEL, VSEL) (all with respect to GND)	13.5 V
Output current (OUT pins)	2 A
Output sink/source current (STAT1 and STAT2)	10 mA
Operating free-air temperature range, T <sub>A</sub>	–20°C to 70°C
Storage temperature range, T <sub>stg</sub>	– 65°C to 150°C
Junction temperature range, T <sub>J</sub>	– 40°C to 125°C
Lead temperature (Soldering, 10 sec)	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURE (SEE FIGURE 1)‡**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
PWP§	700 mW	5.6 mW/°C	448 mW	140 mW

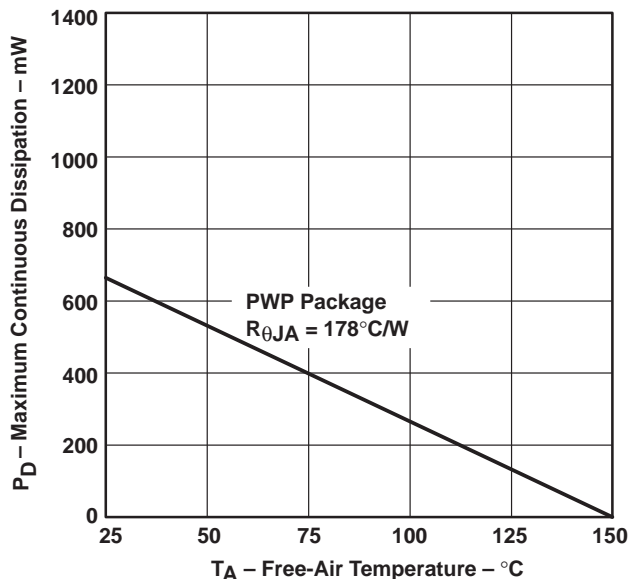
**DISSIPATION RATING TABLE 2 – CASE TEMPERATURE (SEE FIGURE 2)‡**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
PWP§	25 W	285.7 mW/°C	22.9 W	7.1 W

‡ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junctions temperature within recommended operating range, see the *thermal information* section.

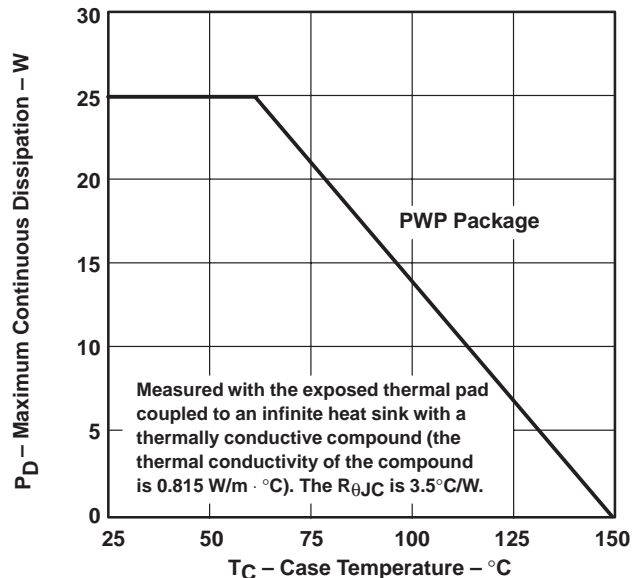
§ Refer to the *thermal information* section for detailed power dissipation considerations when using the TSSOP packages.

**DISSIPATION DERATING CURVE†**  
**vs**  
**FREE-AIR TEMPERATURE**



**Figure 1**

**MAXIMUM CONTINUOUS DISSIPATION†**  
**vs**  
**CASE TEMPERATURE**



**Figure 2**

† Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

bq24001, bq24002, bq24003  
**SINGLE-CELL ADVANCED LINEAR LI-ION CHARGE  
MANAGEMENT IC WITH INTEGRATED POWER FET**  
SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

**recommended operating conditions**

	MIN	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.5	10	V
Input voltage, V <sub>IN</sub>	4.5	10	V
Continuous output current		1.2	A
Operating junction temperature range, T <sub>J</sub>	-40	125	°C

**electrical characteristic over recommended operating junction temperature, supply and input voltages, and V<sub>I</sub> (V<sub>CC</sub>) ≥ V<sub>I</sub> (I<sub>N</sub>) (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>VCC1</sub>	V <sub>CC</sub> current	V <sub>CC</sub> > V <sub>CC_UVLO</sub> , EN ≤ V <sub>IH</sub> (EN)			1	mA
I <sub>VCC2</sub>	V <sub>CC</sub> current, standby-mode	EN ≤ V <sub>IL</sub> (EN)		1		μA
I <sub>IN</sub>	I <sub>N</sub> current, standby mode	EN ≤ V <sub>IL</sub> (EN)			10	μA
I <sub>stby1</sub>	Standby current (sum of currents into OUT and VSENSE pins)	V <sub>CC</sub> < V <sub>CC_UVLO</sub> , V <sub>OUT</sub> = 4.3 V, VSENSE = 4.3 V		2	4	μA
		EN ≤ V <sub>IL</sub> (EN), V <sub>OUT</sub> = 4.3 V, VSENSE = 4.3 V		2	4	

**voltage regulation, 0°C ≤ T<sub>J</sub> ≤ 125°C**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage		VSEL = V <sub>SS</sub> , 0 < I <sub>O</sub> ≤ 1.2 A	4.059	4.10	4.141	V
Output voltage		VSEL = V <sub>CC</sub> , 0 < I <sub>O</sub> ≤ 1.2 A	4.158	4.20	4.242	V
Load regulation		1 mA ≤ I <sub>O</sub> ≤ 1.2 A, V <sub>I</sub> (I <sub>N</sub> ) = 5 V, V <sub>CC</sub> = 5 V, T <sub>J</sub> = 25°C		1		mV
Line regulation		V <sub>OUT</sub> + V <sub>DO</sub> + V <sub>ilim</sub> (MAX) < V <sub>I</sub> (V <sub>CC</sub> ) < 10 V, T <sub>J</sub> = 25°C		0.01		%/V
Dropout voltage = V <sub>I</sub> (I <sub>N</sub> ) - V <sub>out</sub>		I <sub>O</sub> = 1.0 A, 4.9 V < V <sub>I</sub> (V <sub>CC</sub> ) < 10 V			0.7	V
Dropout voltage = V <sub>I</sub> (I <sub>N</sub> ) - V <sub>out</sub>		I <sub>O</sub> = 1.2 A, V <sub>OUT</sub> + V <sub>DO</sub> + V <sub>ilim</sub> MAX < V <sub>I</sub> (V <sub>CC</sub> ) < 10 V,			0.8	V

**current regulation, 0°C ≥ T<sub>J</sub> ≥ 125°C**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current regulation threshold		VSENSE < V <sub>O</sub> (VSEL-LOW/HIGH)	0.095	0.1	0.105	V
Delay time		VSENSE pulsed above V <sub>VLOWV</sub> to I <sub>O</sub> = 10% of regulated value, See Note 1			1	ms
Rise time		I <sub>O</sub> increasing from 10% to 90% of regulated value. R <sub>ilim</sub> ≥ 0.2 Ω, , See Note 1	0.1		1	ms

NOTE 1: Assured by design, not production tested.

**current sense resistor, 0°C ≥ T<sub>J</sub> ≥ 125°C**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current sense resistor range		100 mA ≤ I <sub>lim</sub> ≤ 1.2A	0.083		1	Ω

**precharge current regulation, 0°C ≥ T<sub>J</sub> ≥ 125°C**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Precharge current regulation		VSENSE < V <sub>LOWV</sub> , 0.083 ≤ R <sub>ilim</sub> ≤ 1.0 Ω	40	60	80	mA



**bq24001, bq24002, bq24003**  
**SINGLE-CELL ADVANCED LINEAR LI-ION CHARGE**  
**MANAGEMENT IC WITH INTEGRATED POWER FET**

SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

**electrical characteristic over recommended operating junction temperature, supply and input voltages, and  $V_I (V_{CC}) \geq V_I (IN)$  (unless otherwise noted) (continued)**

**$V_{CC}$  UVLO comparator,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		4.35	4.43	4.50	V
Stop threshold		4.25	4.33	4.40	V
Hysteresis		50			mV

**APG/THERM comparator,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Upper trip threshold		1.480	1.498	1.515	V
Lower trip threshold		0.545	0.558	0.570	V
Input bias current				1	$\mu\text{A}$

**lowv comparator,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		2.80	2.90	3.00	V
Stop threshold		3.00	3.10	3.20	V
Hysteresis		100			mV

**highv comparator,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		3.80	3.90	4.00	V

**overv comparator,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		4.35	4.45	4.55	V
Stop threshold		4.25	4.30	4.35	V
Hysteresis		50			mV

**taperdet comparator,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Trip threshold		12	18.5	25	mV

**EN logic input,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	$\text{k}\Omega$

**VSEL logic input,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	$\text{k}\Omega$



**bq24001, bq24002, bq24003**  
**SINGLE-CELL ADVANCED LINEAR LI-ION CHARGE**  
**MANAGEMENT IC WITH INTEGRATED POWER FET**

SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

**electrical characteristic over recommended operating junction temperature, supply and input voltages, and  $V_I (V_{CC}) \geq V_I (IN)$  (unless otherwise noted) (continued)**

**TMR SEL input,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.7			V
Low-level input voltage				0.6	V
Input bias current	$V_I(\text{TMR SEL}) \leq 5\text{V}$			15	$\mu\text{A}$

**STAT1, STAT2 (bq24001, bq24003),  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output (low) saturation voltage	$I_O = 10\text{ mA}$			1.5	V
Output (low) saturation voltage	$I_O = 4\text{ mA}$			0.6	V
Output (high) saturation voltage	$I_O = -10\text{ mA}$	$V_{CC}-1.5$			V
Output (high) saturation voltage	$I_O = -4\text{ mA}$	$V_{CC}-0.5$			V
Output turn on/off time	$I_O = \pm 10\text{ mA}$ , $C = 100\text{ pF}$ , See Note 1			100	$\mu\text{s}$

NOTE 1. Assured by design, not production tested.

**power-on reset (POR),  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POR delay	See Note 1	1.2		3	ms
POR falling-edge deglitch	See Note 1	25		75	$\mu\text{s}$

NOTE 1. Assured by design, not production tested.

**APG/THERM delay,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
APG/THERM falling-edge deglitch	See Note 1	25		75	$\mu\text{s}$

NOTE 1. Assured by design, not production tested.

**timers,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
User-selectable timer accuracy	$T_A = 25^\circ\text{C}$	-15%		15%	
		-20%		20%	
Precharge and taper timer			22.5		minute

**thermal shutdown,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal trip	See Note 1		165		$^\circ\text{C}$
Thermal hysteresis	See Note 1		10		$^\circ\text{C}$

NOTE 1. Assured by design, not production tested.

**CR pin,  $0^\circ\text{C} \geq T_J \geq 125^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	$0 < I_O(\text{CR}) < 100\ \mu\text{A}$	2.816	2.85	2.88	V



# bq24001, bq24002, bq24003 SINGLE-CELL ADVANCED LINEAR Li-ION CHARGE MANAGEMENT IC WITH INTEGRATED POWER FET

SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

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## detailed description

### power FET

The integrated transistor is a P-channel MOSFET. The power FET features a reverse-blocking Schottky diode, which prevents current flow from OUT to IN.

An internal thermal-sense circuit shuts off the power FET when the junction temperature rises to approximately 165°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 10°C, the power FET turns back on. The power FET continues to cycle off and on until the fault is removed.

### current sense

The bq2400x regulates current by sensing, on the ISNS pin, the voltage drop developed across an external sense resistor. The sense resistor must be placed between the supply voltage (Vcc) and the input of the IC (IN pins).

### voltage sense

To achieve maximum voltage regulation accuracy, the bq2400x uses the feedback on the VSENSE pin. Externally, this pin should be connected as close to the battery cell terminals as possible. For additional safety, a 10kΩ internal pullup resistor is connected between the VSENSE and OUT pins.

### enable (EN)

The logic EN input is used to enable or disable the IC. A high-level signal on this pin enables the bq2400x. A low-level signal disables the IC and places the device in a low-power standby mode.



TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE  
 vs  
 OUTPUT CURRENT

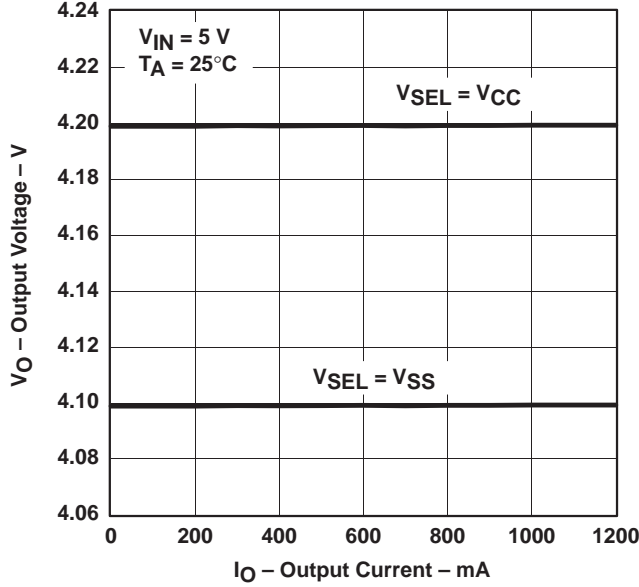


Figure 3

OUTPUT VOLTAGE  
 vs  
 JUNCTION TEMPERATURE

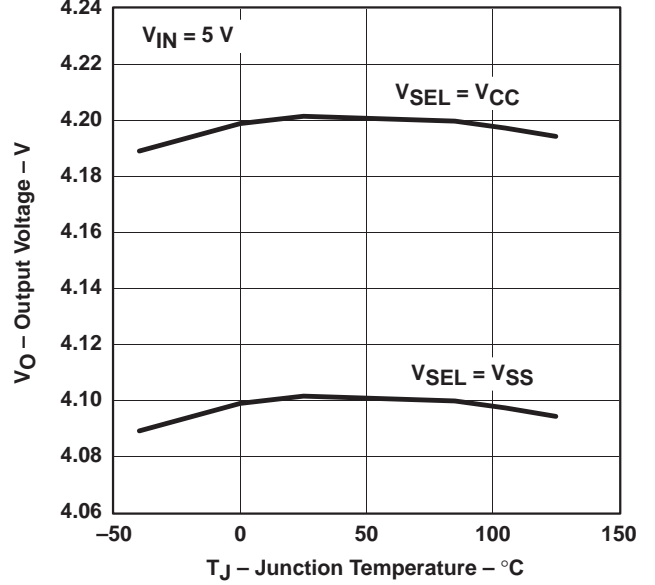


Figure 4

OUTPUT VOLTAGE  
 vs  
 INPUT VOLTAGE

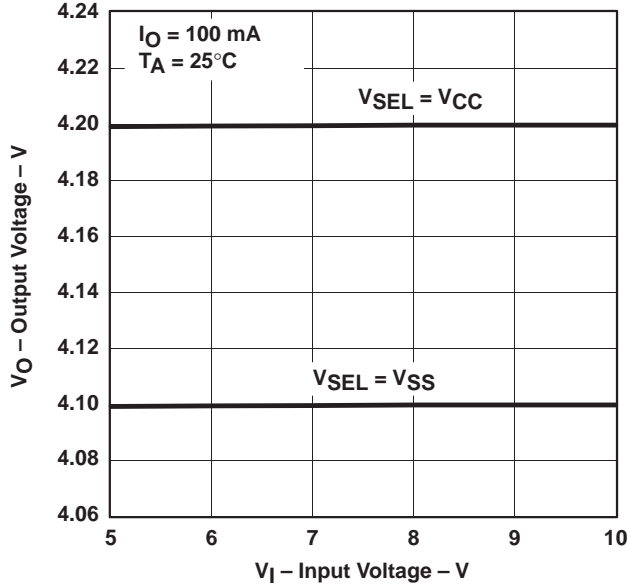


Figure 5

CURRENT SENSE VOLTAGE  
 vs  
 INPUT VOLTAGE

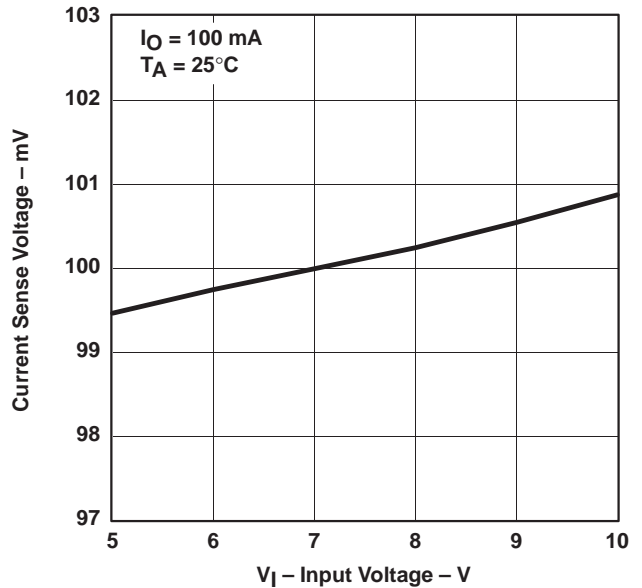
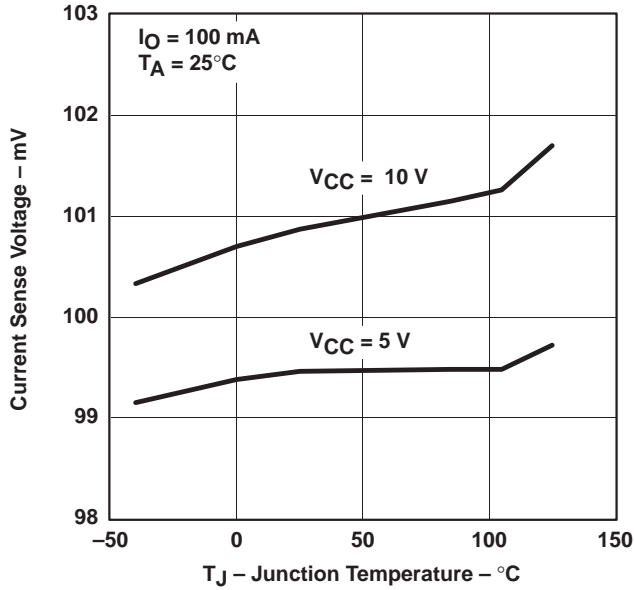


Figure 6

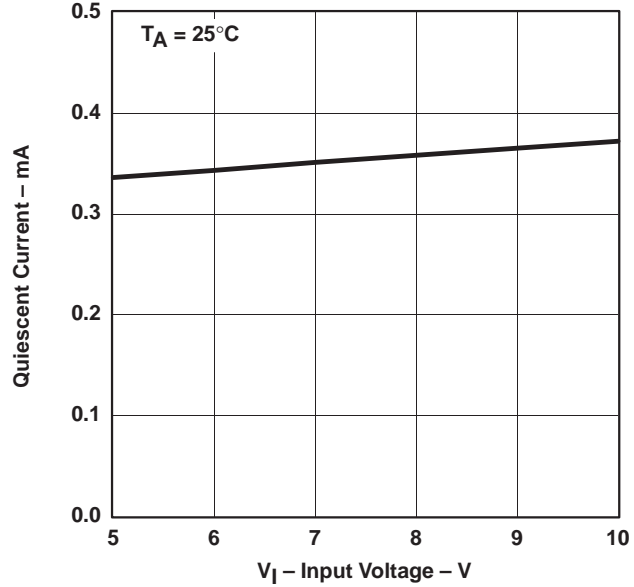
**TYPICAL CHARACTERISTICS**

**CURRENT SENSE VOLTAGE  
 vs  
 JUNCTION TEMPERATURE**



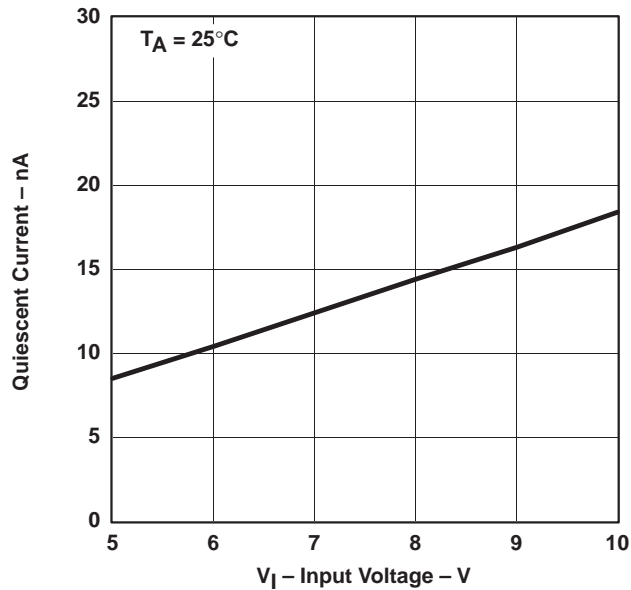
**Figure 7**

**QUIESCENT CURRENT  
 vs  
 INPUT VOLTAGE**



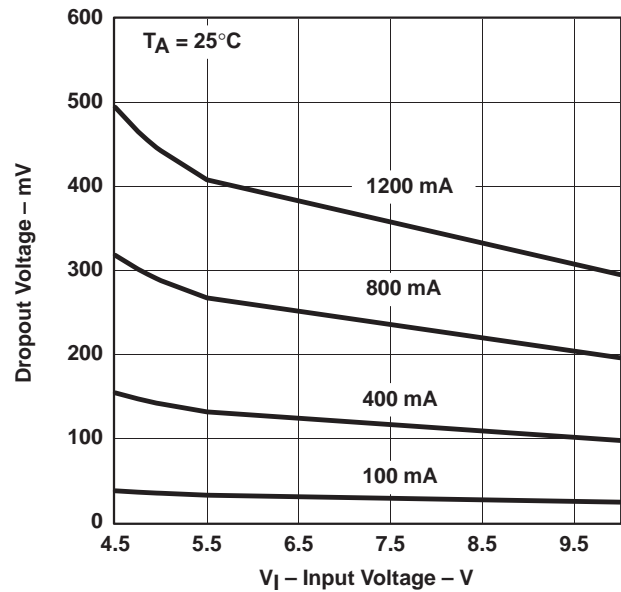
**Figure 8**

**QUIESCENT CURRENT  
 (POWER DOWN)  
 vs  
 INPUT VOLTAGE**



**Figure 9**

**DROPOUT VOLTAGE  
 vs  
 INPUT VOLTAGE**



**Figure 10**

TYPICAL CHARACTERISTICS

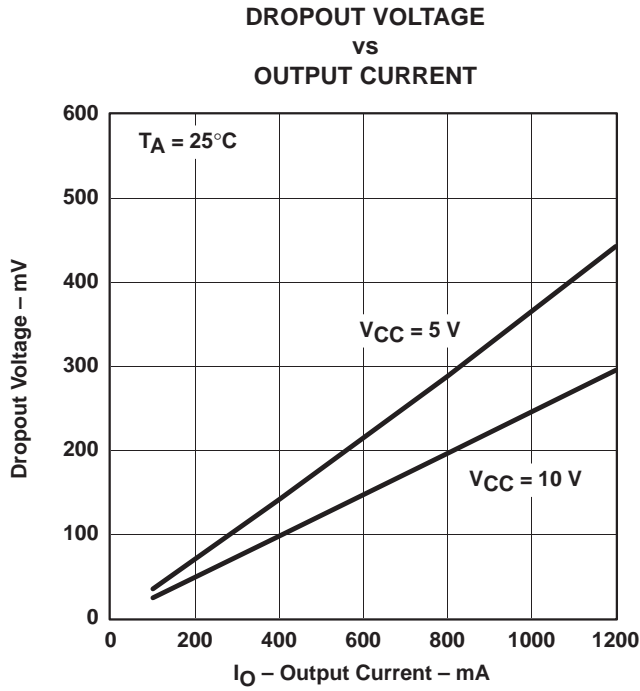


Figure 11

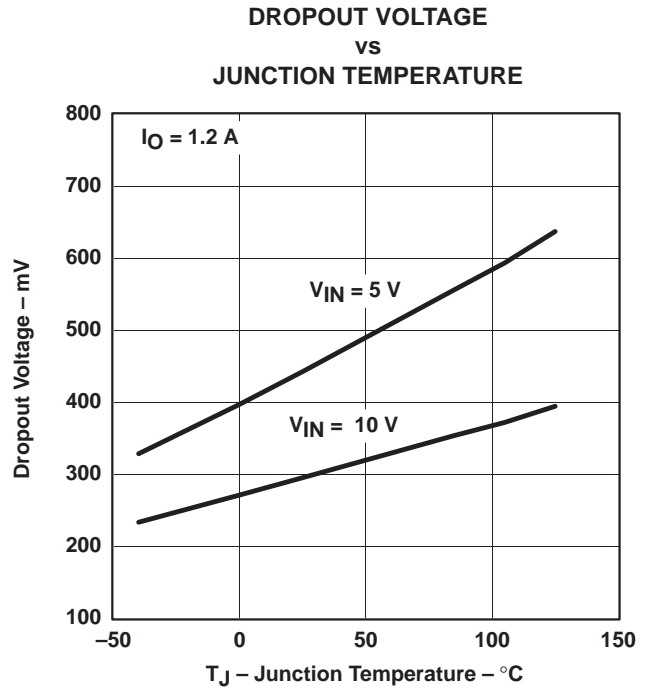


Figure 12

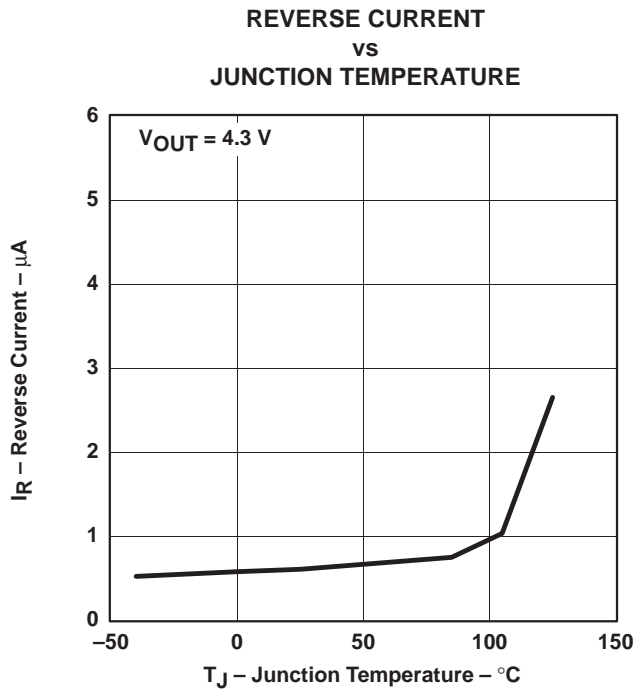


Figure 13

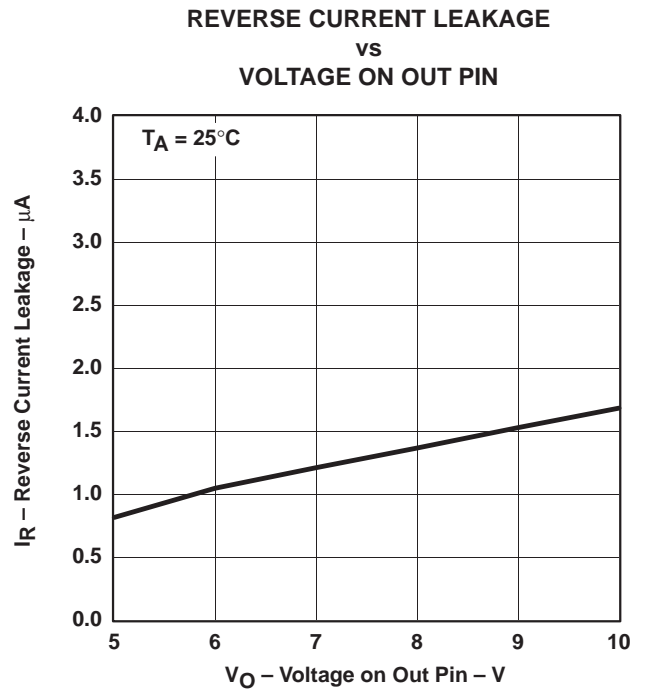


Figure 14

### THERMAL INFORMATION

#### thermally enhanced TSSOP-20

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad (see Figure 15) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

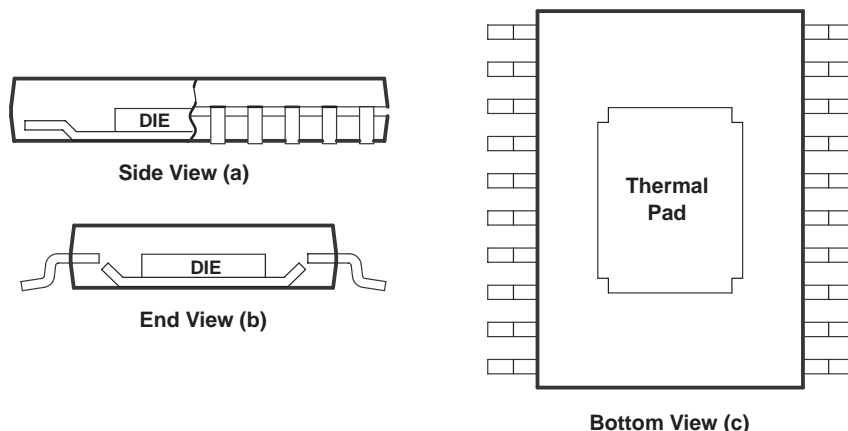


Figure 15. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air (reference Figure 17(a), 8 cm<sup>2</sup> of copper heat sink and natural convection). Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly (see Figures 17(b) and 17(c)). The line drawn at 0.3 cm<sup>2</sup> in Figures 16 and 17 indicates performance at the minimum recommended heat-sink size.

THERMAL INFORMATION

thermally enhanced TSSOP-20 (continued)

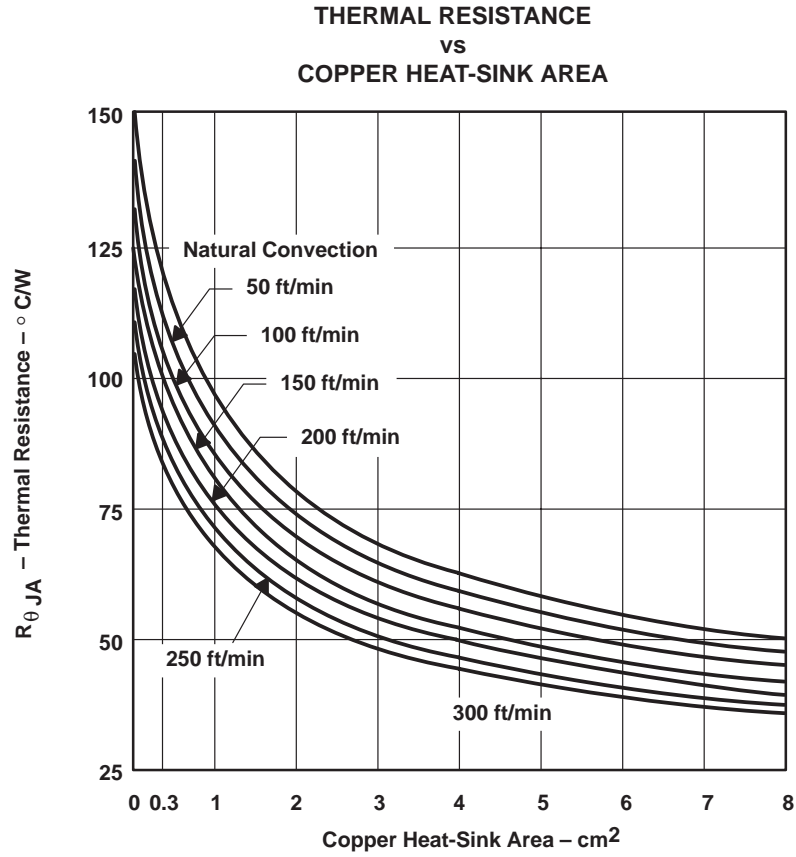
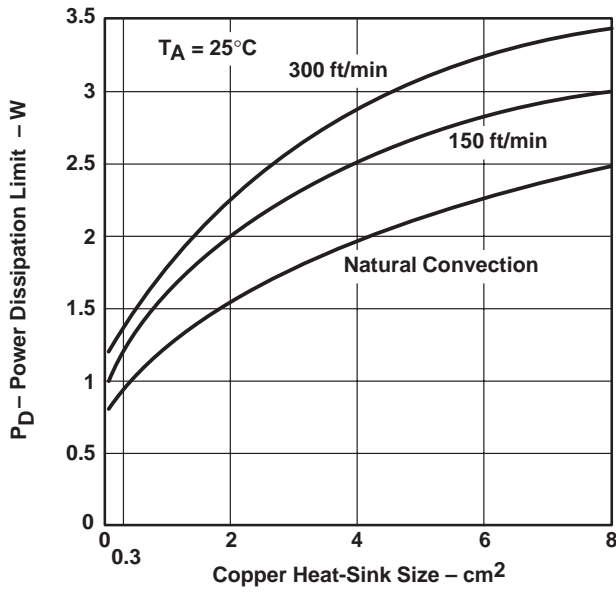


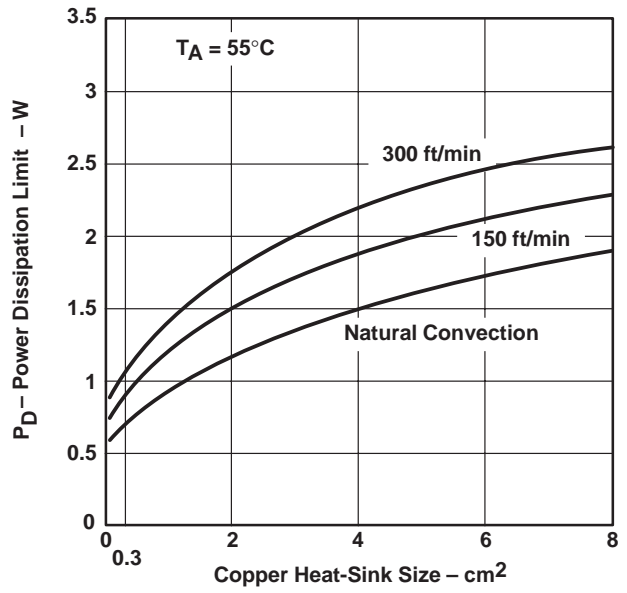
Figure 16

**THERMAL INFORMATION**

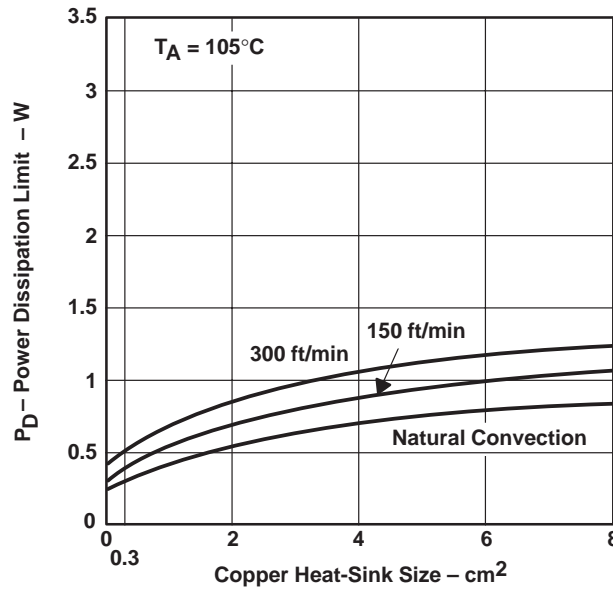
thermally enhanced TSSOP-20 (continued)



(a)



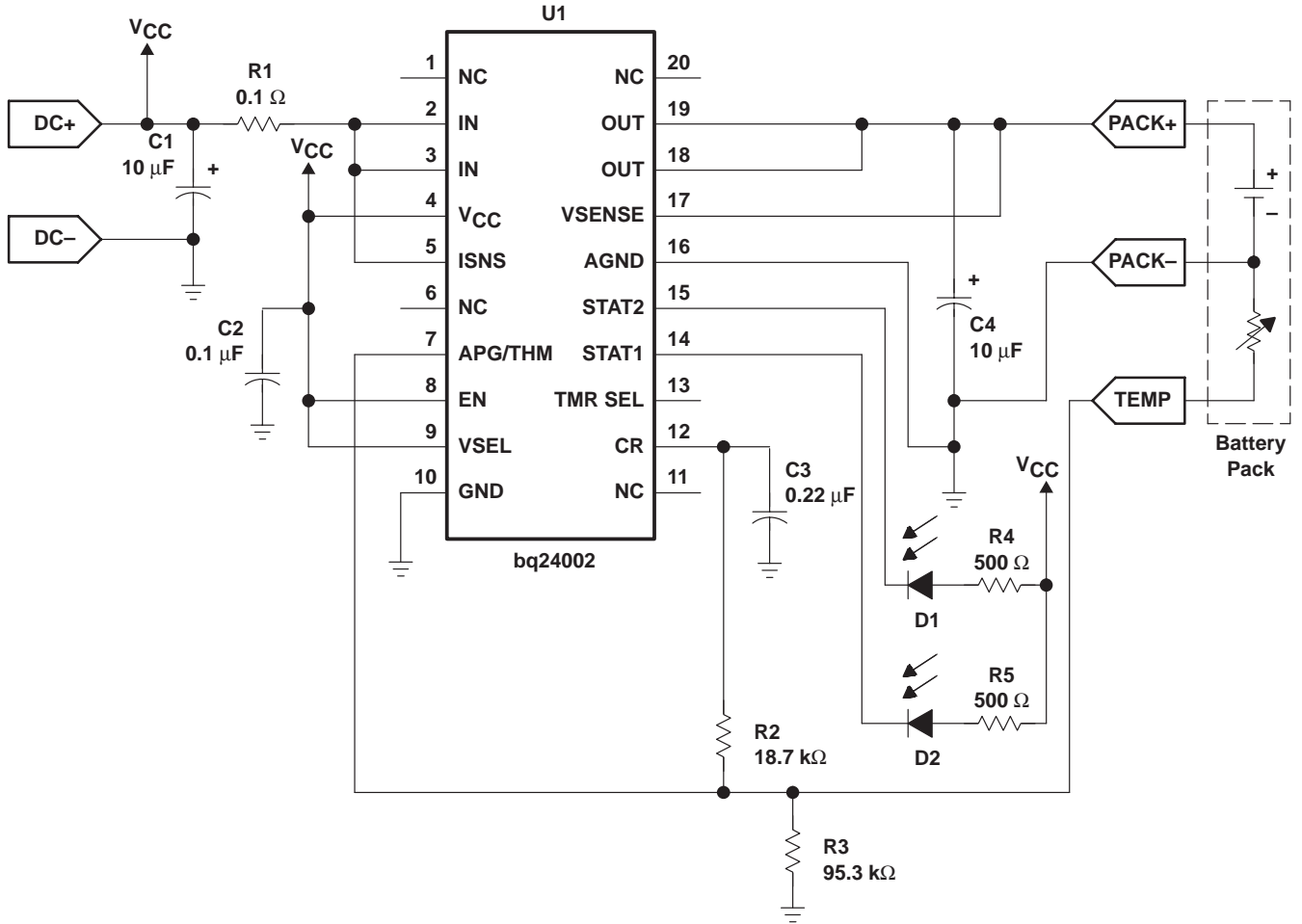
(b)



(c)

Figure 17. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

**APPLICATION INFORMATION**

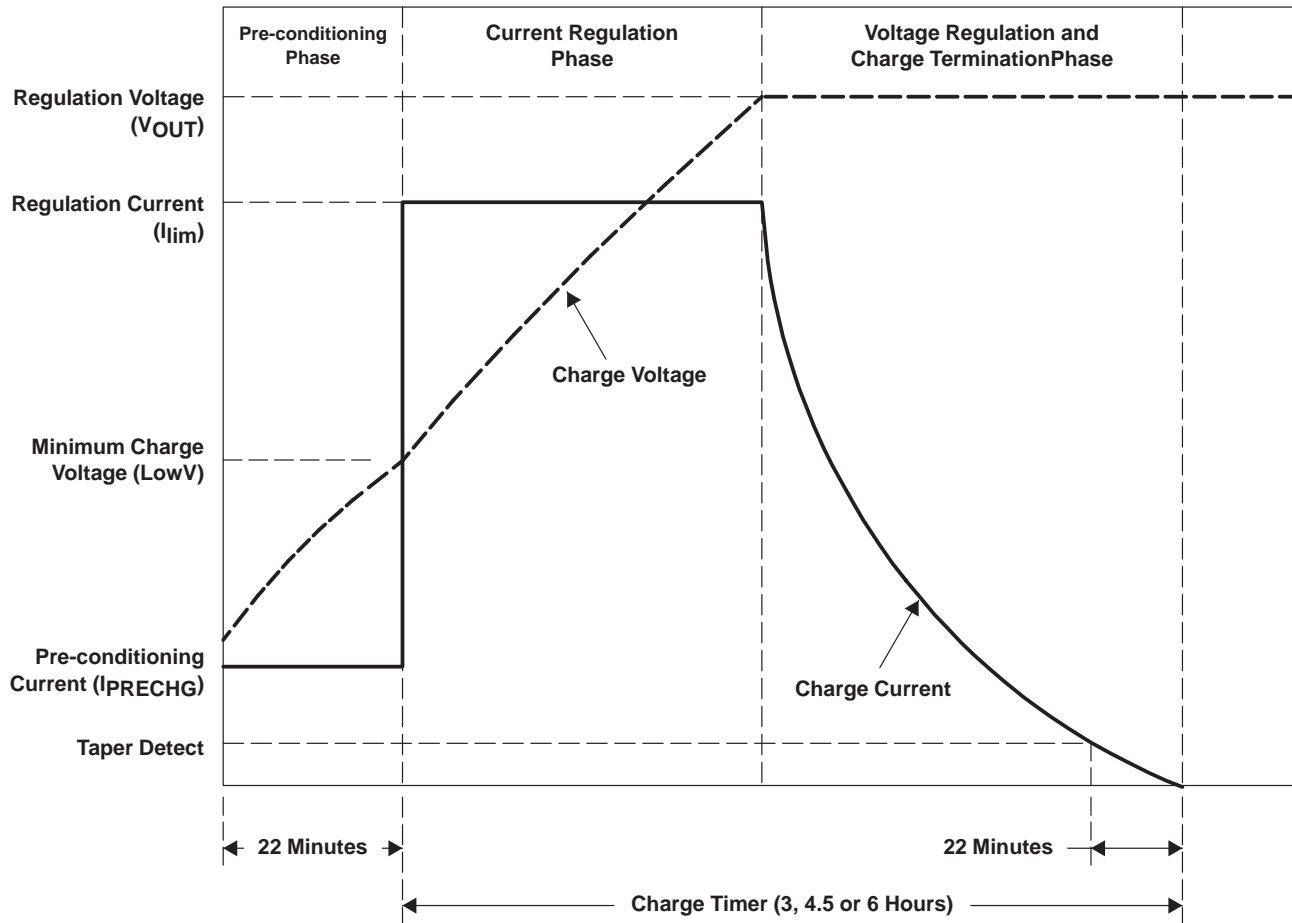


**Figure 18. Application Diagram**

**APPLICATION INFORMATION**

**functional description**

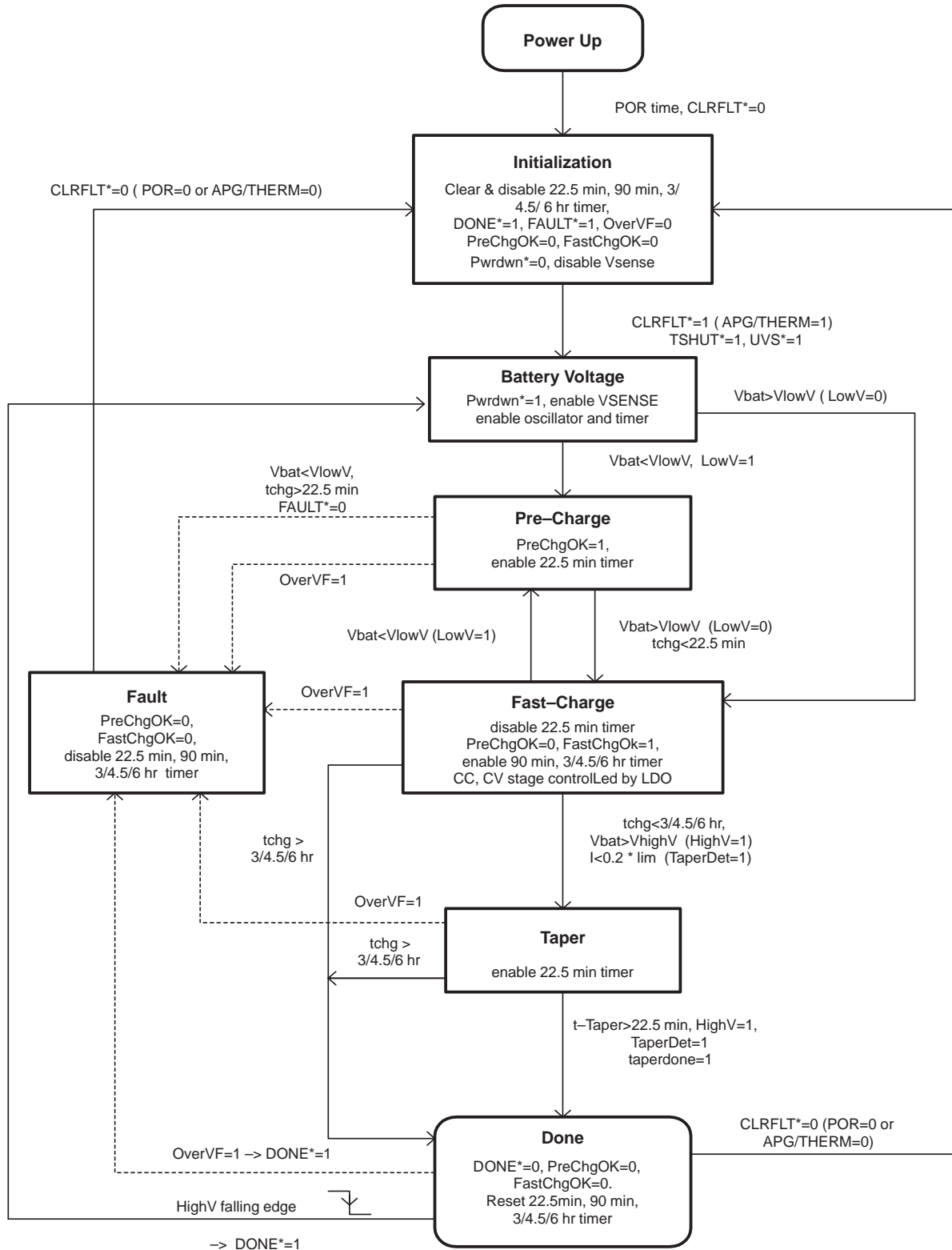
The bq2400x supports a precision current- and voltage-regulated Li-Ion charging system suitable for cells with either coke or graphite anodes. See Figure 21 for a typical charge Profile and Figure 22 for an operational flowchart.



**Figure 19. Typical Charge Profile**



**APPLICATION INFORMATION**



**Figure 20. Operational Flow Chart**

**bq24001, bq24002, bq24003**  
**SINGLE-CELL ADVANCED LINEAR Li-ION CHARGE**  
**MANAGEMENT IC WITH INTEGRATED POWER FET**

SLUS462B – SEPTEMBER 2000 – REVISED FEBRUARY 2001

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**APPLICATION INFORMATION**

**charge qualification and preconditioning**

The bq2400x starts a charge cycle when power is applied while a battery is present. Charge qualification is based on battery voltage and the APG/THERM input.

As shown in the block diagram, the internal LowV comparator output prevents fast-charging a deeply depleted battery and detects a faulty battery. When set, charging current is provided by a dedicated precharge current source. The precharge timer limits the precharge duration. The precharge current also minimizes heat dissipation in the pass element during the initial stage of charge.

The APG/THERM input can also be configured to monitor either the adapter power or the battery temperature using a thermistor. The bq2400x suspends charge if this input is outside the limits set by the user. Please refer to the APG/THERM input section for additional details.

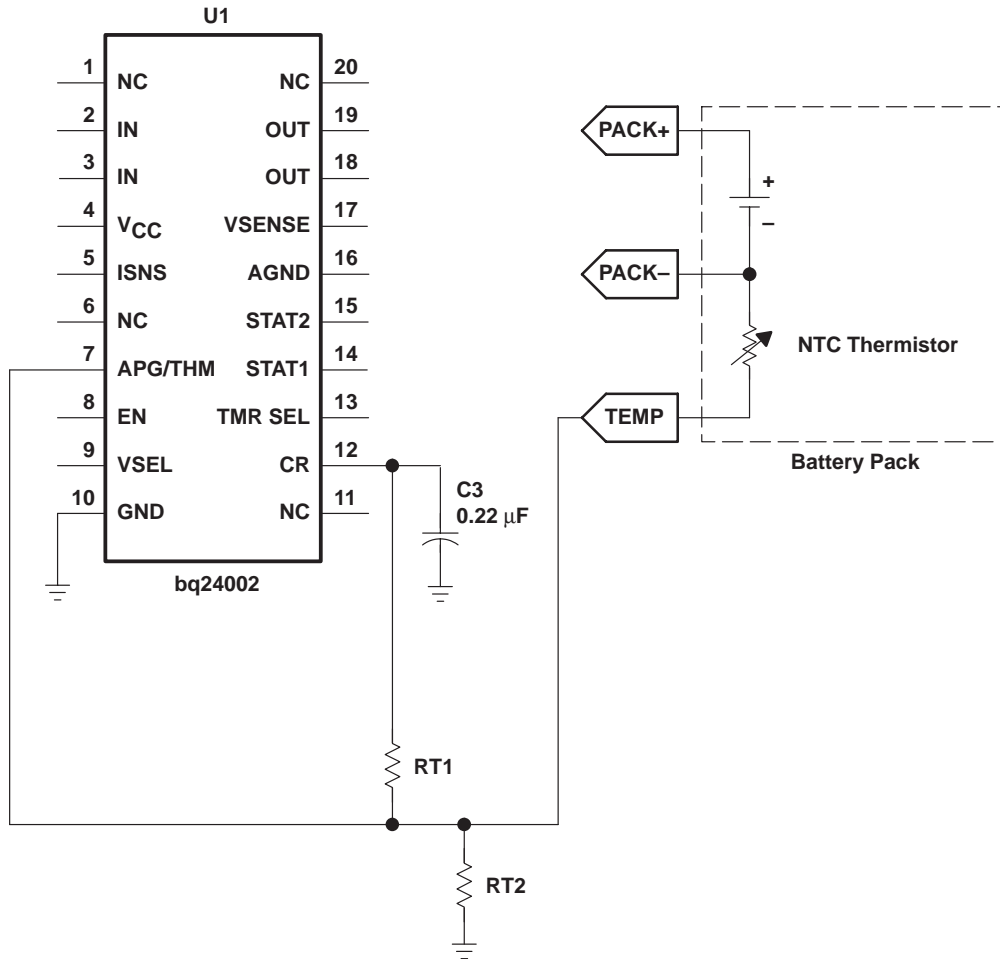
**APG/THERM input**

The bq400x continuously monitors temperature or system input voltage by measuring the voltage between the APG/THERM (Adapter Power Good /thermistor) and GND. For temperature, a negative- or a positive-temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage (see Figure 21). The bq2400x compares this voltage against its internal  $V_{TP1}$  and  $V_{TP2}$  thresholds to determine if charging is allowed (see Figure 22).



**APPLICATION INFORMATION**

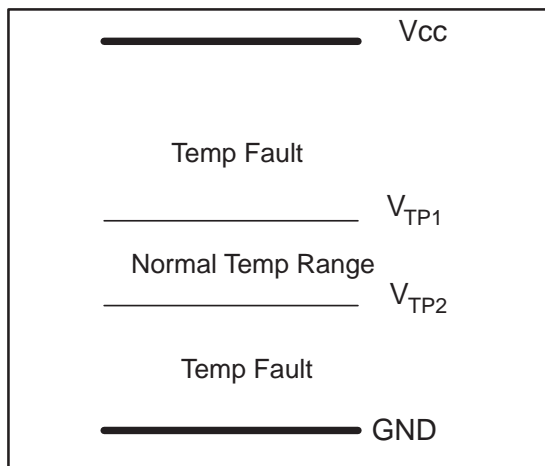
**APG/THERM input (continued)**



**Figure 21. Temperature Sensing Circuit**

**APPLICATION INFORMATION**

**APG/THERM input (continued)**



**Figure 22. Temperature Threshold**

For NTC thermistors, the resistor values of  $R_{T1}$  and  $R_{T2}$  are calculated by the following equations:

$$R_{T1} = \frac{(V_{CR} \times R_{TC} \times R_{TH})(V_{TP1} - V_{TP2})}{(R_{TC} - R_{TH}) \times (V_{TP1} \times V_{TP2})}$$

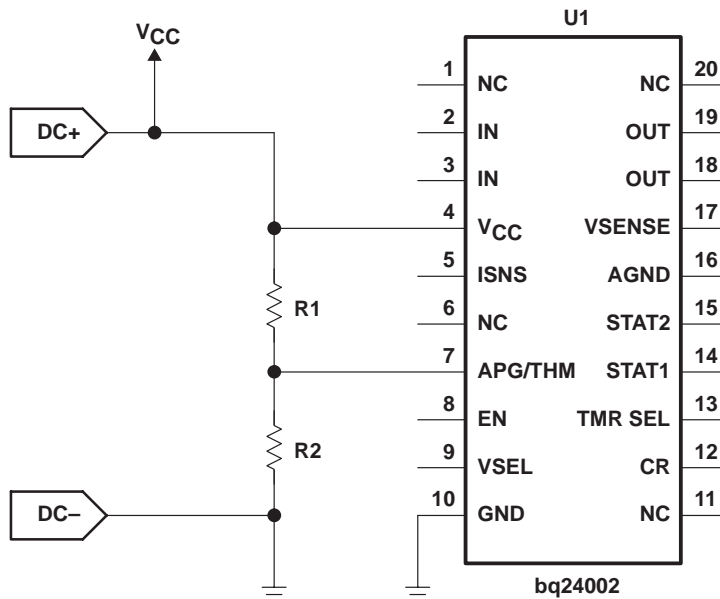
$$R_{T2} = \frac{(-V_{CR} \times R_{TC} \times R_{TH})(V_{TP2} - V_{TP1})}{\left[ (R_{TC} - R_{TH}) \times (V_{TP1} \times V_{TP2}) \right] + \left[ V_{CR} \left( (R_{TH} \times V_{TP1}) - (R_{TC} \times V_{TP2}) \right) \right]}$$

Where  $V_{CR}$  is the output of the CR pin,  $R_{TC}$  is the cold-temperature resistance and  $R_{TH}$  is the hot temperature resistance of the thermistor, as specified by the thermistor manufacturer.  $V_{TP1}$  and  $V_{TP2}$  are the internal thresholds of the window comparator.

The APG/THERM input can also be used to monitor the system-input voltage. Charging is allowed if the voltage developed on this pin is within the internal  $V_{TP1}$  and  $V_{TP2}$  thresholds.

**APPLICATION INFORMATION**

**APG/THERM input (continued)**



**Figure 23. APG Sensing Circuit**

Values of resistors R1 and R2 can be calculated using the following equation:

$$V_{APG} = V_{CC} \frac{R2}{(R1 + R2)}$$

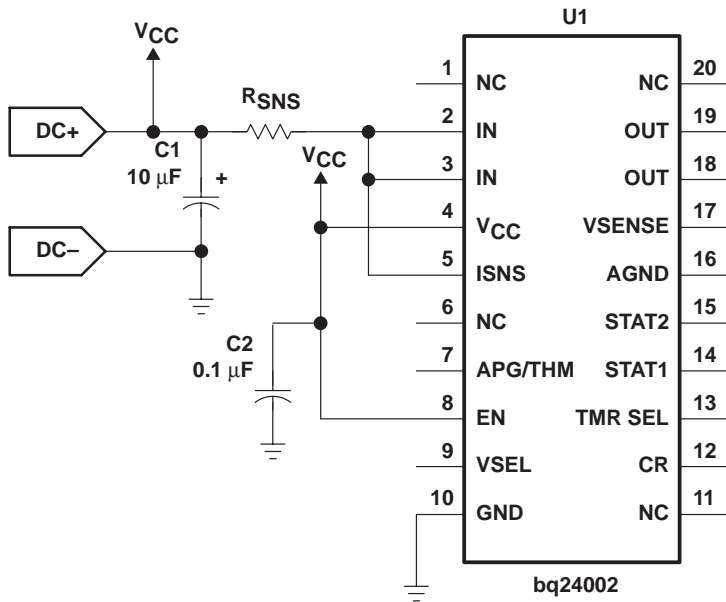
where  $V_{APG}$  is the voltage at the APG/THM pin.

**current regulation**

The bq2400x provides current regulation while the battery-pack voltage is less than the regulation voltage. The current regulation loop effectively amplifies the error between a reference signal,  $V_{lim}$ , and the drop across the external sense resistor,  $R_{SNS}$ .

**APPLICATION INFORMATION**

**current regulation (continued)**



**Figure 24. Current Sensing Circuit**

Charge current feedback, applied through pin ISNS, maintains regulation around a threshold of Vilim. The following formula calculates the value of the sense resistor:

$$R_{SNS} = \frac{V_{lim}}{I_{REG}}$$

where I<sub>REG</sub> is the desired charging current.

**voltage monitoring and regulation**

Voltage regulation feedback is through pin VSENSE. This input is tied directly to the positive side of the battery pack. The bq2400x supports cells with either coke (4.1 V) or graphite (4.2 V) anode. Pin VSEL selects the charge regulation voltage.

VSEL State (see Note)	CHARGE REGULATION VOLTAGE
Low	4.1 V
High	4.2 V

NOTE: VSEL should not be left floating.

## APPLICATION INFORMATION

### charge termination

The bq2400x continues with the charge cycle until termination by one of the two possible termination conditions:

**Maximum Charge Time:** The bq2400x sets the maximum charge time through pin TMRSEL. The TMR SEL pin allows the user to select between three different total charge-time timers (3, 4, 5, or 6 hours). The charge timer is initiated after the preconditioning phase of the charge and is reset at the beginning of a new charge cycle. Note that in the case of a fault condition, such as an out of range signal on the APG/THERM input or a thermal shutdown, the bq2400x suspends the timer.

TMRSEL STATE	CHARGE TIME
Floating†	3 hours
Low	6 hours
High	4.5 hours

† To improve noise immunity, it is recommended that a minimum of 10 pF capacitor be tied to Vss on a floating pin.

**Minimum Current:** The bq2400x monitors the charging current during the voltage regulation phase. The bq2400x initiates a 22-minute timer once the current falls below the Vthres<sub>TAPERDET</sub> level. Fast charge is terminated once the 22-minute timer expires.

### charge status display

The three available options allow the user to configure the charge status display for single LED (bq24001), two individual LEDs (bq24002) or a bicolor LED (bq24003). The output stage is totem pole for the bq24001 and bq24003 and open-drain for the bq24002. The following tables summarize the operation of the three options:

**Table 1. bq24001 (Single LED)**

CHARGE STATE	STAT1
Precharge	ON
Fast charge	ON
FAULT	Flashing (1 Hz, 50% duty cycle)
Done (>90%)	OFF
Sleep-mode	OFF
APG/Therm invalid	OFF
Thermal shutdown	OFF
Battery absent	OFF

**Table 2. bq24002 (2 Individual LEDs)**

CHARGE STATE	STAT1 (RED)	STAT2 (GREEN)
Precharge	ON	OFF
Fast charge	ON	OFF
FAULT	Flashing (1 Hz, 50% duty cycle)	OFF
Done (>90%)	OFF	ON
Sleep-mode	OFF	OFF
APG/Therm invalid	OFF	OFF
Thermal shutdown	OFF	OFF
Battery absent	OFF	OFF‡

‡ If thermistor is used, then the Green LED will be off.

**APPLICATION INFORMATION**

**charge status display (continued)**

**Table 3. bq24003 (Single Bicolor LED)**

CHARGE STATE	LED1 (RED)	LED2 (GREEN)	APPARENT COLOR
Precharge	ON	OFF	RED
Fast charge	ON	OFF	RED
FAULT	ON	ON	YELLOW
Done (>90%)	OFF	ON	GREEN
Sleep-mode	OFF	OFF	OFF
APG/Therm invalid	OFF	OFF	OFF
Thermal shutdown	OFF	OFF	OFF
Battery absent	OFF	OFF <sup>‡</sup>	OFF <sup>‡</sup>

<sup>‡</sup> If thermistor is used, then the Green LED will be off.

**thermal shutdown**

The bq2400x monitors the junction temperature,  $T_J$ , of the DIE and suspends charging if  $T_J$  exceeds 165°C. Charging resumes when  $T_J$  falls below 155°C.

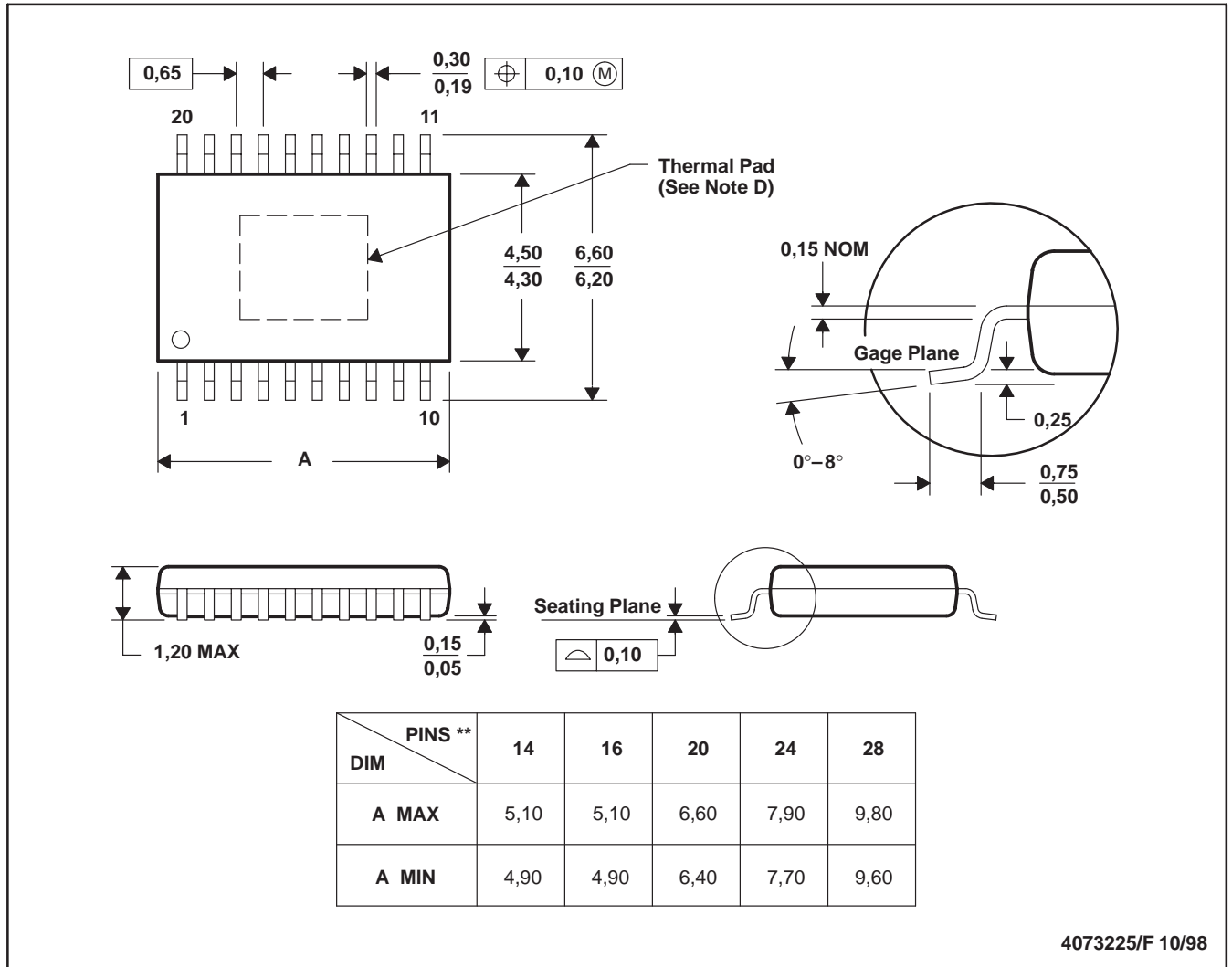


MECHANICAL DATA

PWP (R-PDSO-G\*\*)

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusions.  
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.  
 E. Falls within JEDEC MO-153.

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