



VN800S-E VN800PT-E

HIGH SIDE DRIVER

Table 1. General Features

Type	R _{DS(on)}	I _{OUT}	V _{CC}
VN800S-E VN800PT-E	135 mΩ	0.7 A	36 V

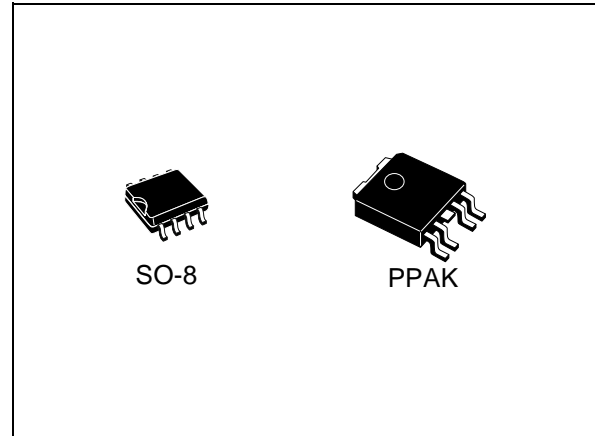
- CMOS COMPATIBLE INPUT
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VN800S-E, VN800PT-E are monolithic devices made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active V_{CC} pin voltage clamp protects the device against low energy spikes.

Figure 1. Package



Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in norms conformity with IEC1131 (Programmable Controllers International Standard).

Table 2. Order Codes

Package	Tube	Tape and Reel
SO-8	VN800S-E	VN800STR-E
PPAK	VN800PT-E	VN800PTTR-E

Note: (*) See application schematic at page 10.

Figure 2. Block Diagram

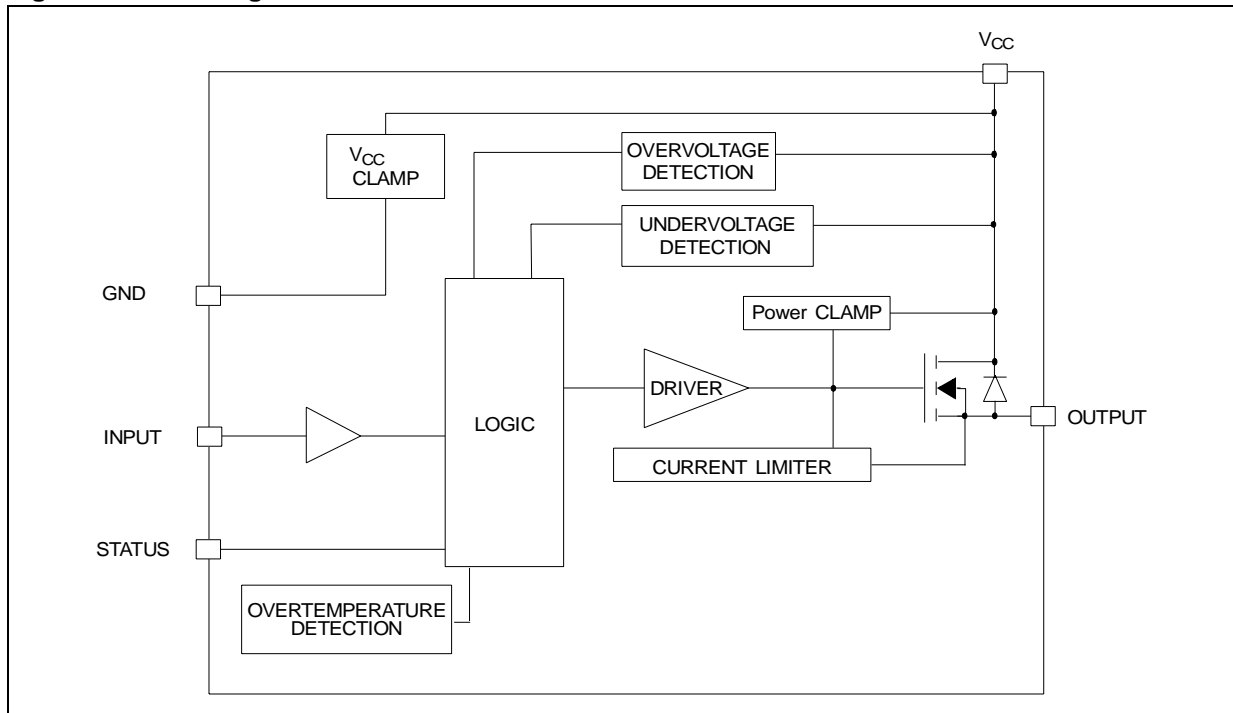


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		SO-8	PPAK	
V_{CC}	DC Supply Voltage	41		V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3		V
$-I_{GND}$	DC Reverse Ground Pin Current	- 200		mA
I_{OUT}	DC Output Current	Internally Limited		A
$-I_{OUT}$	Reverse DC Output Current	- 6		A
I_{IN}	DC Input Current	+/- 10		mA
V_{IN}	Input Voltage Range	-3/+ V_{CC}		V
V_{STAT}	DC Status Voltage	+ V_{CC}		V
V_{ESD}	Electrostatic Discharge (Human Body Model: $R=1.5K\Omega$; $C=100pF$)			
	- INPUT	4000		V
	- STATUS	4000		V
	- OUTPUT	5000		V
	- V_{CC}	5000		V
P_{tot}	Power Dissipation $T_C=25^\circ C$	4.2	41.7	W
E_{MAX}	Maximum Switching Energy ($L=77.5mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=1.5A$)	121		mJ
E_{MAX}	Maximum Switching Energy ($L=125mH$; $R_L=0\Omega$; $V_{bat}=13.5V$; $T_{jstart}=150^\circ C$; $I_L=1.5A$)		195	mJ
T_j	Junction Operating Temperature	Internally Limited		$^\circ C$
T_c	Case Operating Temperature	- 40 to 150		$^\circ C$
T_{stg}	Storage Temperature	- 55 to 150		$^\circ C$
L_{max}	Max Inductive Load ($V_{CC}=30V$; $I_{LOAD}=0.5A$; $T_{amb}=100^\circ C$; $R_{thcase>ambient}\leq 25^\circ C/W$)		2	H

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

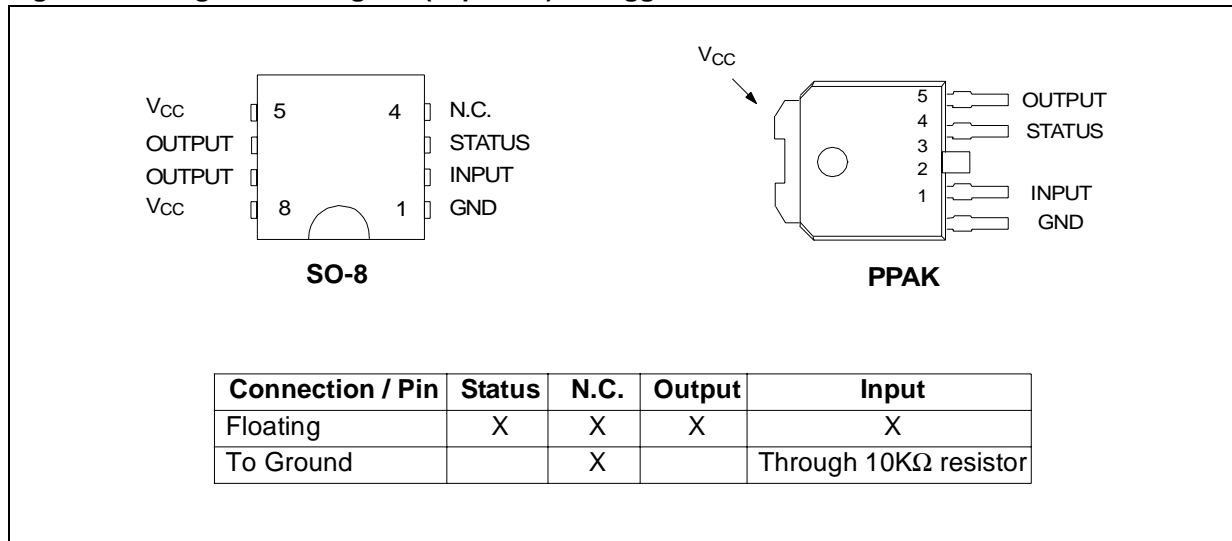


Figure 4. Current and Voltage Conventions

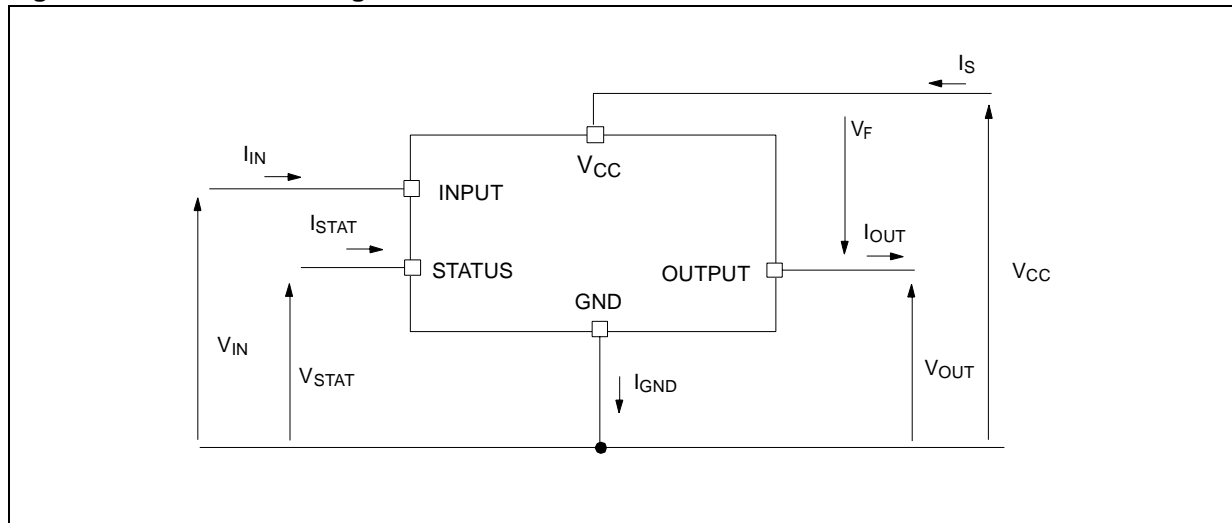


Table 4. Thermal Data

Symbol	Parameter	Max	Value		Unit
			SO-8	PPAK	
R _{thj-case}	Thermal Resistance Junction-case	Max	-	3	°C/W
R _{thj-lead}	Thermal Resistance Junction-lead	Max	30	-	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	93 ⁽¹⁾	78 ⁽³⁾	°C/W
		Max	82 ⁽²⁾	45 ⁽⁴⁾	°C/W

(¹) When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35μ thick) connected to all V_{CC} pins.

(²) When mounted on FR4 printed circuit board with 2 cm² of copper area (at least 35μ thick).

(³) When mounted on FR4 printed circuit board with 0.5 cm² of copper area (at least 35μ thick) connected to all V_{CC} pins.

(⁴) When mounted on FR4 printed circuit board with 6 cm² of copper area (at least 35μ thick).

ELECTRICAL CHARACTERISTICS ($8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$ unless otherwise specified)

Table 5. Power

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Supply Voltage		5.5		36	V
V_{USD}	Undervoltage Shut-down		3	4	5.5	V
V_{OV}	Overvoltage Shut-down		36	42		V
R_{ON}	On State Resistance	$I_{OUT} = 0.5A$; $T_j = 25^{\circ}C$ $I_{OUT} = 0.5A$			135 270	$m\Omega$ $m\Omega$
I_S	Supply Current	Off State; $V_{CC} = 24V$; $T_{case} = 25^{\circ}C$ On State; $V_{CC} = 24V$ On State; $V_{CC} = 24V$; $T_{case} = 100^{\circ}C$		10 1.5	20 3.5 2.6	μA mA mA
I_{LGND}	Output Current at turn-off	$V_{CC} = V_{STAT} = V_{IN} = V_{GND} = 24V$; $V_{OUT} = 0V$			1	mA
$I_{L(off1)}$	Off State Output Current	$V_{IN} = V_{OUT} = 0V$	0		50	μA
$I_{L(off2)}$	Off State Output Current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 125^{\circ}C$			5	μA
$I_{L(off3)}$	Off State Output Current	$V_{IN} = V_{OUT} = 0V$; $V_{CC} = 13V$; $T_j = 25^{\circ}C$			3	μA

Table 6. Switching ($V_{CC} = 24V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$R_L = 48\Omega$ from V_{IN} rising edge to $V_{OUT} = 2.4V$		10		μs
$t_{d(off)}$	Turn-off Delay Time	$R_L = 48\Omega$ from V_{IN} falling edge to $V_{OUT} = 21.6V$		40		μs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	$R_L = 48\Omega$ from $V_{OUT} = 2.4V$ to $V_{OUT} = 19.2V$		See relative diagram		$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	$R_L = 48\Omega$ from $V_{OUT} = 21.6V$ to $V_{OUT} = 2.4V$		See relative diagram		$V/\mu s$

Table 7. Input Pin

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{INL}	Input Low Level				1.25	V
I_{INL}	Low Level Input Current	$V_{IN} = 1.25V$	1			μA
V_{INH}	Input High Level		3.25			V
I_{INH}	High Level Input Current	$V_{IN} = 3.25V$			10	μA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
I_{IN}	Input Current	$V_{IN} = V_{CC} = 36V$			200	μA

ELECTRICAL CHARACTERISTICS (continued)

Table 8. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward on Voltage	$-I_{OUT}=0.6A$; $T_j=150^{\circ}C$			0.6	V

Table 9. Status Pin

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT}=1.6\text{ mA}$			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; $V_{STAT}=V_{CC}=36\text{ V}$			10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; $V_{STAT}=5V$			30	pF

Table 10. Protections (see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^{\circ}C$
T_R	Reset Temperature		135			$^{\circ}C$
T_{hyst}	Thermal Hysteresis		7	15		$^{\circ}C$
T_{SDL}	Status Delay in Overload Condition	$T_j > T_{jsh}$			20	μs
I_{lim}	DC Short Circuit Current	$V_{CC}=24V$; $R_{LOAD}=10m\Omega$	0.7		2	A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=0.5\text{ A}$; $L=6mH$	$V_{CC}-47$	$V_{CC}-52$	$V_{CC}-57$	V

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Figure 5.

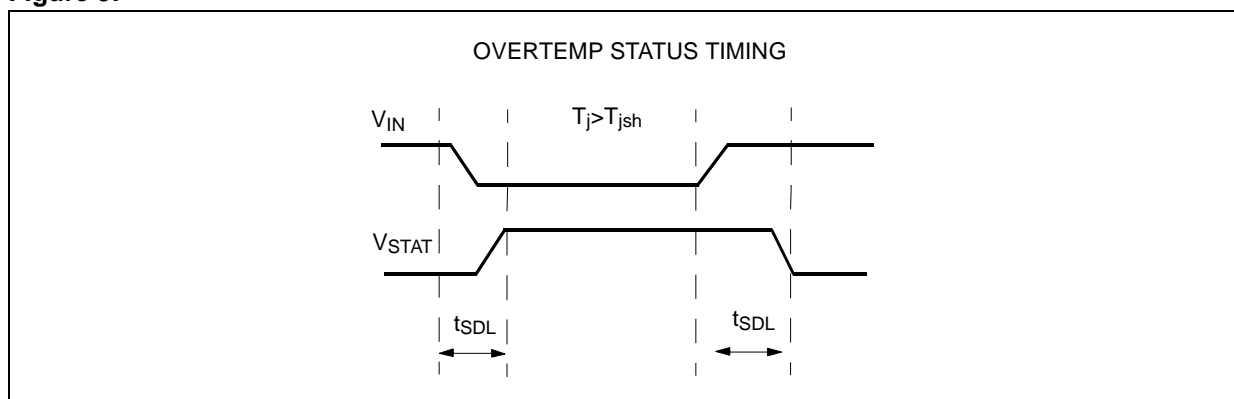


Table 11. Truth Table

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	($T_j < T_{TSD}$) H
	H	X	($T_j > T_{TSD}$) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Figure 6. Switching time Waveforms

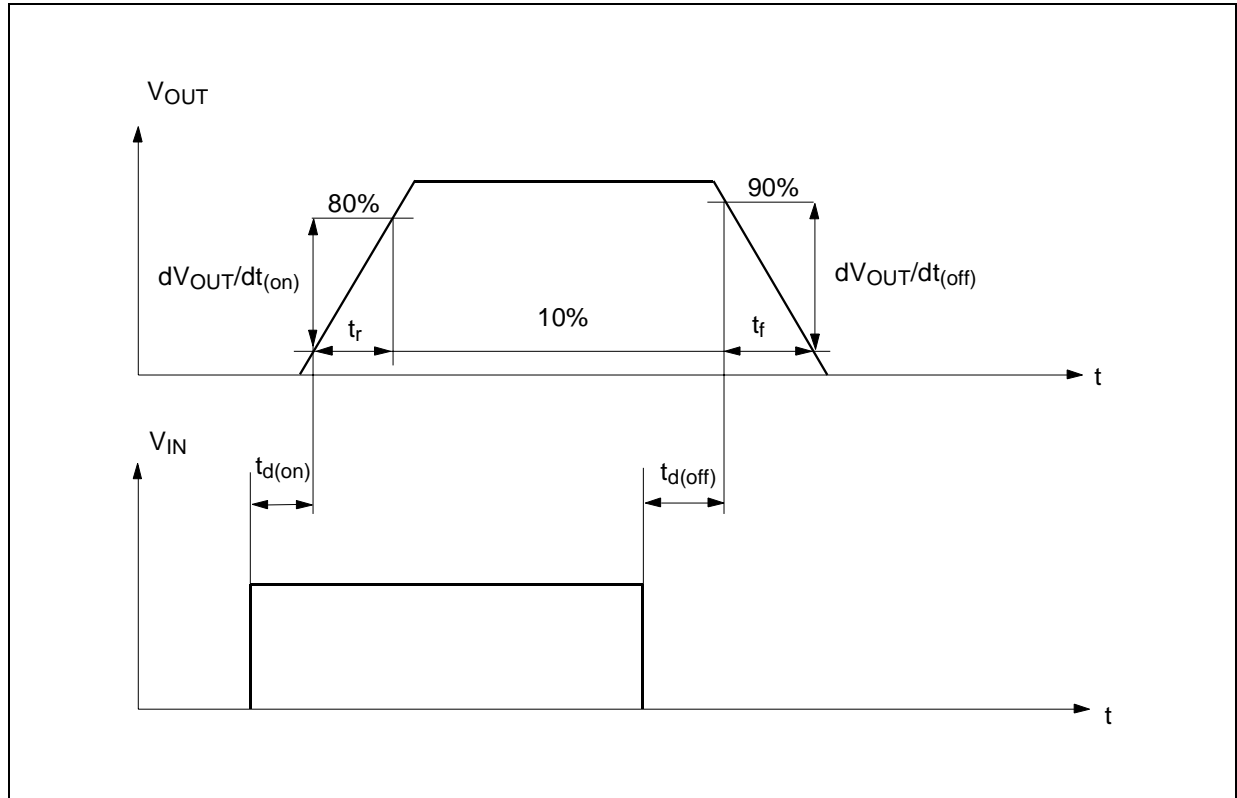


Table 12. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Peak Short Circuit Current Test Circuit

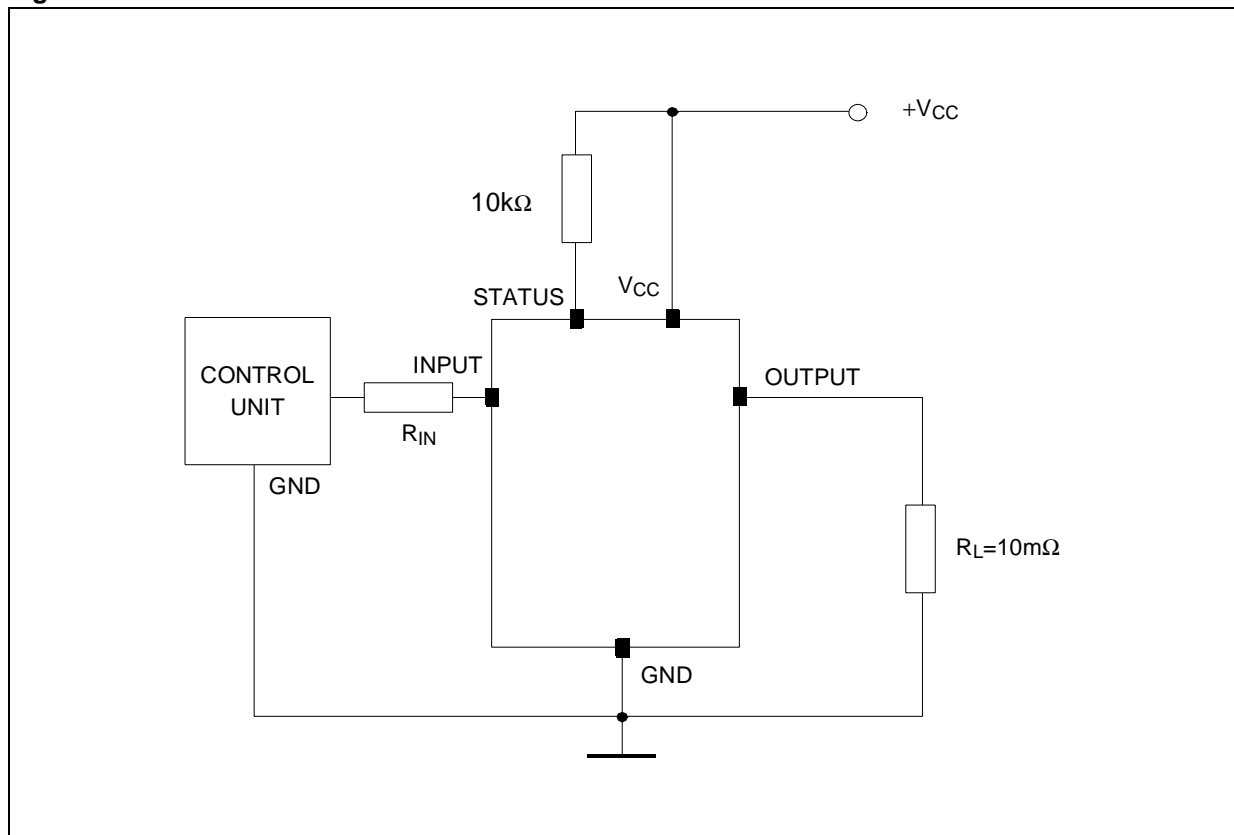


Figure 8. Avalanche Energy Test Circuit

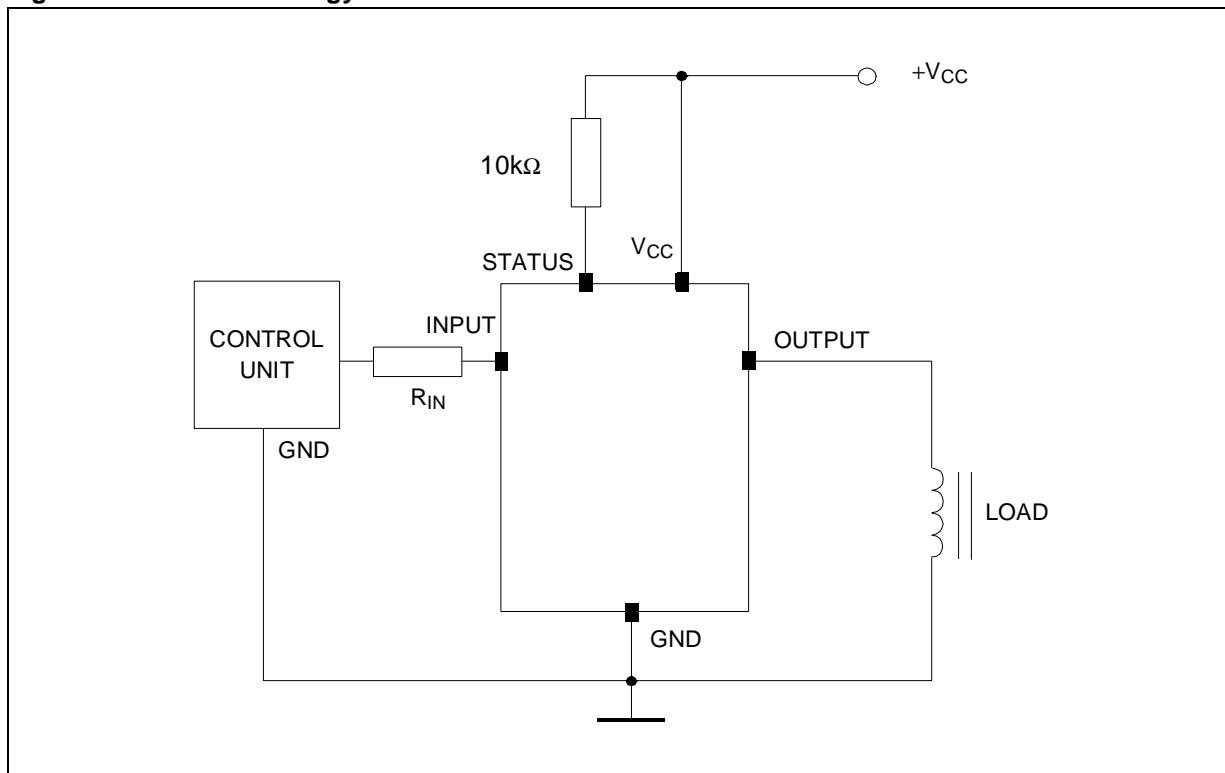


Figure 9. Waveforms

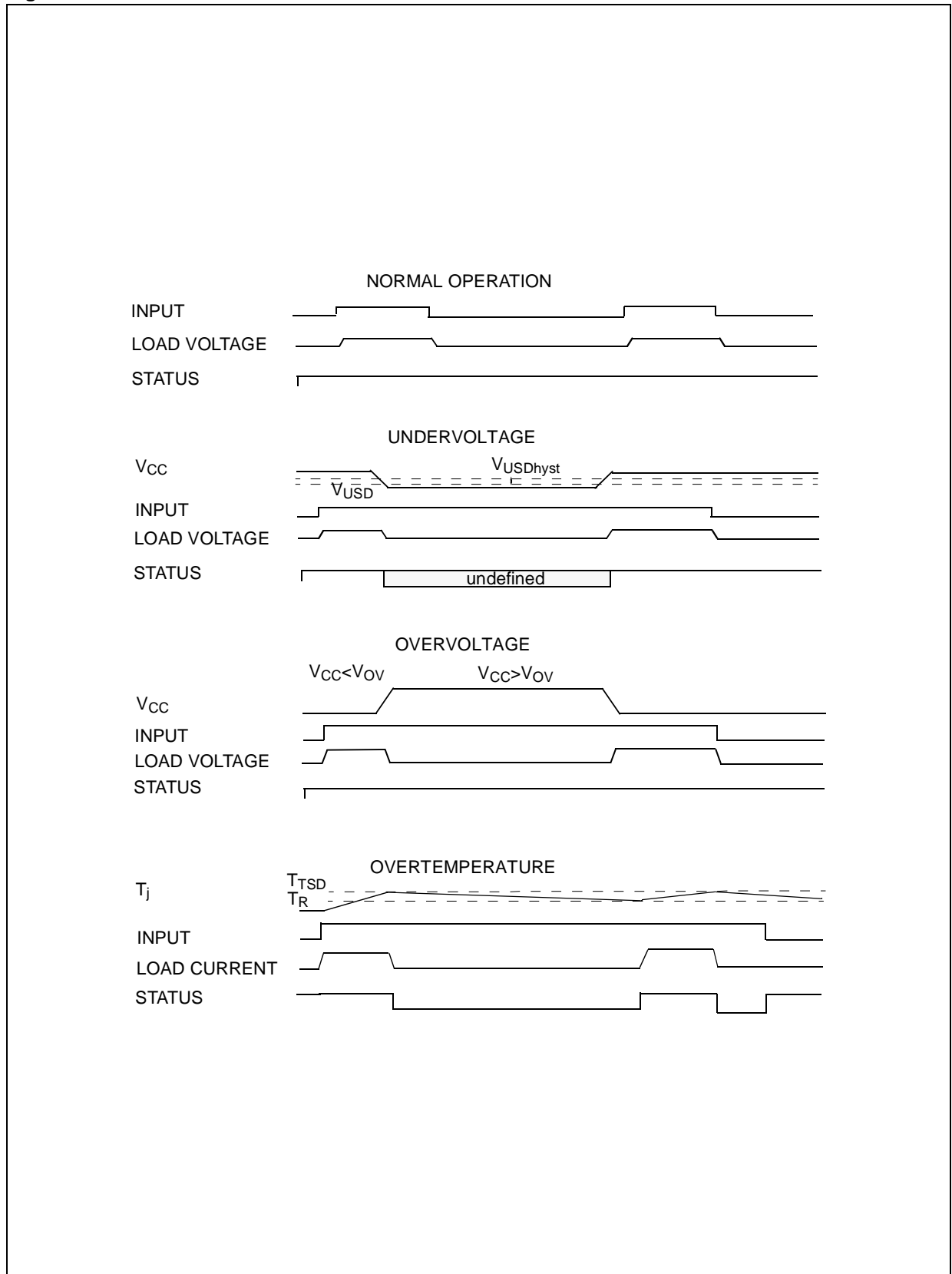
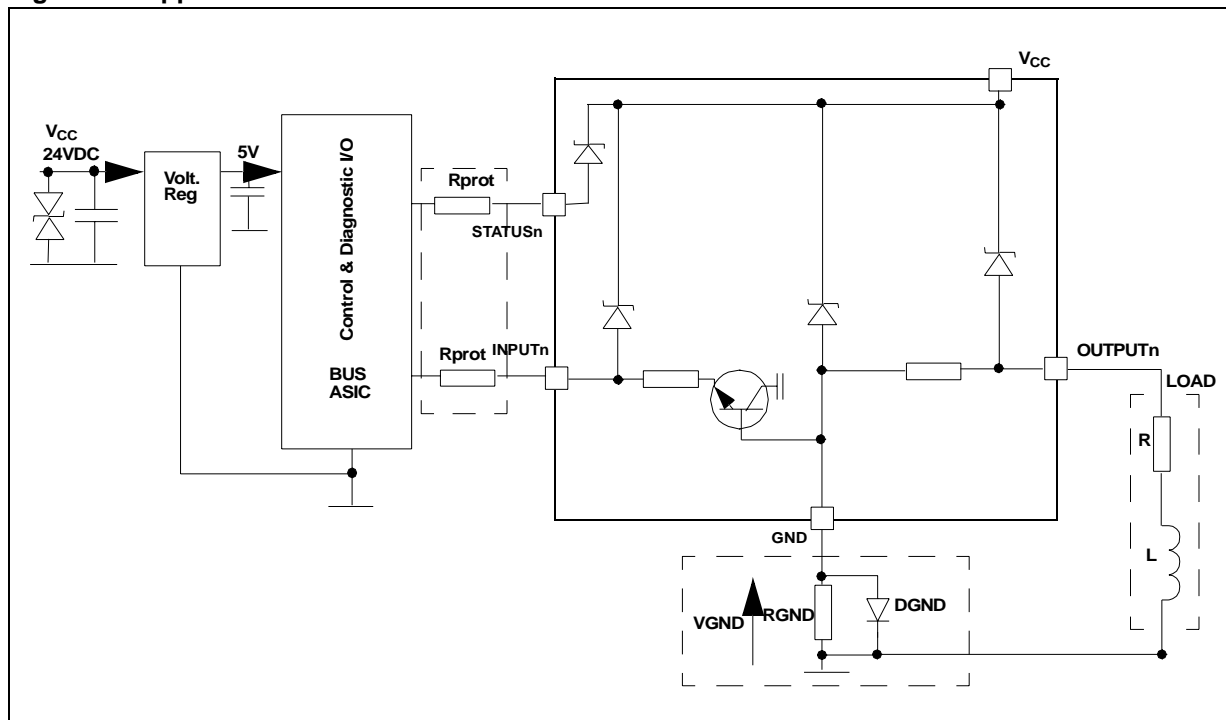


Figure 10. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600mV / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I_{GND} is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where I_{S(on)max} becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift (I_{S(on)max} * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

μC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak}= - 100V and I_{latchup} ≥ 20mA; V_{OHμC} ≥ 4.5V

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended R_{prot} value is 10kΩ.

Figure 11. Off State Output Current

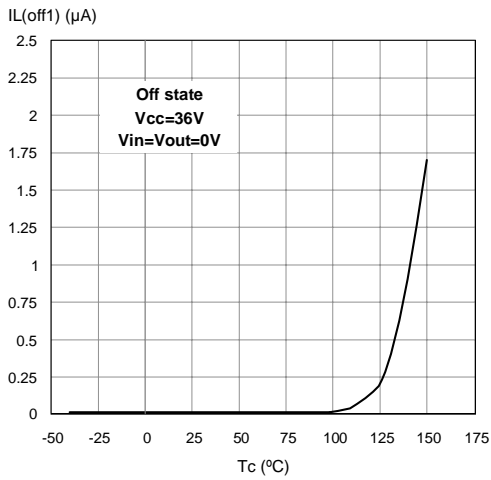


Figure 12. High Level Input Current

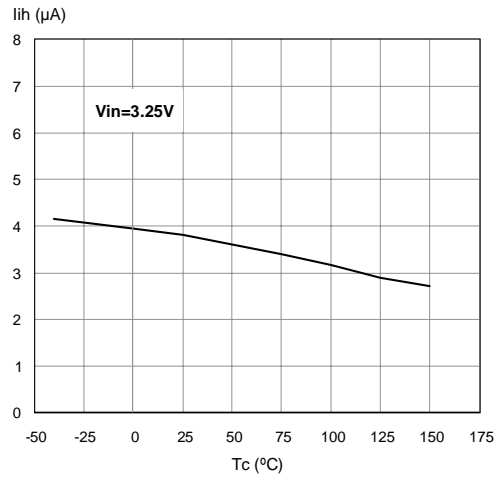


Figure 13. Status Leakage Current

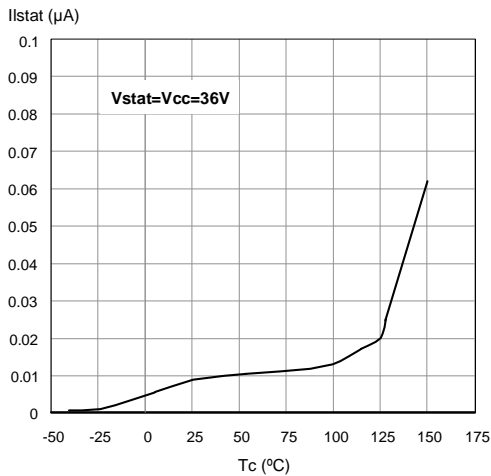


Figure 15. On State Resistance Vs VCC

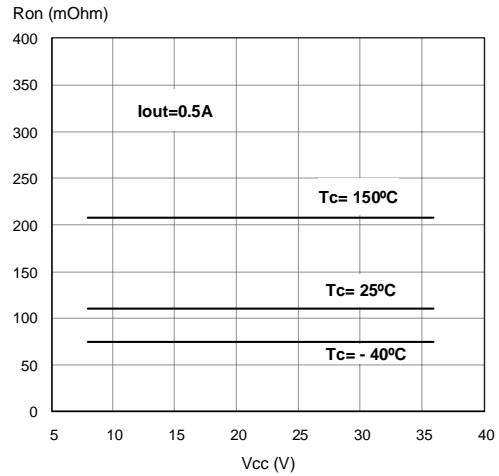


Figure 14. On State Resistance Vs Tcase

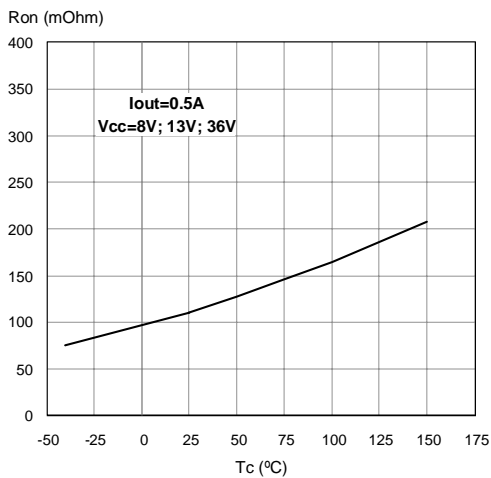


Figure 16. Input High Level

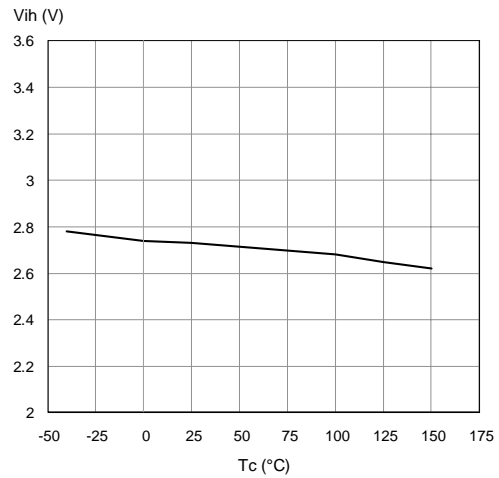


Figure 17. Input Low Level

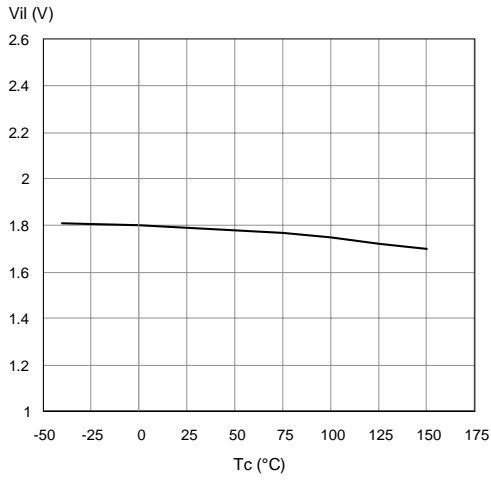


Figure 20. Input Hysteresis Voltage

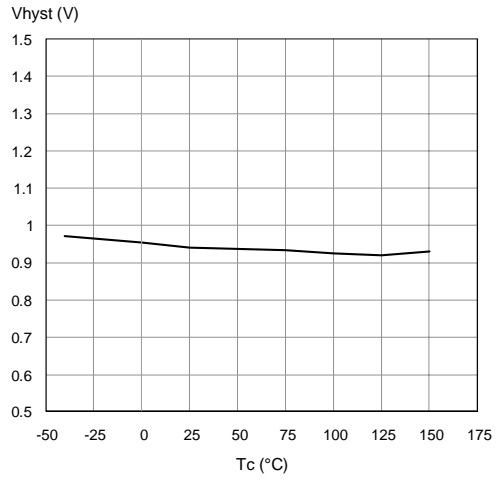


Figure 18. Turn-on Voltage Slope

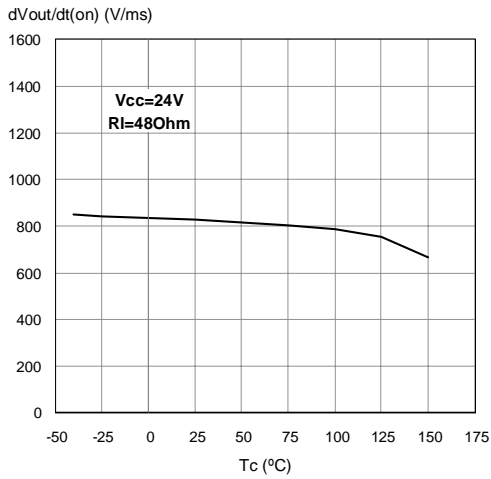


Figure 21. Turn-off Voltage Slope

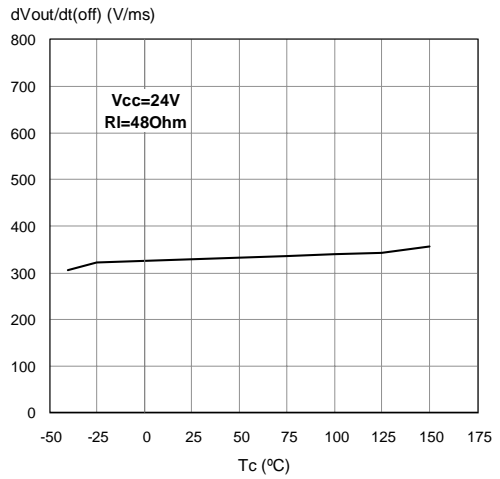


Figure 19. Overvoltage Shutdown

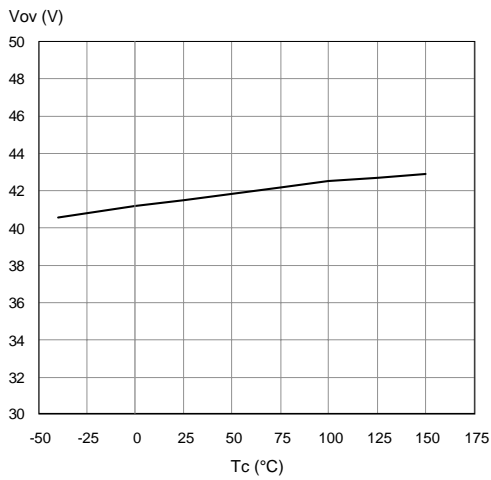


Figure 22. I_{LIM} Vs T_{case}

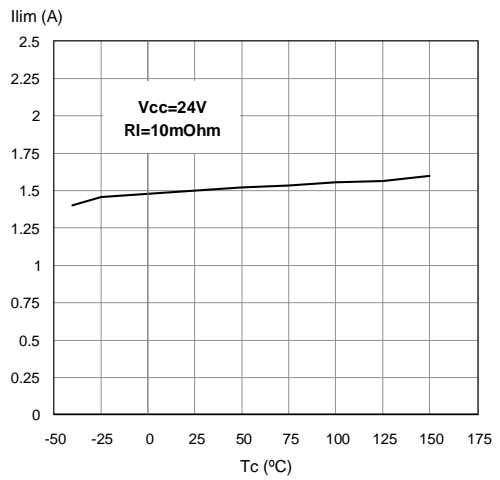
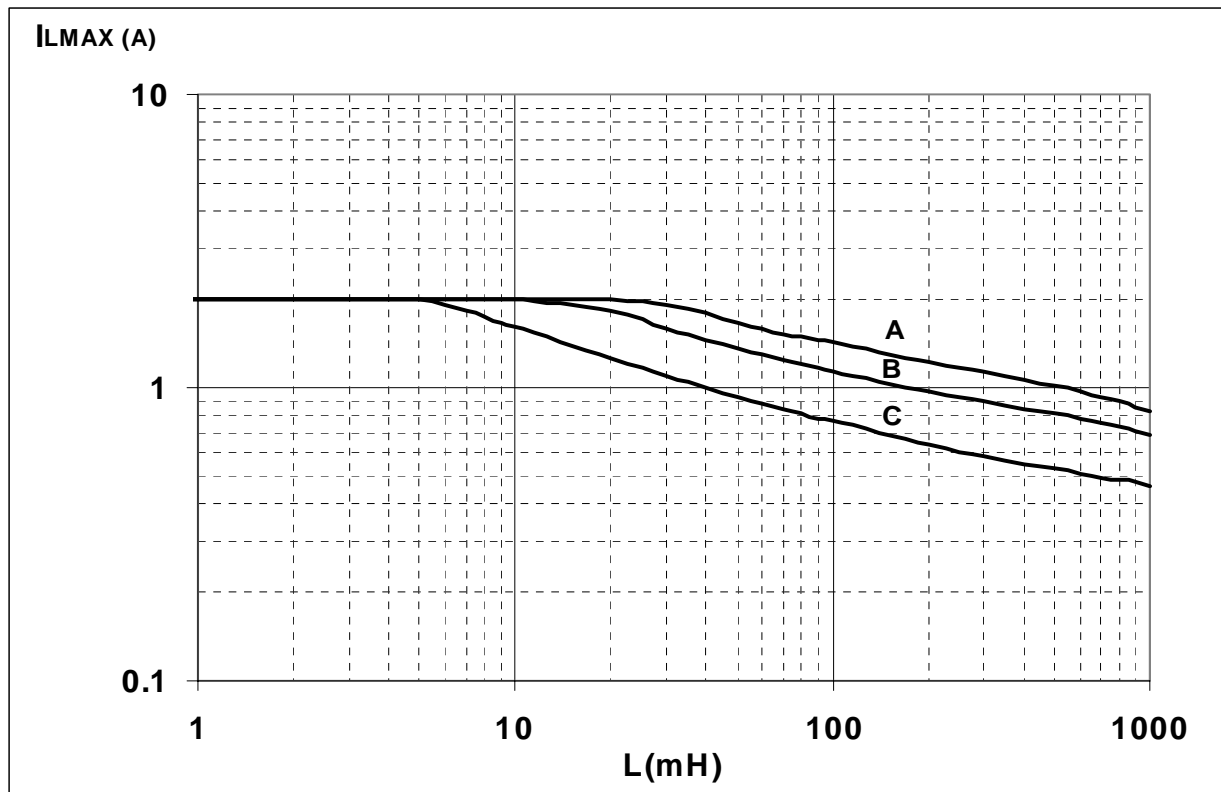


Figure 23. SO-8 Maximum turn off current versus load inductance



- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B = Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C = Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$

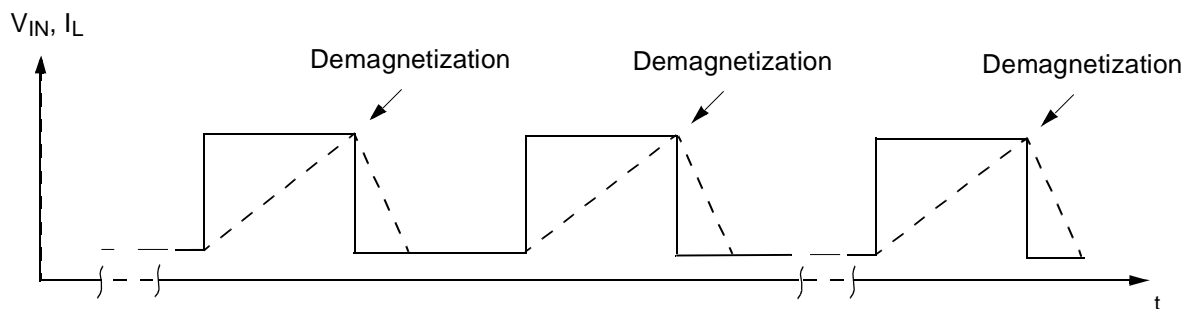
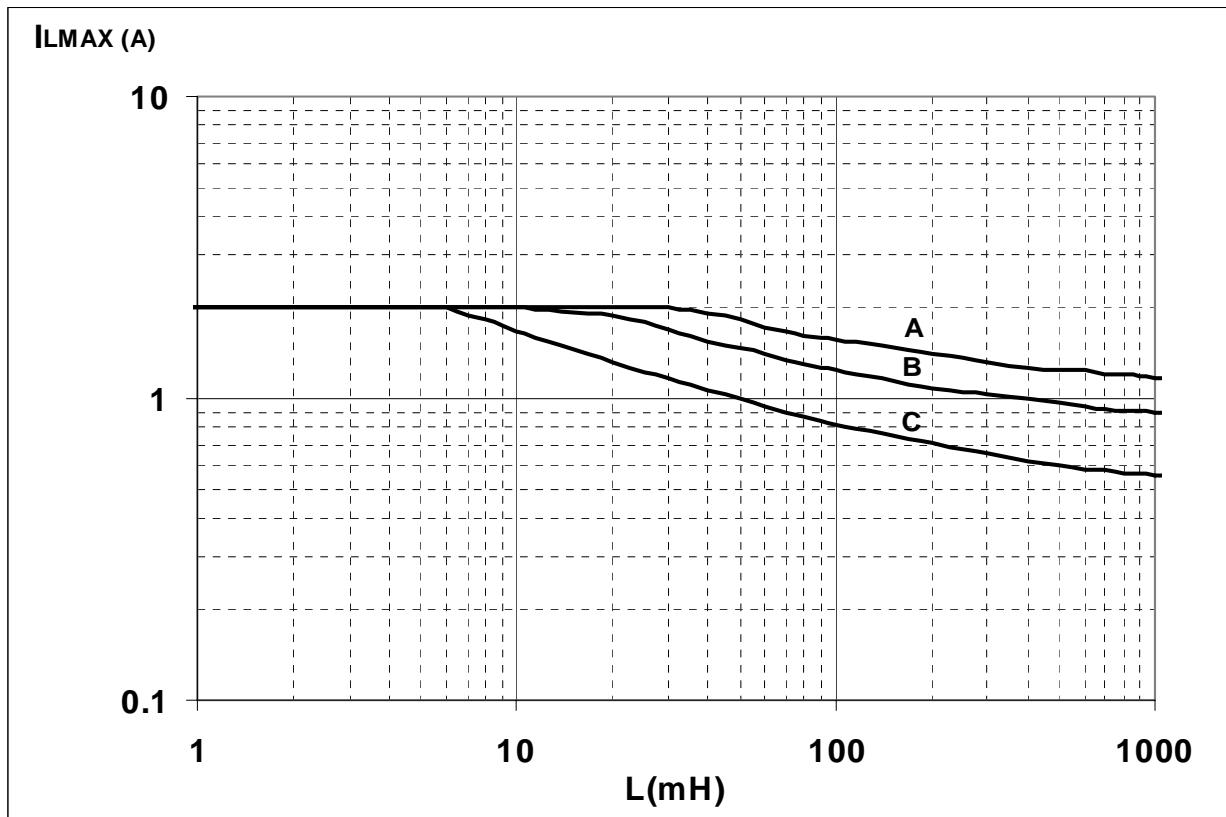


Figure 24. PPAK Maximum turn off current versus load inductance



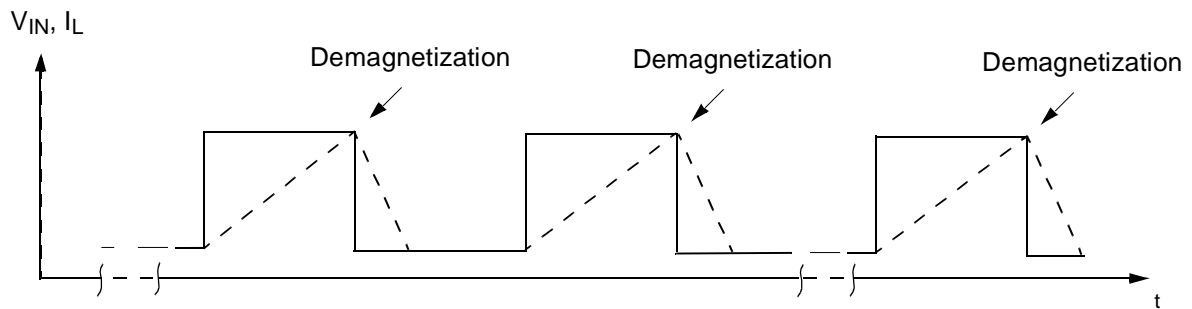
- A = Single Pulse at $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at $T_{Jstart}=125^{\circ}C$

Values are generated with $R_L=0\Omega$

In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Conditions:

$V_{CC}=13.5V$



SO-8 Thermal Data

Figure 25. SO-8 PC Board

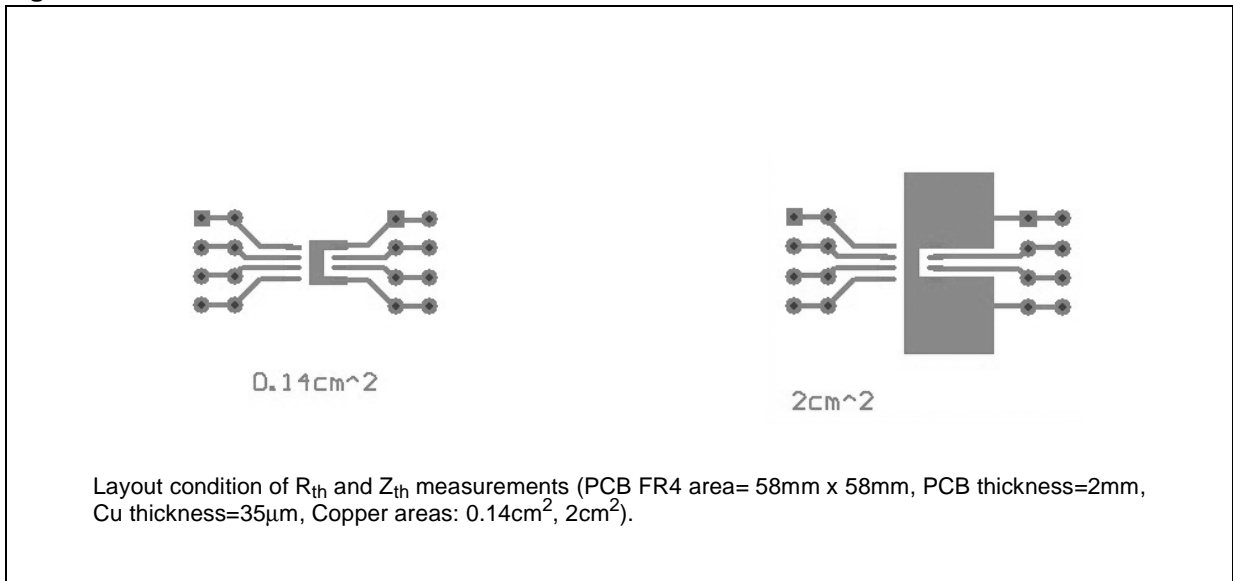
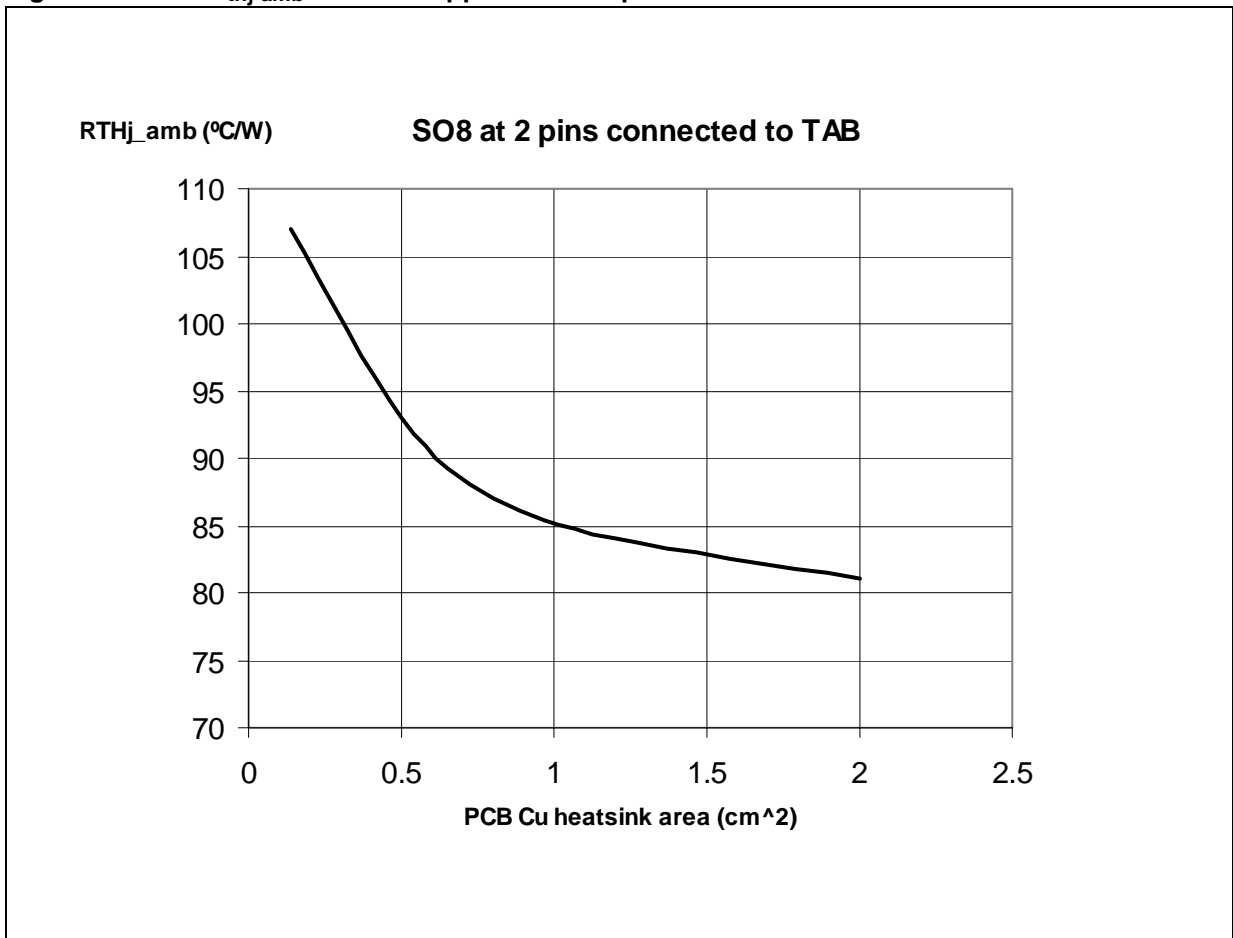


Figure 26. SO-8 $R_{thj-amb}$ Vs PCB copper area in open box free air condition



PPAK Thermal Data

Figure 27. PPAK PC Board

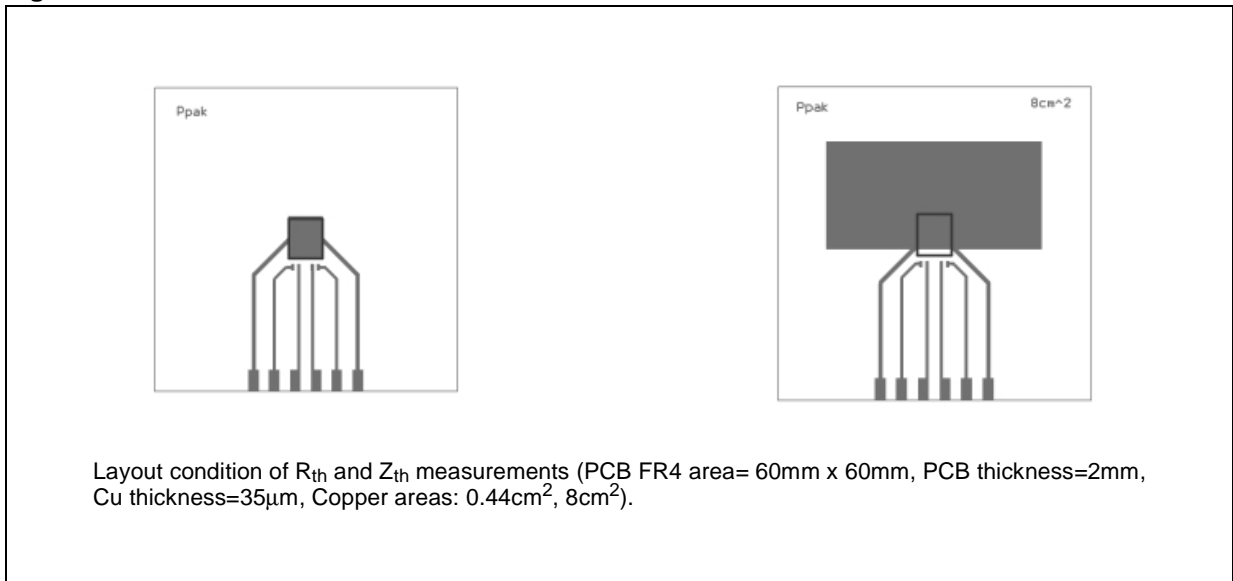


Figure 28. PPAK $R_{thj-amb}$ Vs PCB copper area in open box free air condition

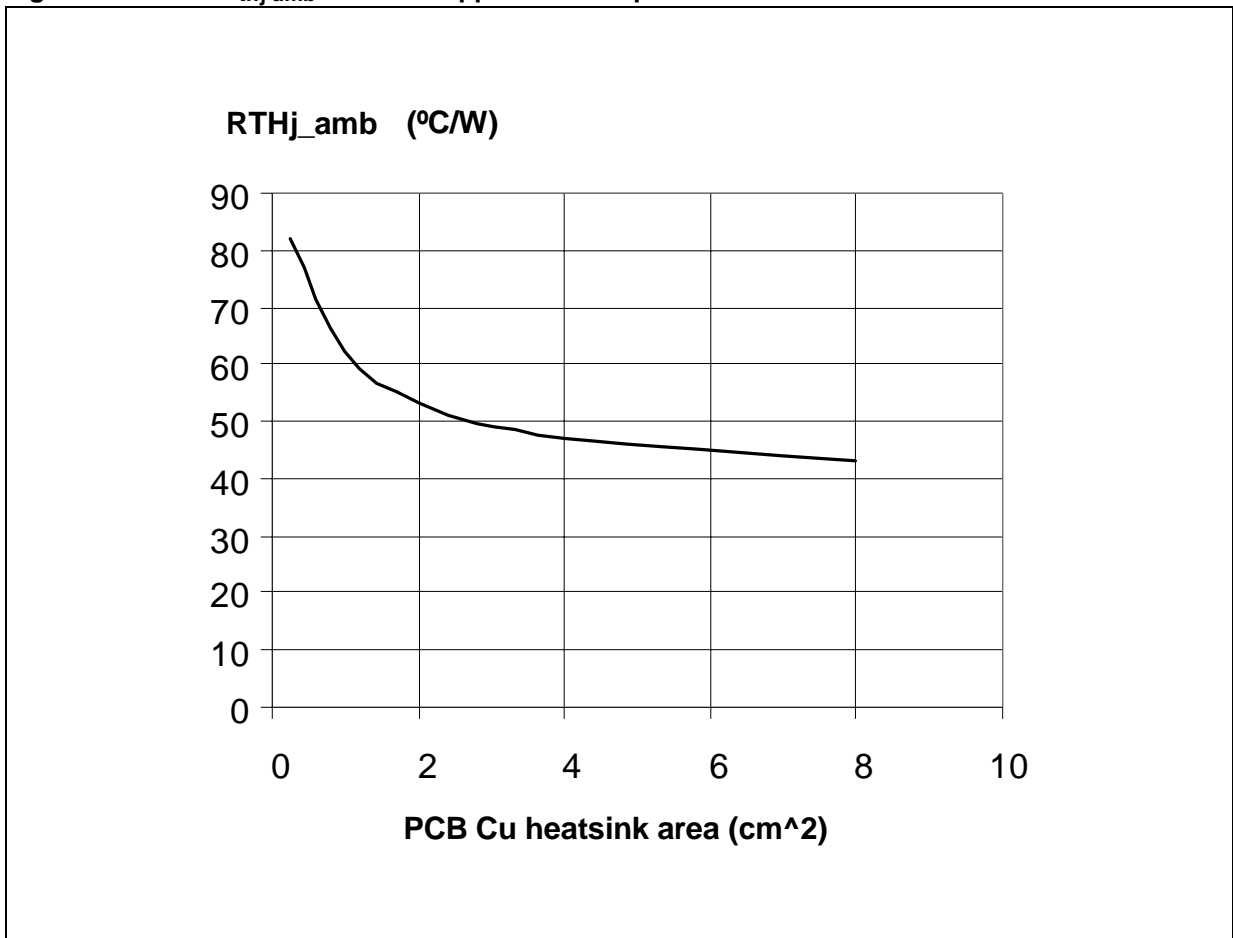


Figure 29. SO-8 Thermal Impedance Junction Ambient Single Pulse

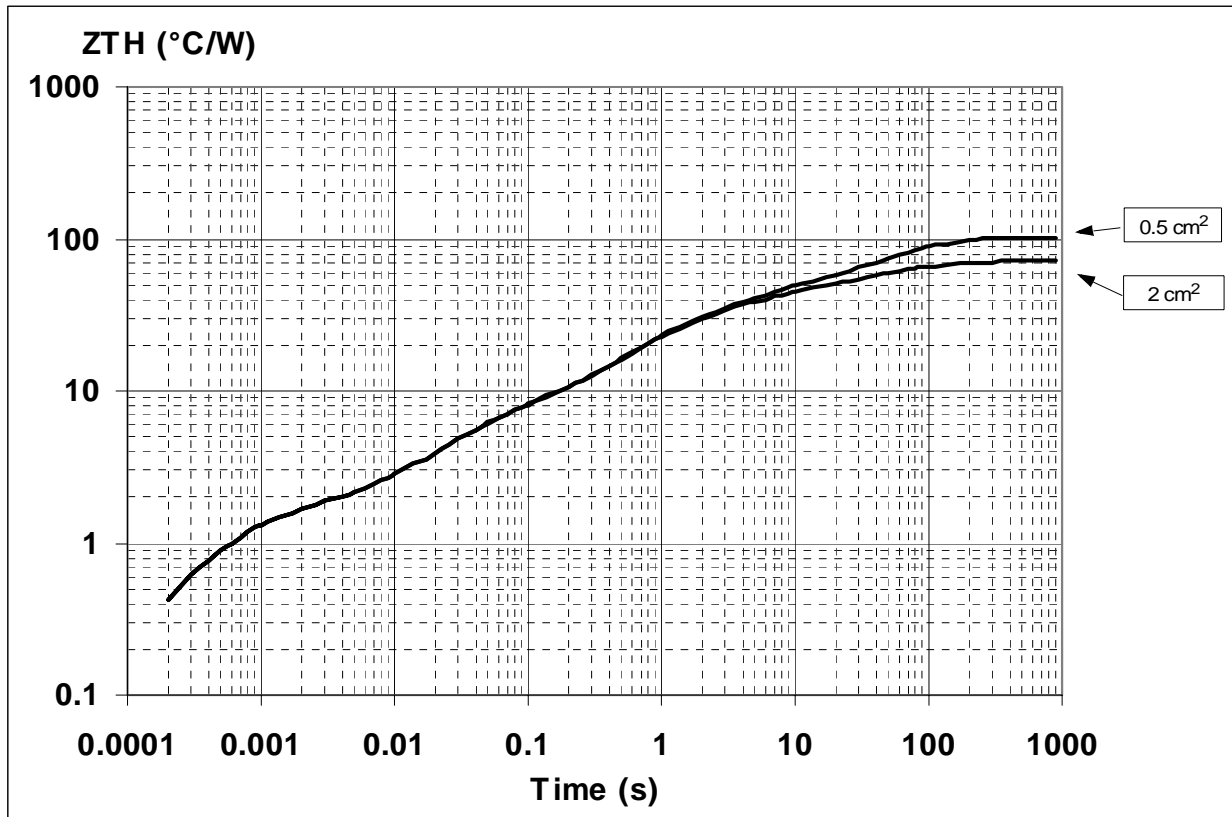
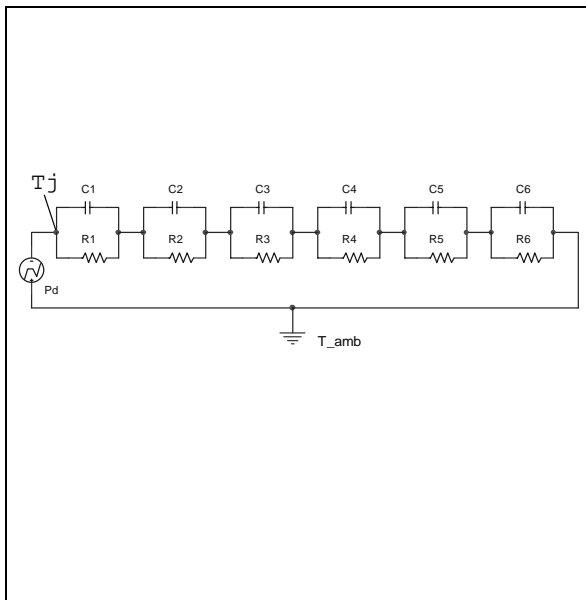


Figure 30. Thermal fitting model of a single channel HSD in SO-8



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 13. Thermal Parameter

Area/island (cm ²)	0.14	2
R1 (°C/W)	0.24	
R2 (°C/W)	1.2	
R3 (°C/W)	4.5	
R4 (°C/W)	21	
R5 (°C/W)	16	
R6 (°C/W)	58	28
C1 (W.s/°C)	0.00015	
C2 (W.s/°C)	0.0005	
C3 (W.s/°C)	7.50E-03	
C4 (W.s/°C)	0.045	
C5 (W.s/°C)	0.35	
C6 (W.s/°C)	1.05	2

Figure 31. PPAK Thermal Impedance Junction Ambient Single Pulse

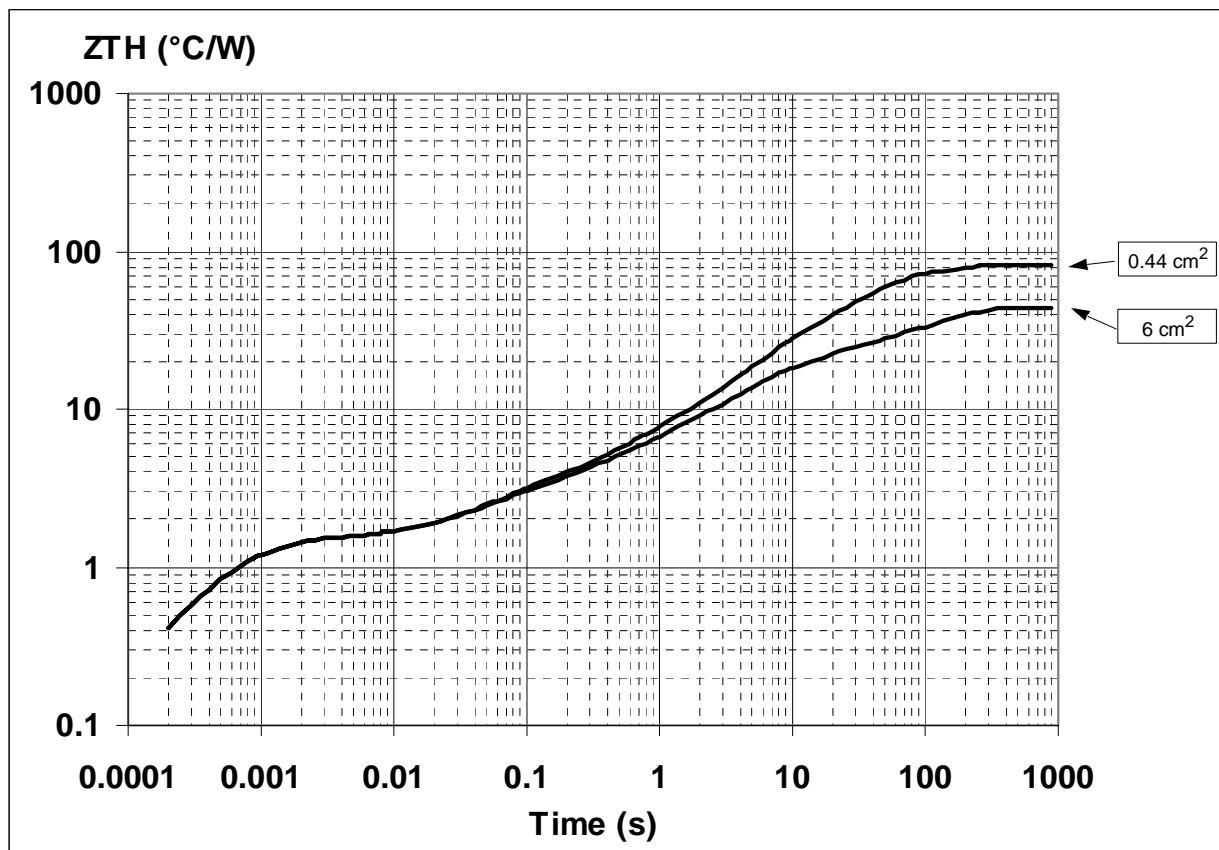
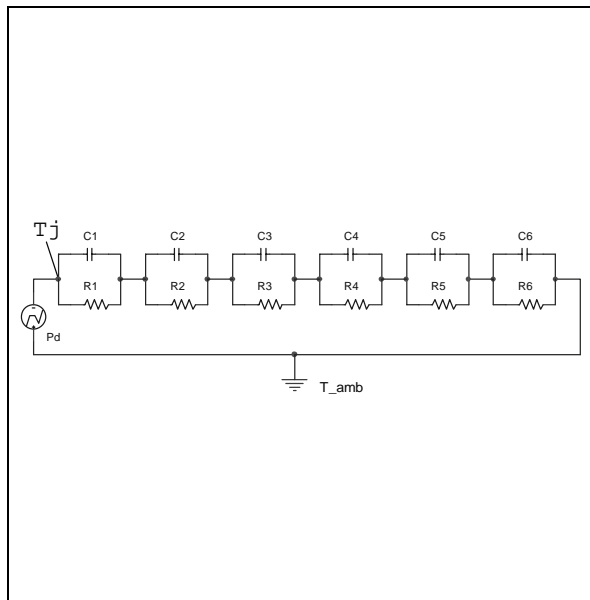


Figure 32. Thermal fitting model of a single channel HSD in PPAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 14. Thermal Parameter

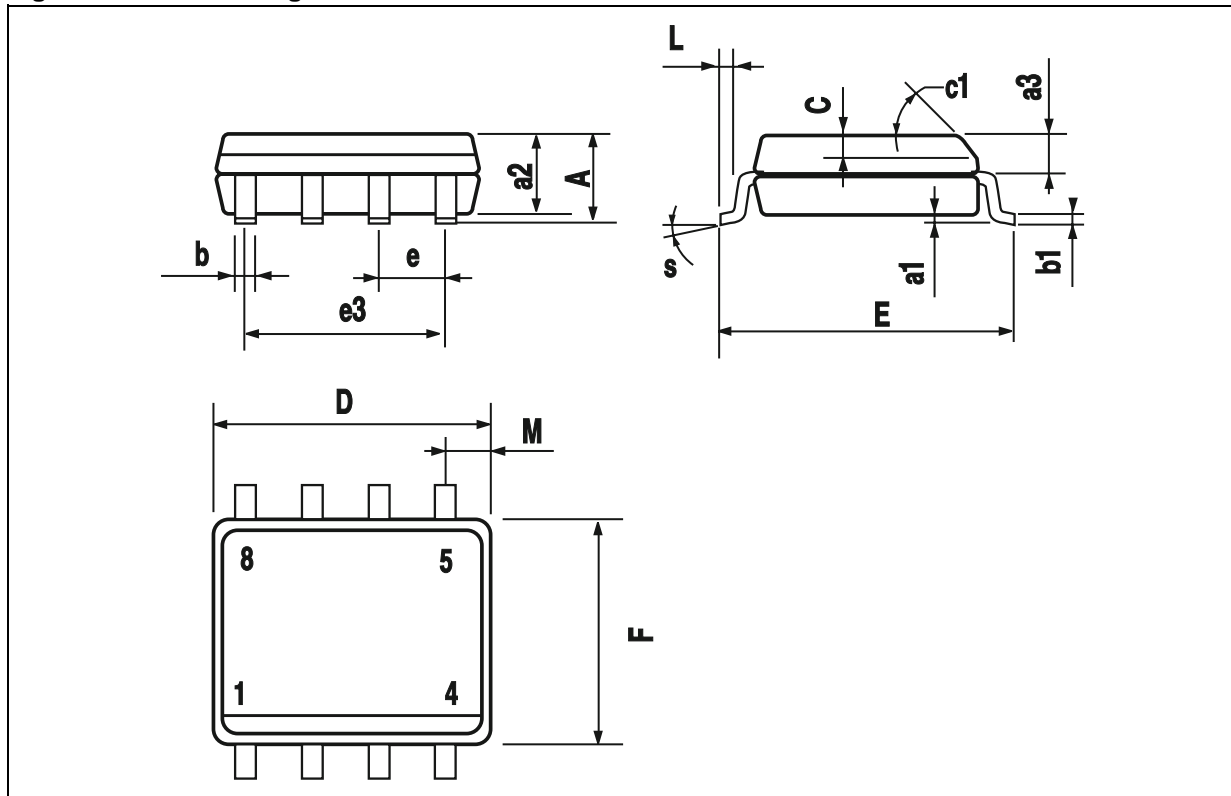
Area/island (cm ²)	0.44	6
R1 (°C/W)	0.04	
R2 (°C/W)	0.25	
R3 (°C/W)	0.3	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0008	
C2 (W.s/°C)	0.007	
C3 (W.s/°C)	0.02	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

PACKAGE MECHANICAL

Table 15. SO-8 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A			1.75
a1	0.1		0.25
a2			1.65
a3	0.65		0.85
b	0.35		0.48
b1	0.19		0.25
C	0.25		0.5
c1	45 (typ.)		
D	4.8		5
E	5.8		6.2
e		1.27	
e3		3.81	
F	3.8		4
L	0.4		1.27
M			0.6
S	8 (max.)		
L1	0.8		1.2

Figure 33. SO-8 Package Dimensions



PACKAGE MECHANICAL

Table 16. PPAK Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.40		0.60
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D1		5.1	
D	6.00		6.20
E	6.40		6.60
E1		4.7	
e		1.27	
G	4.90		5.25
G1	2.38		2.70
H	9.35		10.10
L2		0.8	1.00
L4	0.60		1.00
R		0.2	
V2	0°		8°
Package Weight	Gr. 0.3		

Figure 34. PPAK Package Dimensions

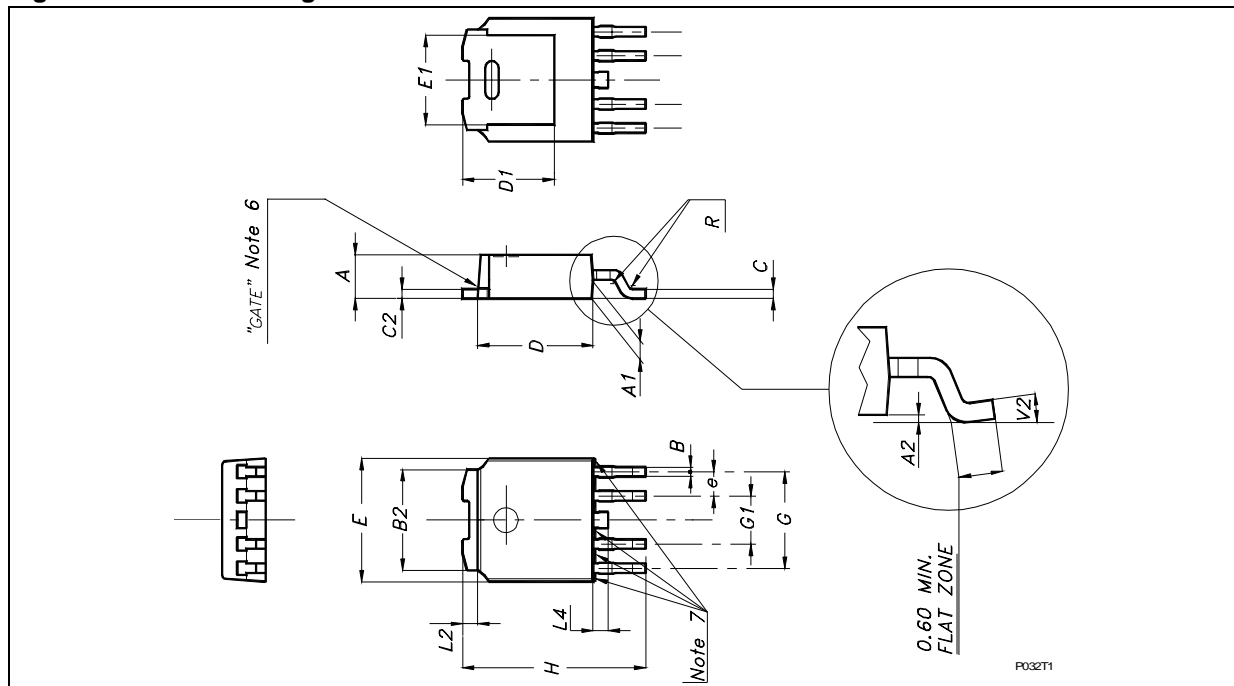


Figure 35. SO-8 Tube Shipment (no suffix)

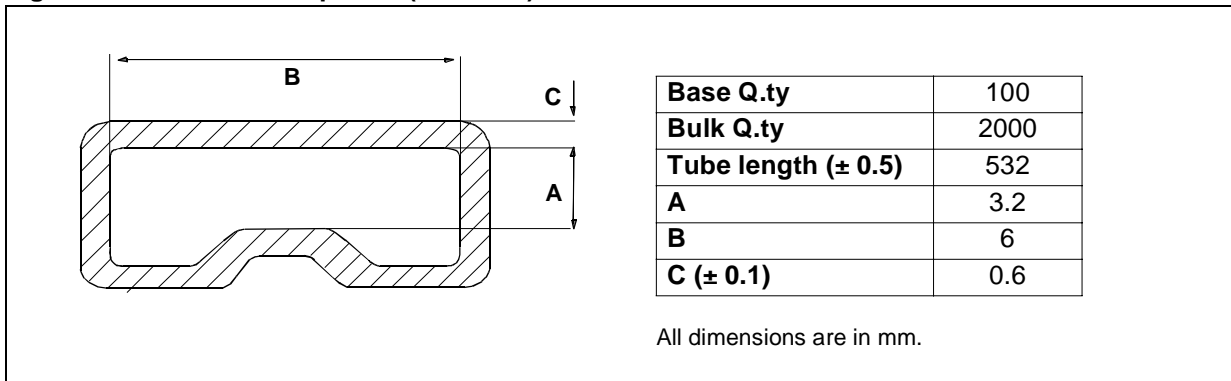


Figure 36. SO-8 Tape And Reel Shipment (suffix "TR")

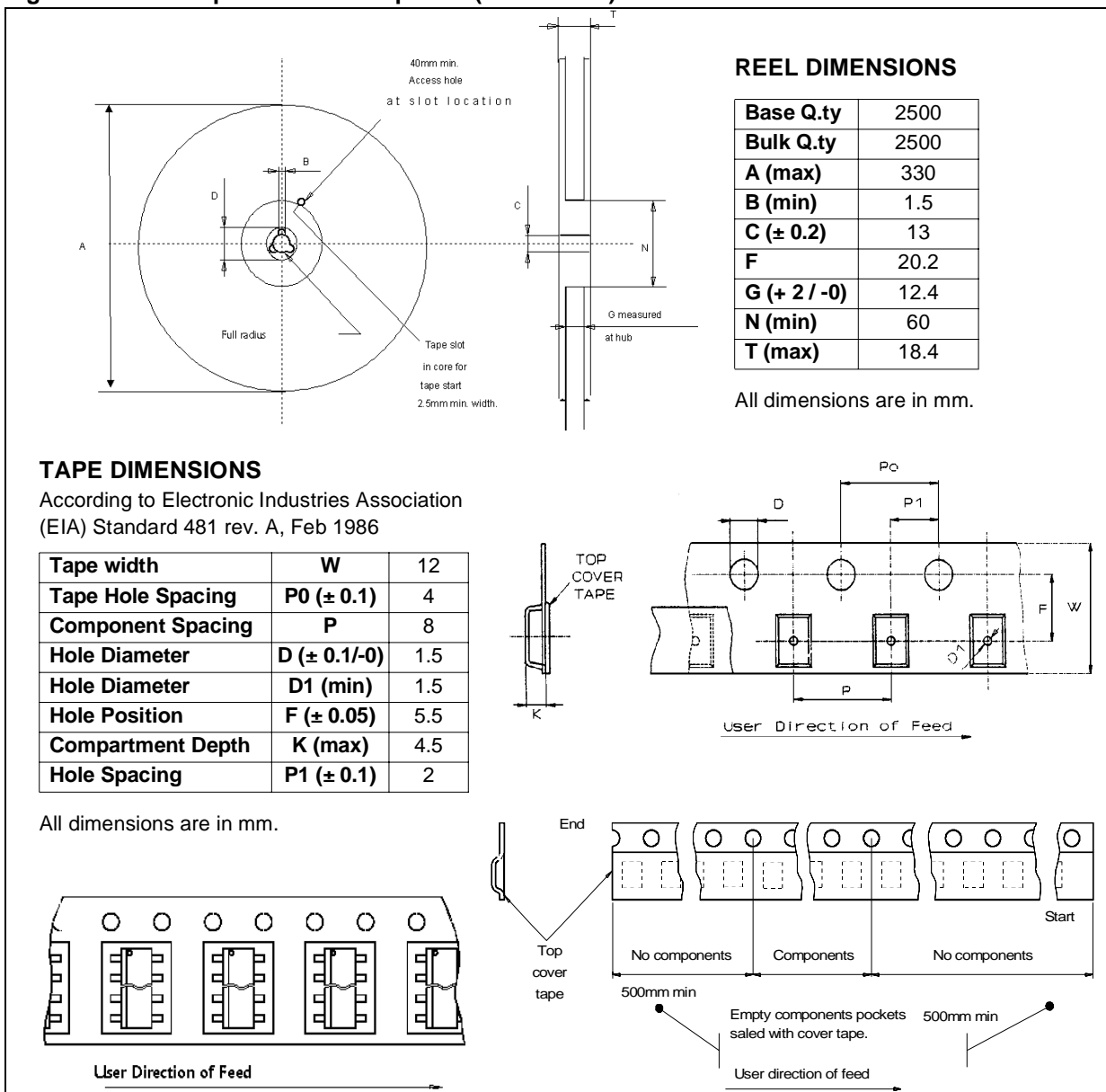


Figure 37. PPAK Suggested Pad Layout and Tube Shipment (no suffix)

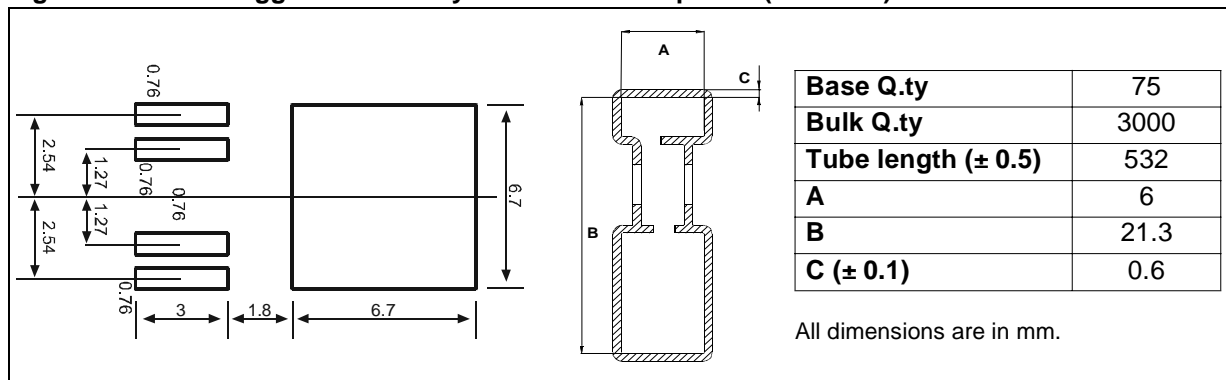
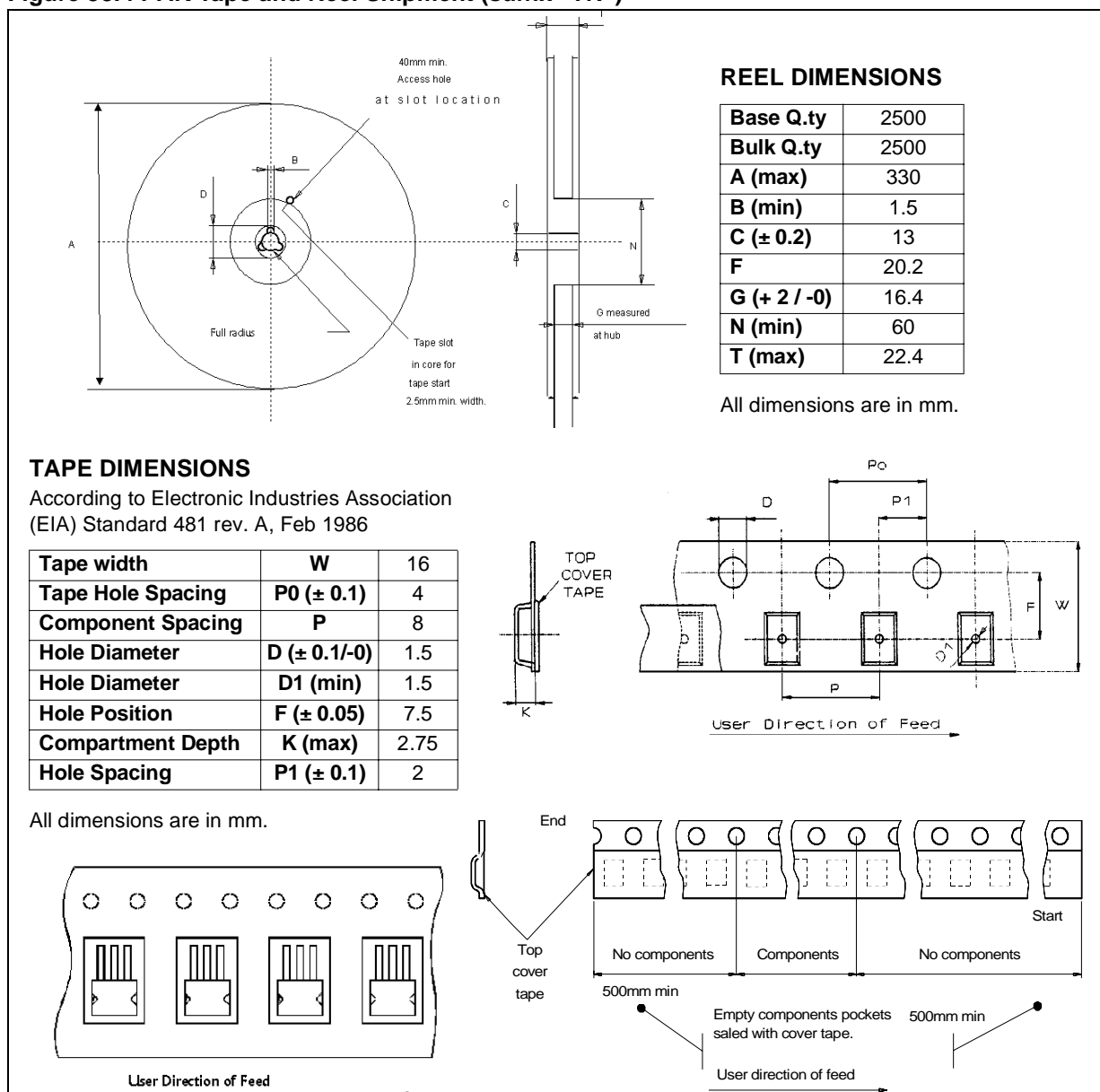


Figure 38. PPAK Tape and Reel Shipment (suffix "TR")



REVISION HISTORY**Table 17. Revision History**

Date	Revision	Description of Changes
Oct. -2004	1	- First Issue

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