



VN750 VN750S / VN750-B5

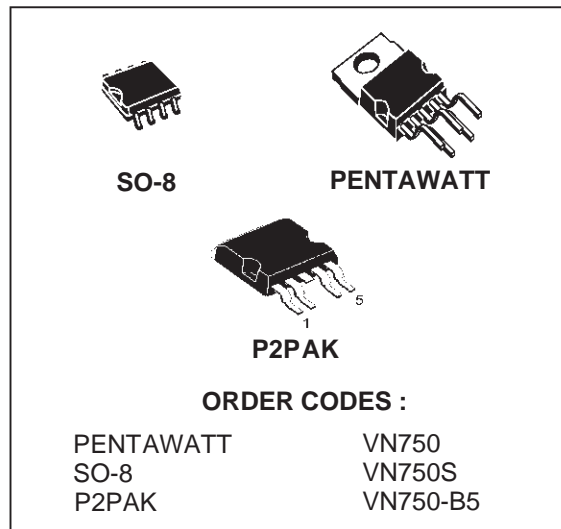
HIGH SIDE DRIVER

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN750			
VN750S	60 m Ω	6 A	36 V
VN750-B5			

- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (*)

DESCRIPTION

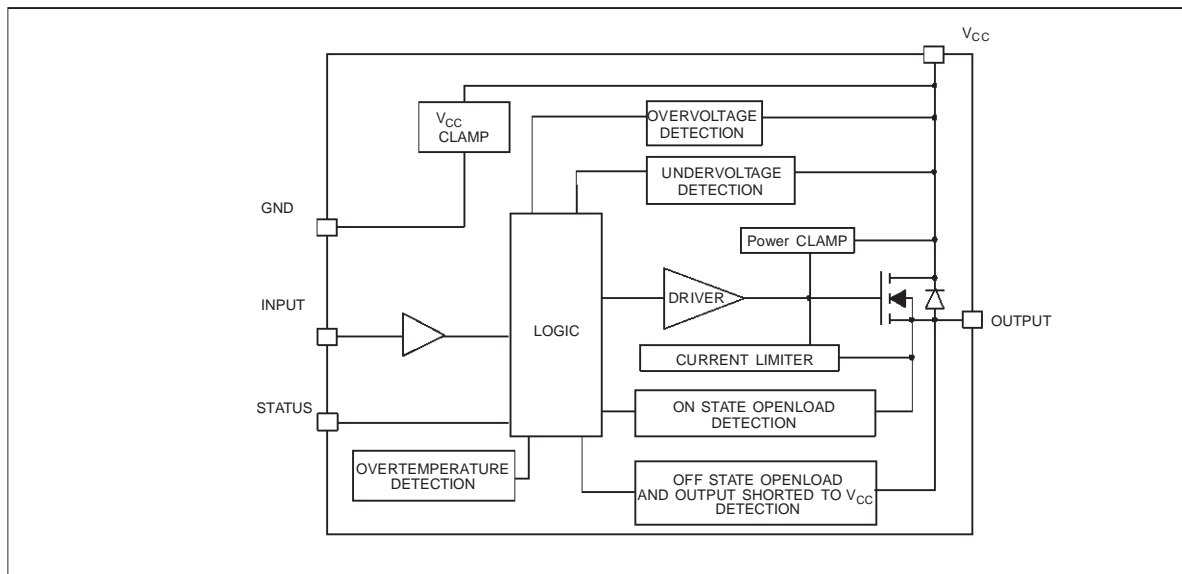
The VN750, VN750S, VN750-B5 are a monolithic device designed in STMicroelectronics VIPower Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation



combined with thermal shutdown and automatic restart protect the device against overload.

The device detects open load condition both is on and off state. Output shorted to V_{CC} is detected in the off state. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM



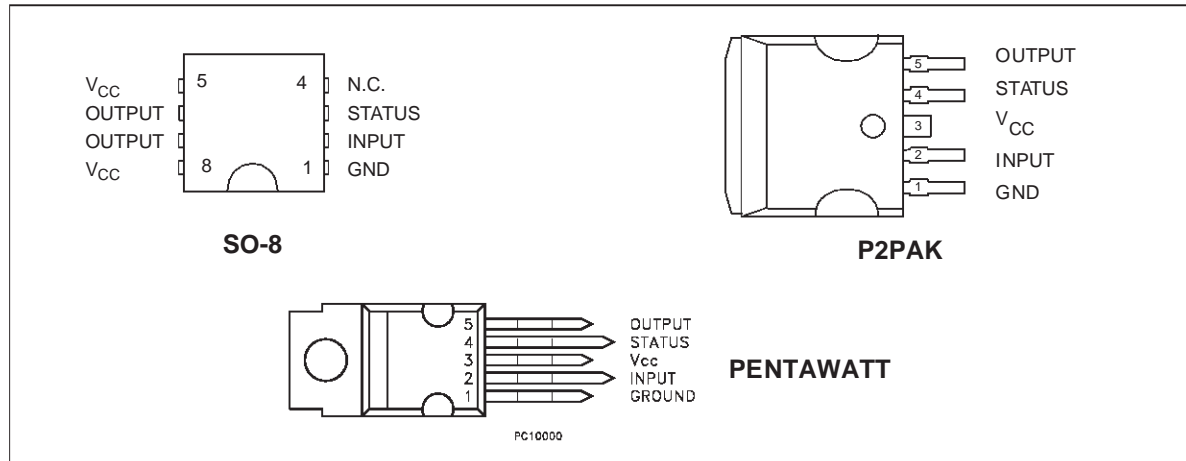
(*) See application schematic at page 8

VN750 / VN750S / VN750-B5

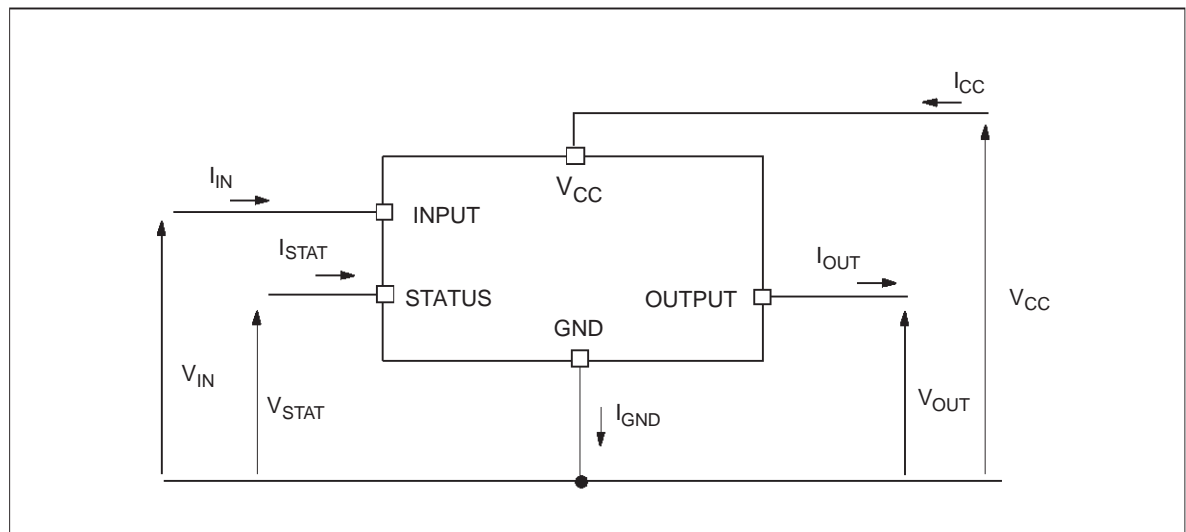
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value			Unit
		SO-8	PENTAWATT	P2PAK	
V_{CC}	DC Supply Voltage	41			V
$-V_{CC}$	Reverse DC Supply Voltage	- 0.3			V
$-I_{gnd}$	DC Reverse Ground Pin Current	- 200			mA
I_{OUT}	DC Output Current	Internally Limited			A
$-I_{OUT}$	Reverse DC Output Current	- 6			A
I_{IN}	DC Input Current	+/- 10			mA
I_{STAT}	DC Status Current	+/- 10			mA
V_{ESD}	Electrostatic Discharge (R=1.5KΩ; C=100pF)	2000			V
P_{tot}	Power Dissipation $T_C=25^{\circ}C$	3.1	42	42	W
T_j	Junction Operating Temperature	Internally Limited			$^{\circ}C$
T_c	Case Operating Temperature	- 40 to 150			$^{\circ}C$
T_{stg}	Storage Temperature	- 55 to 150			$^{\circ}C$

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter		Value			Unit
			S0-8	PENTAWATT	P2PAK	
R _{thj-pins}	Thermal Resistance Junction-pins	Max	40	-	-	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	120	60	60	°C/W
R _{thj-case}	Thermal Resistance Junction-case	Max	-	3	3	°C/W

ELECTRICAL CHARACTERISTICS (8V < V_{CC} < 36V; -40°C < T_j < 150°C unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CC}	Operating Supply Voltage		5.5	13	36	V
V _{USD}	Under Voltage Shut-down		3	4	5.5	V
V _{USDhyst}	Under Voltage Shut-down Hysteresis			0.5		V
V _{OV}	Overvoltage Shut-down		36	(*)	48	V
R _{ON}	On State Resistance	I _{OUT} =2A; T _j =25°C; V _{CC} >8V		(*)	60	mΩ
		I _{OUT} =2A; V _{CC} >8V			120	mΩ
I _S	Supply Current	Off State; V _{CC} =13V		10	25	μA
		On State; V _{CC} =13V		2	3.5	mA
I _{L(off1)}	Off State Output Current	V _{IN} =V _{OUT} =0V	0	(*)	50	μA
I _{L(off2)}	Off State Output Current	V _{IN} =0V; V _{OUT} =3.5V	-75		0	μA

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t _{d(on)}	Turn-on Delay Time	R _L =6.5Ω from V _{IN} rising edge to V _{OUT} =1.3V		40		μs
t _{d(off)}	Turn-off Delay Time	R _L =6.5Ω from V _{IN} falling edge to V _{OUT} =11.7V		30		μs
dV _{OUT} /dt _(on)	Turn-on Voltage Slope	R _L =6.5Ω from V _{OUT} =1.3V to V _{OUT} =10.4V		(*)		V/μs
dV _{OUT} /dt _(off)	Turn-off Voltage Slope	R _L =6.5Ω from V _{OUT} =11.7V to V _{OUT} =1.3V		(*)		V/μs

INPUT PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{IL}	Input Low Level			(*)	1.25	V
I _{IL}	Low Level Input Current	V _{IN} =1.25V	1	(*)		μA
V _{IH}	Input High Level		3.25	(*)		V
I _{IH}	High Level Input Current	V _{IN} =3.25V		(*)	10	μA
V _{hyst}	Input Hysteresis Voltage		0.5	(*)		V
V _{ICL}	Input Clamp Voltage	I _{IN} =1mA	6.5	(*)	8.5	V
		I _{IN} =-1mA		-0.7		V

(*) See curves at pages 9, 10, 11

ELECTRICAL CHARACTERISTICS (continued)
STATUS PIN

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	$I_{STAT}=1.6mA$		(*)	0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation $V_{STAT}=5V$		(*)	10	μA
C_{STAT}	Status Pin Input Capacitance	Normal Operation $V_{STAT}=5V$			100	pF
V_{SCL}	Status Clamp Voltage	$I_{STAT}=1mA$	6.5	(*)	8.5	V
		$I_{STAT}=-1mA$		-0.7		V

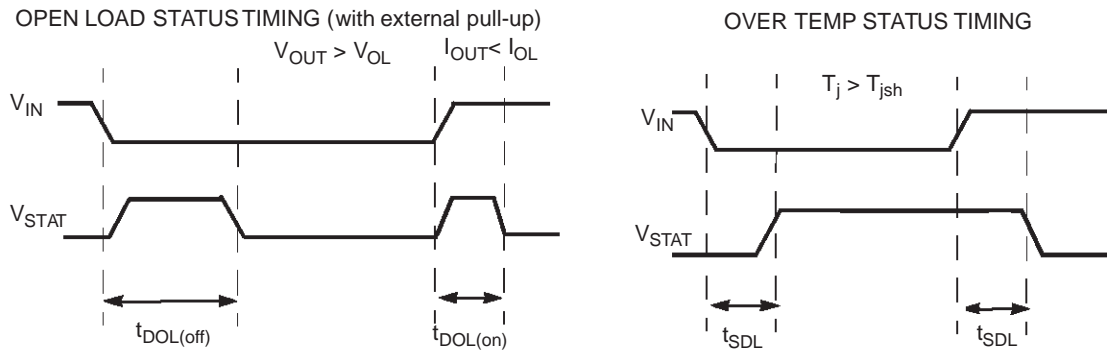
PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	$^{\circ}C$
T_R	Reset Temperature		135			$^{\circ}C$
T_{hyst}	Thermal Hysteresis		7	15		$^{\circ}C$
t_{SDL}	Status delay in overload condition	$T_j > T_{jsh}$			20	μs
I_{lim}	Current limitation	$9V < V_{CC} < 36V$	6	9	15	A
		$5V < V_{CC} < 36V$			15	A
V_{demag}	Turn-off Output Clamp Voltage	$I_{OUT}=2A; V_{IN}=0V; L=6mH$	VCC-41	VCC-48	VCC-55	V

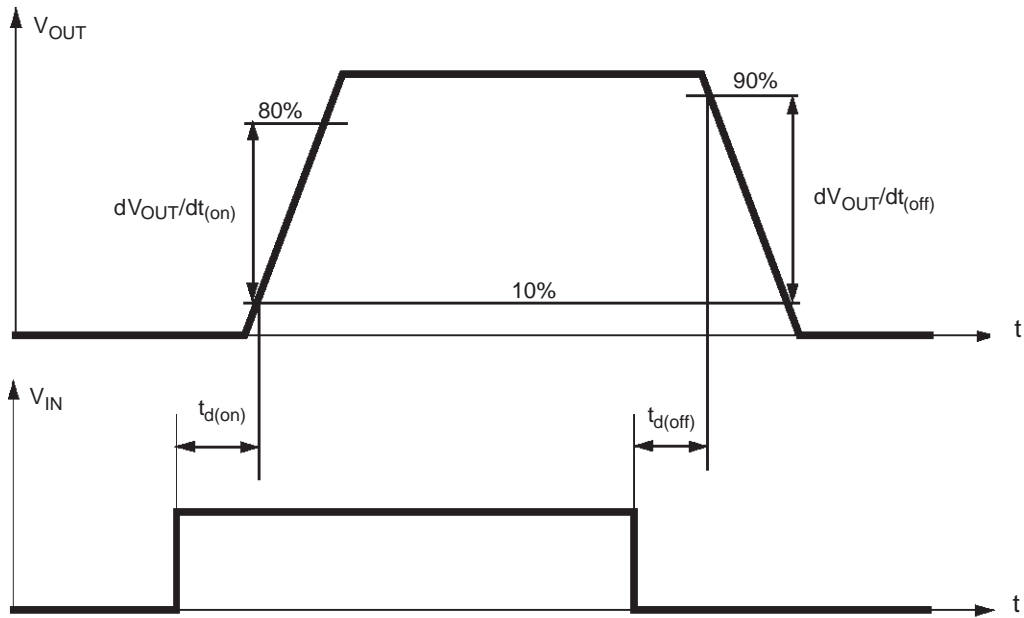
OPENLOAD DETECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	$V_{IN}=5V$	50	(*)	200	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	$I_{OUT}=0A$			200	μs
V_{OL}	Openload OFF State Voltage Detection Threshold	$V_{IN}=0V$	1.5	(*)	3.5	V
$t_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	μs

(*) See curves at pages 9, 10, 11



Switching time Waveforms



TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output Voltage > V _{OL}	L	H	L
	H	H	H
Output Current < I _{OL}	L	L	H
	H	H	L

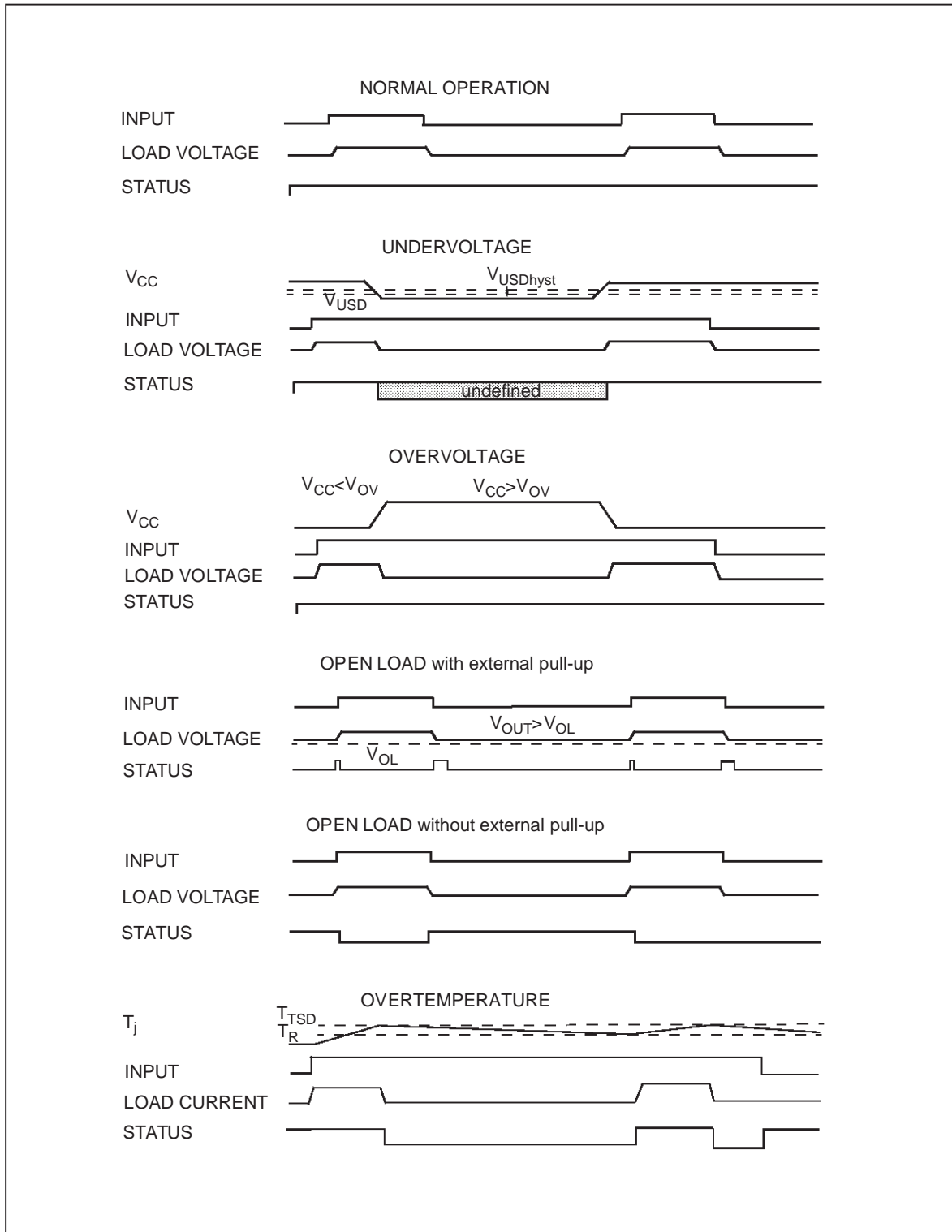
ELECTRICAL TRANSIENT REQUIREMENTS ON V_{CC} PIN

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

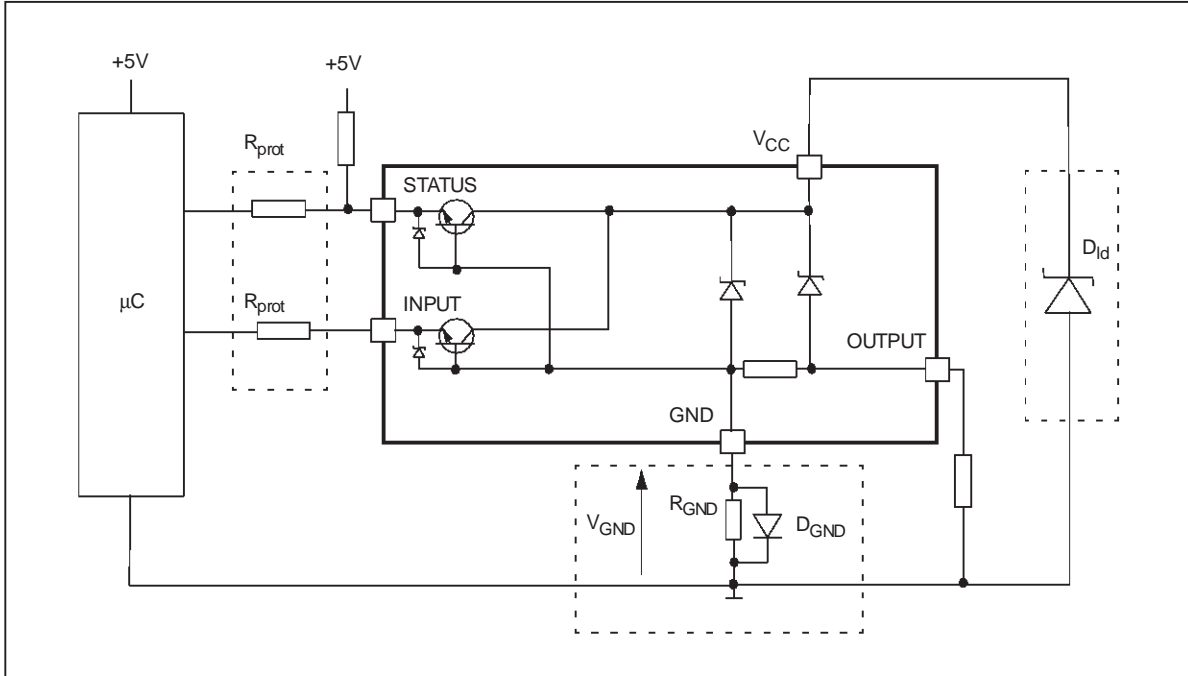
ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure1: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor ($R_{GND} = 1\text{k}\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j 600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{id} is necessary (Transil or MOV) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

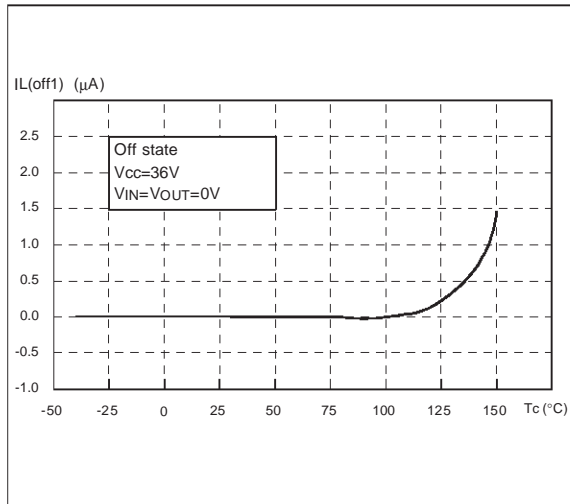
Calculation example:

For $V_{CCpeak} = -100\text{V}$ and $I_{latchup} \geq 20\text{mA}$; $V_{OH\mu C} \geq 4.5\text{V}$

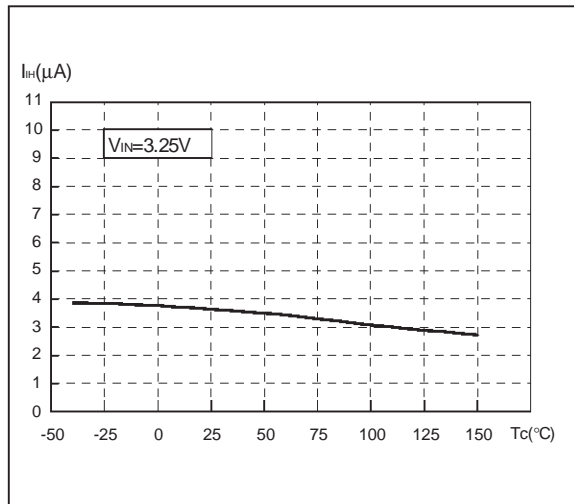
$$5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$$

Recommended R_{prot} value is 10k Ω .

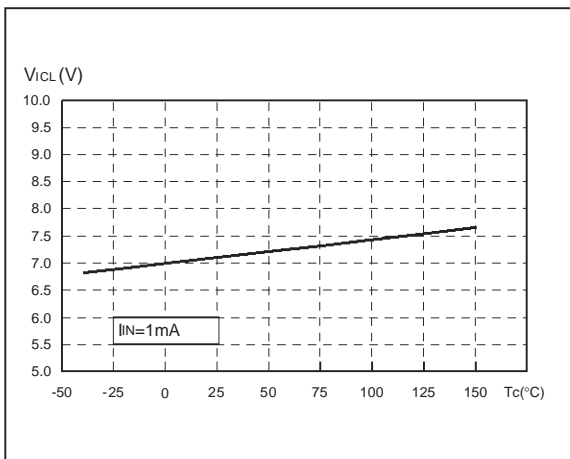
Off State Output Current



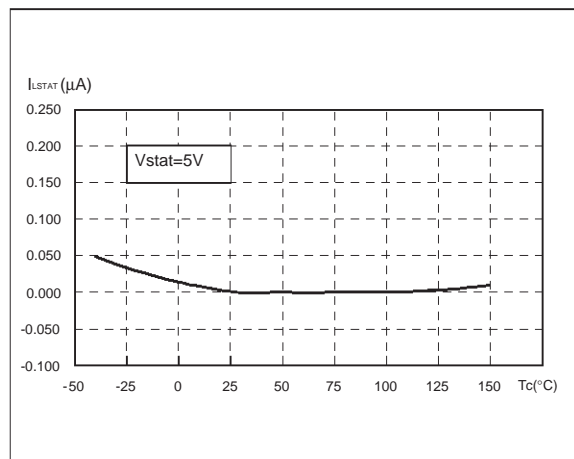
High Level Input Current



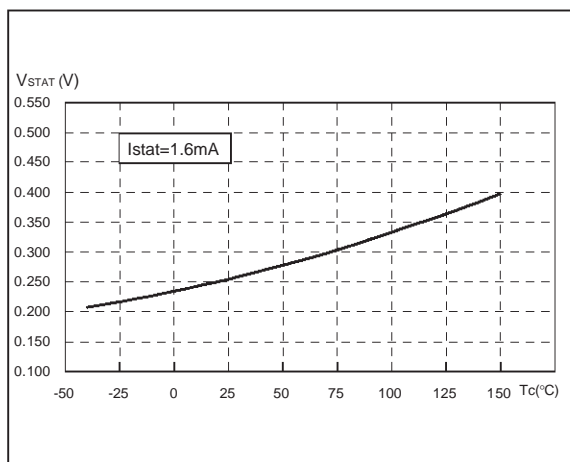
Input Clamp Voltage



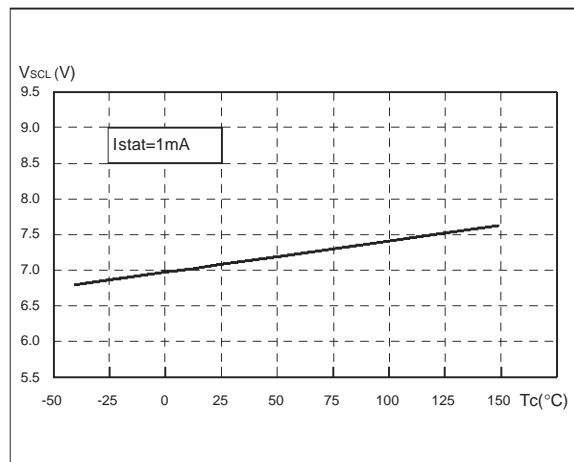
Status Leakage Current



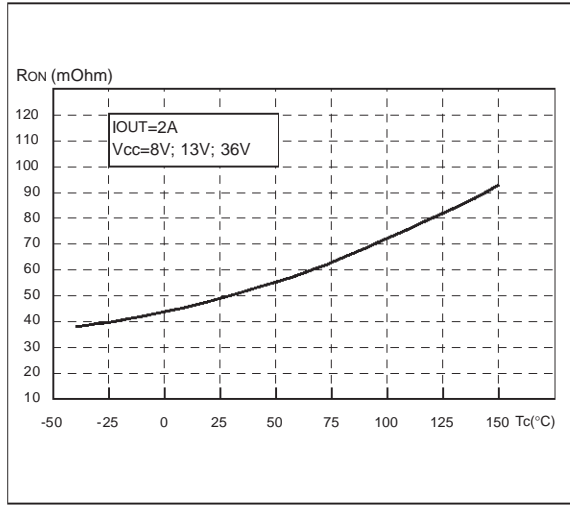
Status Low Output Voltage



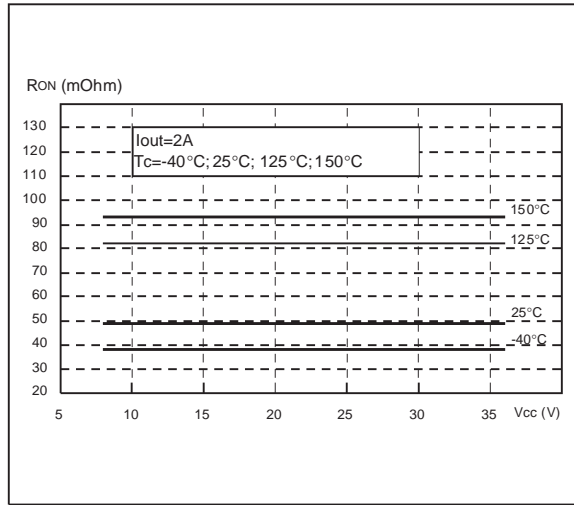
Status Clamp Voltage



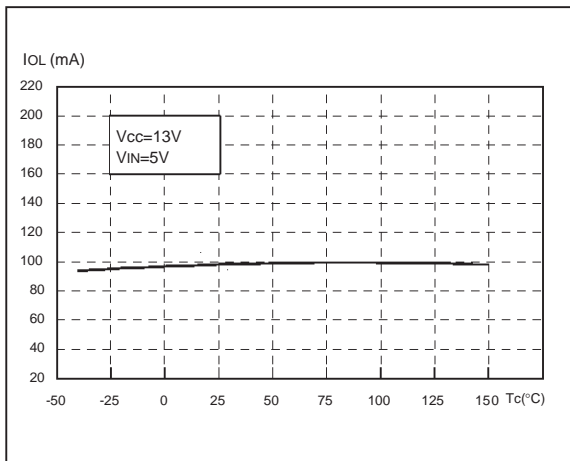
On State Resistance Vs T_{case}



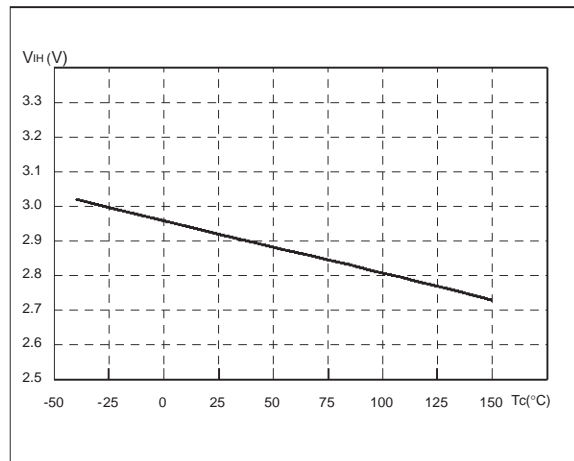
On State Resistance Vs V_{CC}



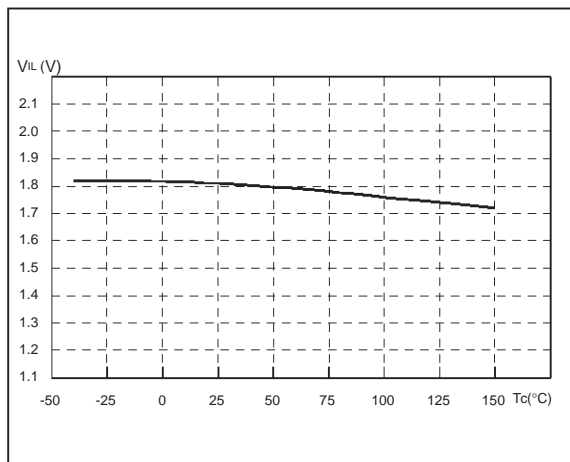
Openload On State Detection Threshold



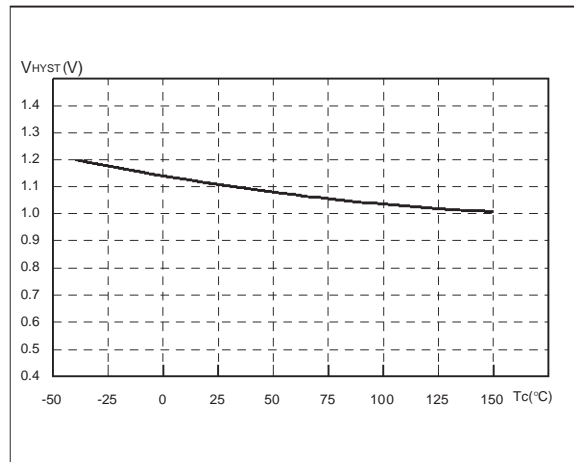
Input High Level



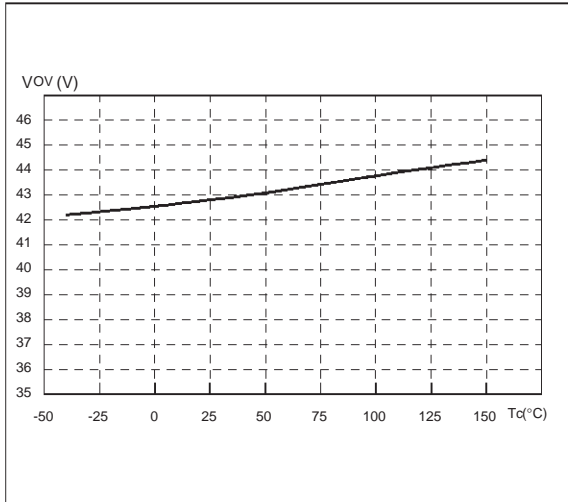
Input Low Level



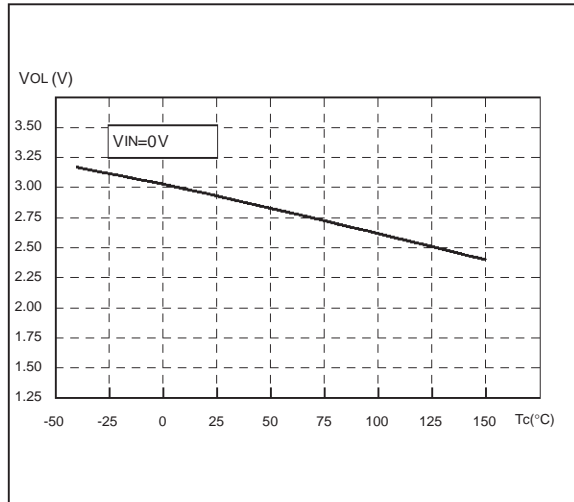
Input Hysteresis Voltage



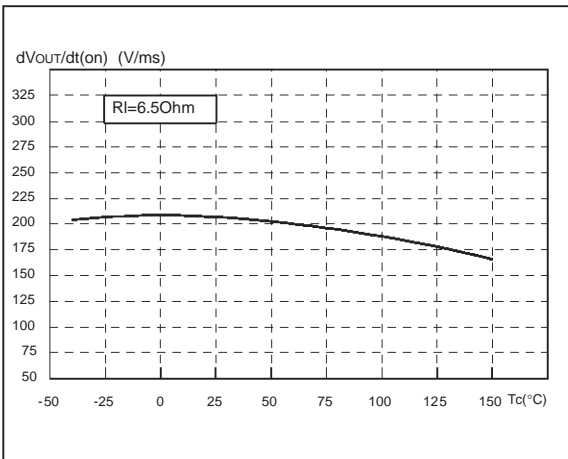
Overvoltage Shutdown



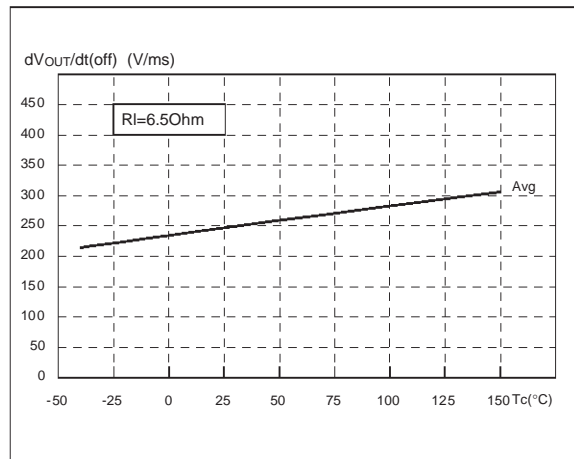
Openload Off State Voltage Detection Threshold



Turn-on Voltage Slope

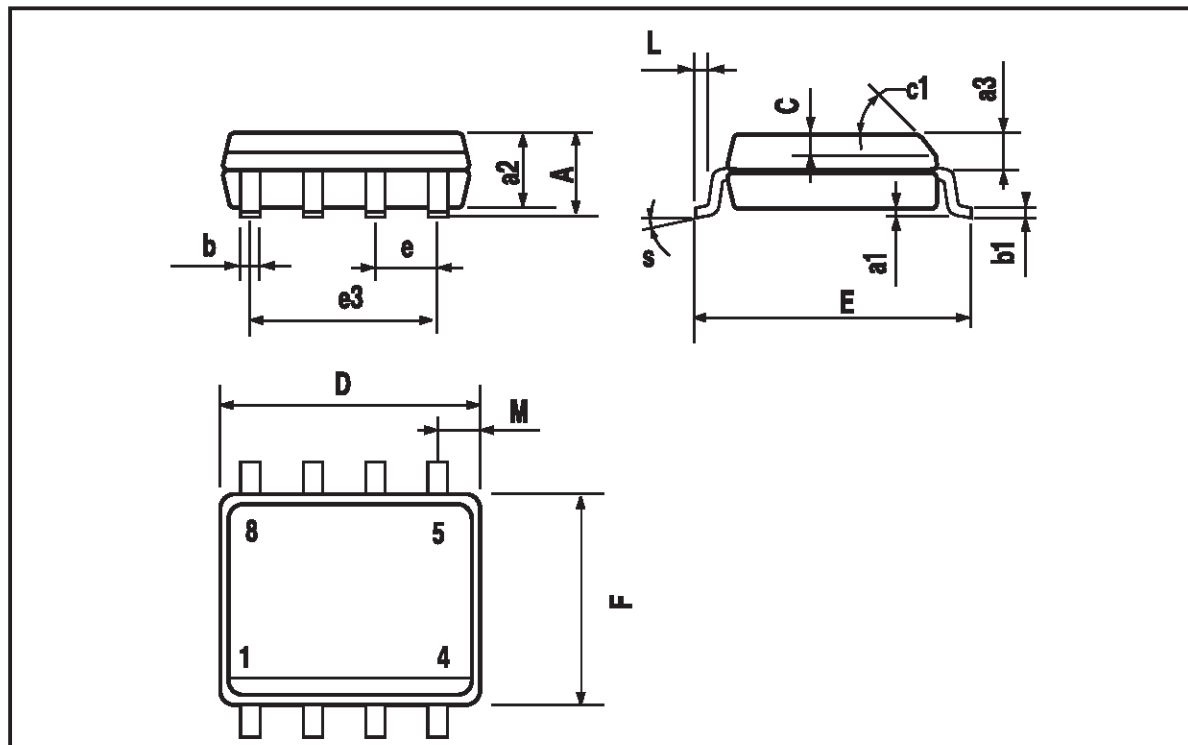


Turn-off Voltage Slope



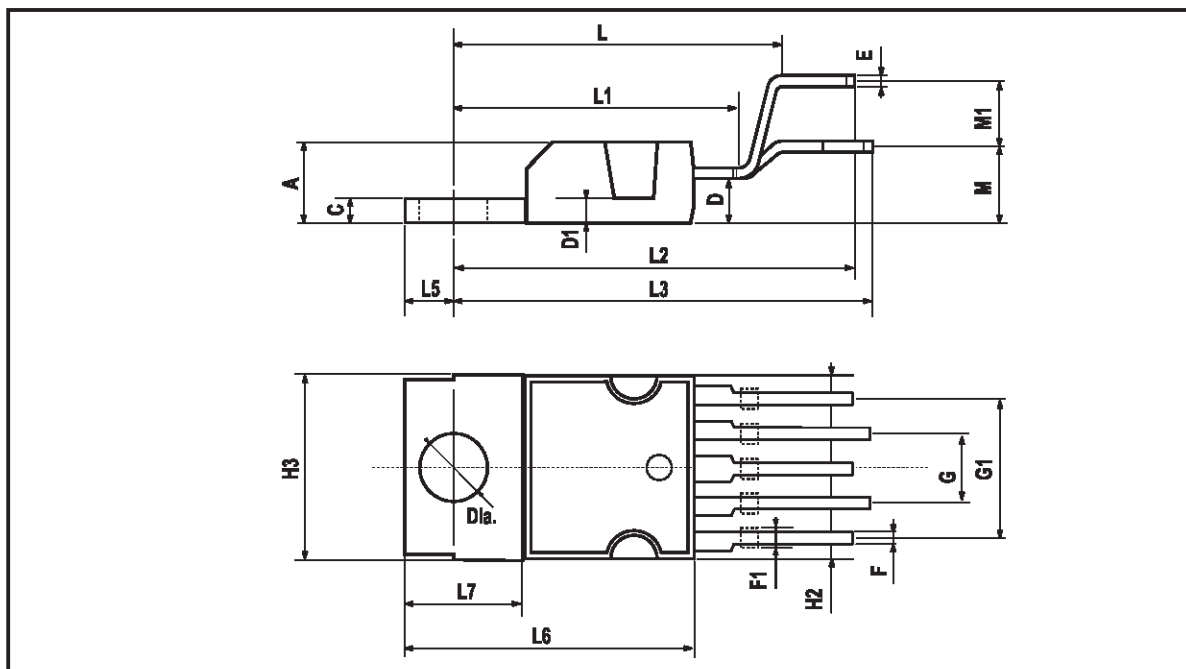
SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					
L1	0.8		1.2	0.031		0.047



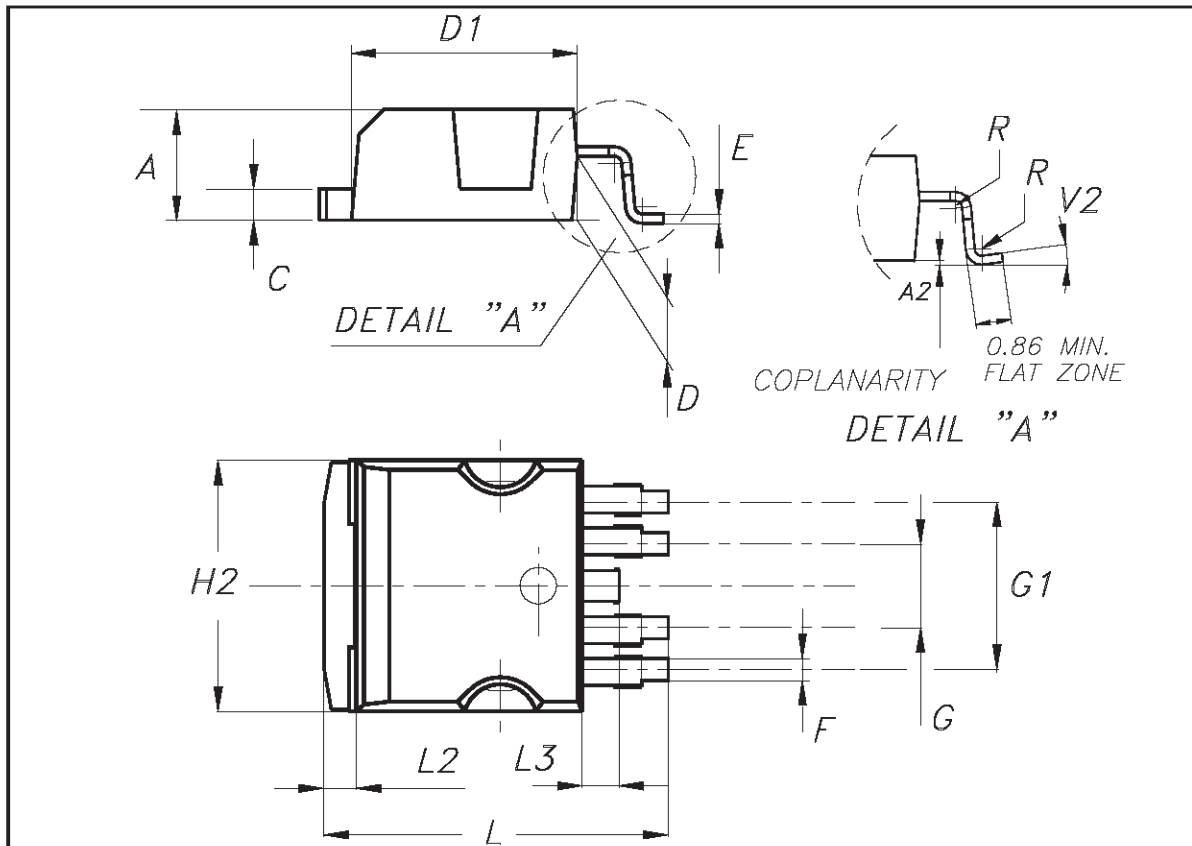
PENTAWATT (VERTICAL) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G	3.2	3.4	3.6	0.126	0.134	0.142
G1	6.6	6.8	7	0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Diam.	3.65		3.85	0.144		0.152



P2PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.30		4.80			
A2	0.03		0.23			
C	1.17		1.37			
D	2.40		2.80			
D1	8.95		9.35			
E	0.35		0.55			
F	0.80		1.05			
G	3.20		3.60			
G1	6.60		7.00			
H2			10.40			
L	13.59		14.39			
L2	1.27		1.40			
L3	1.30		1.70			
R		0.30				
V2	0 d		8 d			



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics. The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics - Printed in ITALY- All Rights Reserved.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta -
Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>