

# STS4C3F60L N-CHANNEL 60V - 0.045 Ω - 4A SO-8 P-CHANNEL 60V - 0.100 Ω - 3A SO-8 StripFET™ MOSFET

#### **Table 1: General Features**

ТҮРЕ	V <sub>DSS</sub>	R <sub>DS(on)</sub>	Ι <sub>D</sub>
STS4C3F60L (N-Channel)		< 0.055 Ω	4 A
STS4C3F60L (P-Channel)		< 0.120 Ω	3 A

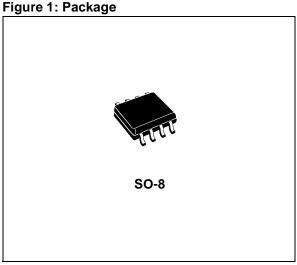
- TYPICAL R<sub>DS(on)</sub> (N-Channel) = 0.045 Ω
- TYPICAL  $R_{DS(on)}$  (P-Channel) = 0.100  $\Omega$
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

#### DESCRIPTION

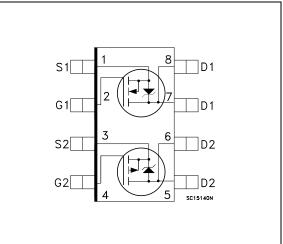
This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low onresistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

#### **APPLICATIONS**

- DC/DC CONVERTERS
- BACK LIGHT INVERTER FOR LCD



#### Figure 2: Internal Schematic Diagram



#### Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STS4C3F60L	S4C3F60L	SO-8	TAPE & REEL

#### STS4C3F60L

#### **Table 3: Absolute Maximum ratings**

Symbol	Parameter	Val	Value			
		N-CHANNEL	P-CHANNEL			
V <sub>DS</sub>	Drain-source Voltage ( $V_{GS} = 0$ )	6	0	V		
V <sub>DGR</sub>	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	6	0	V		
V <sub>GS</sub>	Gate-source Voltage	urce Voltage ± 16		V		
Ι <sub>D</sub>	Drain Current (continuous) at $T_C = 25^{\circ}C$ Single Operating	4	3	Α		
ID	Drain Current (continuous) at T <sub>C</sub> = 100°C Single Operating	2.5	1.9	A		
I <sub>DM</sub> (•)	Drain Current (pulsed)	16	12	Α		
P <sub>TOT</sub>	Total Dissipation at $T_C = 25^{\circ}C$ 2		W			
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature -55 to 150			°C		

(•) Pulse width limited by safe operating area

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

#### **Table 4: Thermal Data**

Rthj-amb (1)	Thermal Resistance Junction-ambient	62.5	°C/W	l
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(1) When mounted on 1 inch² pad of 2 oz. copper,  $t \leq 10 \mbox{ s}$ 

# **ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED) Table 5: On/Off

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, V_{GS} = 0$	n-ch p-ch	60 60			V V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125°C	n-ch p-ch			1 10	μA μA
IGSS	Gate-body Leakage Current (V <sub>DS</sub> = 0)	$V_{GS}$ = ± 16V $V_{GS}$ = ± 16V	n-ch p-ch			±100 ±100	nA nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_{D}$ = 250 µA	n-ch p-ch	1 1.5			V V
R <sub>DS(on)</sub>	Static Drain-source On Resistance		n-ch p-ch n-ch p-ch		0.045 0.100 0.050 0.130	0.055 0.120 0.065 0.160	Ω Ω Ω

#### **Table 6: Dynamic**

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 2 A V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3 A	n-ch p-ch		7 7.2		S S
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25V$ , f = 1 MHz, $V_{GS} = 0$	n-ch p-ch		1030 630		pF pF
$C_{\text{oss}}$	Output Capacitance		n-ch p-ch		140 121		pF pF
C <sub>rss</sub>	Reverse Transfer Capacitance		n-ch p-ch		40 49		pF pF

(1) Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5%

## **ELECTRICAL CHARACTERISTICS** (CONTINUED) **Table 7: Switching On**

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	$\label{eq:VDD} \begin{array}{l} \mbox{N-CHANNEL} \\ \mbox{V}_{DD} = 30 \mbox{ V}, \mbox{ I}_{D} = 2 \mbox{ A}, \\ \mbox{R}_{G} = 4.7 \ \Omega, \mbox{ V}_{GS} = 4.5 \mbox{ V} \end{array}$	n-ch p-ch		15 124		ns ns
tr	Rise Time	$\label{eq:p-channel} \begin{array}{l} \textbf{P-CHANNEL} \\ \textbf{V}_{DD} = 30 \text{ V}, \text{ I}_{D} = 1.5 \text{ A}, \\ \textbf{R}_{G} = 4.7 \ \Omega, \ \textbf{V}_{GS} = 4.5 \text{ V} \\ (\text{Resistive Load see, Figure 28}) \end{array}$	n-ch p-ch		28 54		ns ns
Qg	Total Gate Charge	<b>N-CHANNEL</b> V <sub>DD</sub> = 48 V, I <sub>D</sub> = 4 A, V <sub>GS</sub> = 4.5 V	n-ch p-ch		15 11.6	20.4 15.7	nC nC
Q <sub>gs</sub>	Gate-Source Charge	<b>P-CHANNEL</b> V <sub>DD</sub> = 48 V, I <sub>D</sub> = 3 A,	n-ch p-ch		4 4.5		nC nC
Q <sub>gd</sub>	Gate-Drain Charge	$V_{GS} = 4.5 V$ (see, Figure 31)	n-ch p-ch		4 4.7		nC nC

#### Table 8: Switching Off

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
t <sub>d(off)</sub>	Turn-off Delay Time	<b>N-CHANNEL</b> V <sub>DD</sub> = 30 V, I <sub>D</sub> = 2 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 4.5 V	n-ch p-ch		45 39		ns ns
tŗ	Fall Time	P-CHANNEL $V_{DD} = 30 \text{ V}, I_D = 1.5 \text{ A},$ $R_G = 4.7 \Omega, V_{GS} = 4.5 \text{ V}$ (Resistive Load see, Figure 28)	n-ch p-ch		10 14.5		ns ns

#### Table 9: Source-Drain Diodef

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain Current		n-ch p-ch			4 3	A A
I <sub>SDM</sub> (2)	Source-drain Current (pulsed)		n-ch p-ch			16 12	A A
V <sub>SD</sub> (1)	Forward On Voltage	$I_{SD} = 4 \text{ A}, V_{GS} = 0$ $I_{SD} = 3 \text{ A}, V_{GS} = 0$	n-ch p-ch			1.2 1.2	V V
t <sub>rr</sub>	Reverse Recovery Time	N-CHANNEL I <sub>SD</sub> = 4 A, di/dt = 100 A/µs	n-ch p-ch		85 44		ns ns
Q <sub>rr</sub>	Reverse Recovery Charge	$V_{DD} = 20V, T_j = 150^{\circ}C$	n-ch p-ch		85 68.2		nC nC
I <sub>RRM</sub>	Reverse Recovery Current	P-CHANNEL $I_{SD} = 3 A$ , di/dt = 100 A/µs $V_{DD} = 20V$ , $T_j = 150$ °C (see test circuit, Figure 29)	n-ch p-ch		2 3.1		A A

(1) Pulsed: Pulse duration =  $300 \ \mu$ s, duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating n-channel

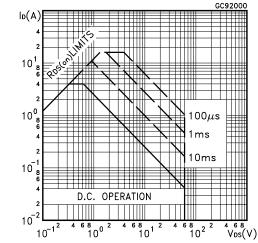
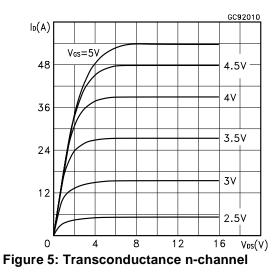
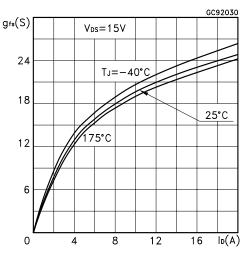


Figure 4: Output Characteristics n-channel





#### Figure 6: Thermal Impedance For Complementary Pair

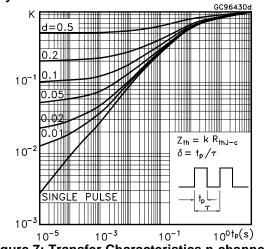


Figure 7: Transfer Characteristics n-channel

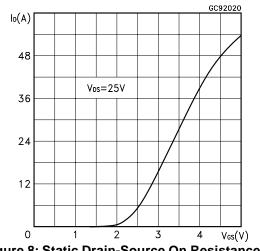
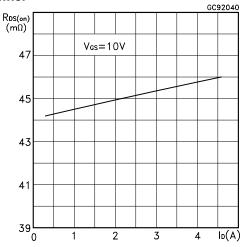


Figure 8: Static Drain-Source On Resistance nchannel



## Figure 9: Gate Charge vs Gate-Source Voltage n-channel

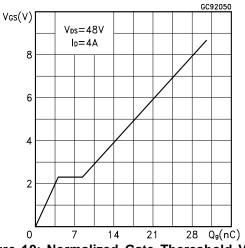


Figure 10: Normalized Gate Thereshold Voltage vs Temperature n-channel

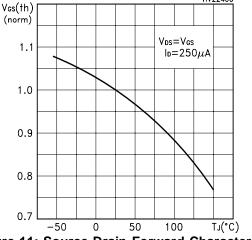
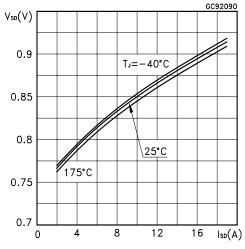


Figure 11: Source-Drain Forward Characteristics n-channel



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#### Figure 12: Capacitance Variations n-channel

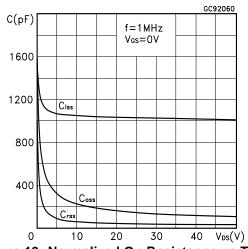


Figure 13: Normalized On Resistance vs Temperature n-channel

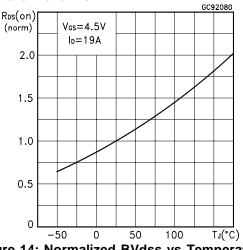


Figure 14: Normalized BVdss vs Temperature n-channel

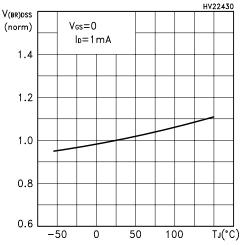


Figure 15: Safe Operating p-channel

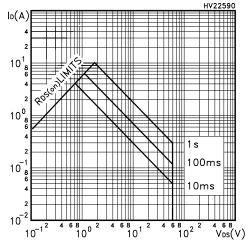
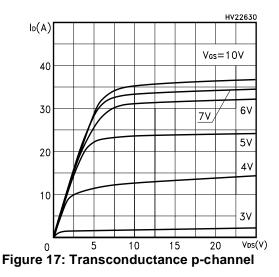


Figure 16: Output Characteristics p-channel



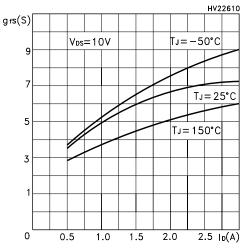


Figure 18: Thermal Impedance for Complementary Pair

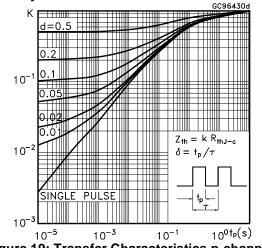


Figure 19: Transfer Characteristics p-channel

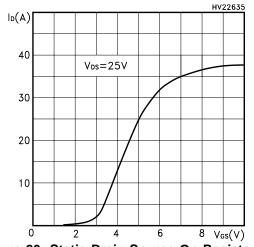
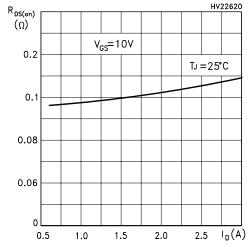


Figure 20: Static Drain-Source On Resistance p-channel



### Figure 21: Gate Charge vs Gate-Source Voltage p-channel

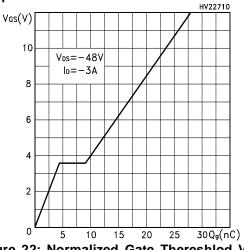


Figure 22: Normalized Gate Thereshlod Voltage vs Temperature p-channel

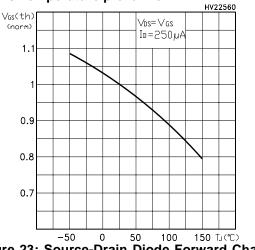
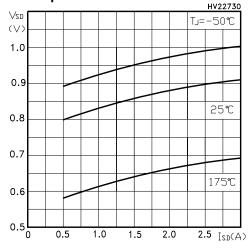


Figure 23: Source-Drain Diode Forward Characteristics p-channel



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#### Figure 24: Capacitances Variations p-channel

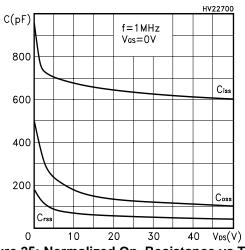


Figure 25: Normalized On Resistance vs Temperature p-channel

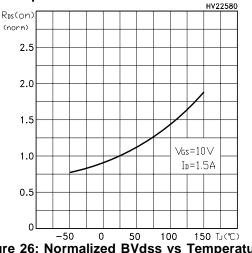
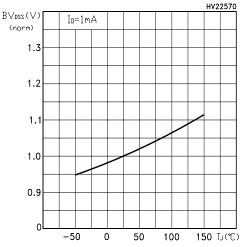


Figure 26: Normalized BVdss vs Temperature p-channel



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Figure 27: Unclamped Inductive Load Test Circuit

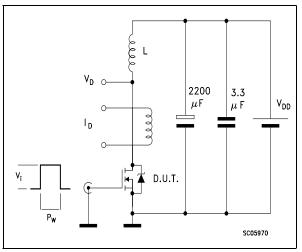


Figure 28: Switching Times Test Circuit For Resistive Load

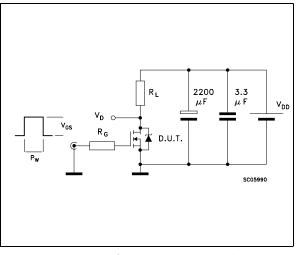


Figure 29: Test Circuit For Inductive Load Switching and Diode Recovery Times

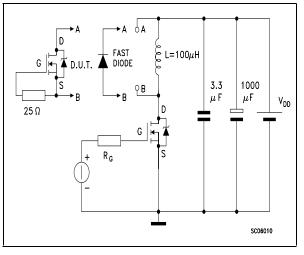


Figure 30: Unclamped Inductive Wafeform

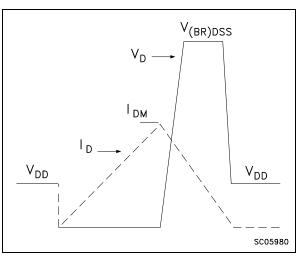
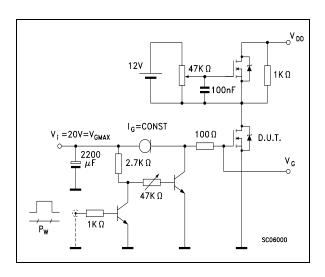
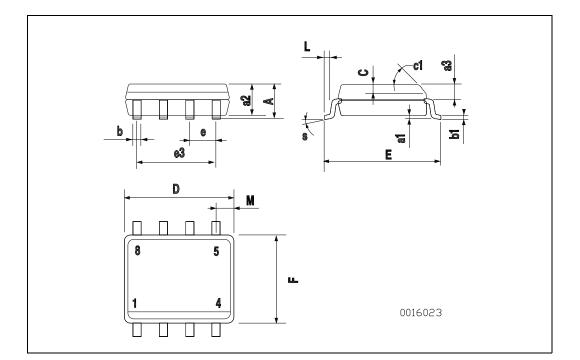


Figure 31: Gate Charge Test Circuit



ым		mm.			inch	
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX
А			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
С	0.25		0.5	0.010		0.019
c1			45 (	(typ.)		
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
е		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
М			0.6			0.023



#### SO-8 MECHANICAL DATA

#### Table 10: Revision History

Date	Revision	Description of Changes
16-Sep-2004	2	Complete Version

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