



M74HCT132

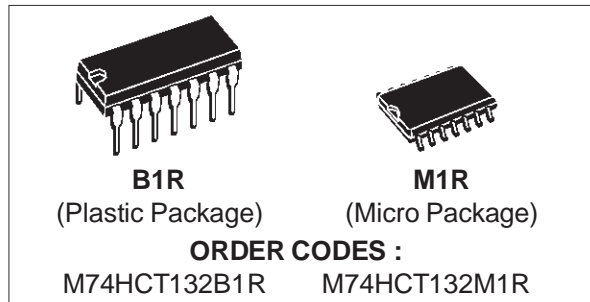
QUAD 2-INPUT SCHMITT NAND GATE

- HIGH SPEED: $t_{PD} = 20 \text{ ns}$ (TYP.) at $V_{CC} = 4.5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 1 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- OUTPUT DRIVE CAPABILITY
10 LSTTL LOADS
- HIGH NOISE IMMUNITY
 V_H (TYP.) = 0.71V AT $V_{CC} = 4.5\text{V}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- PIN AND FUNCTION COMPATIBLE WITH
74 SERIES 132

DESCRIPTION

The M74HCT132 is a high speed CMOS QUAD 2-INPUT SCHMITT NAND GATE fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true COMS low power consumption. Pin

PRELIMINARY DATA

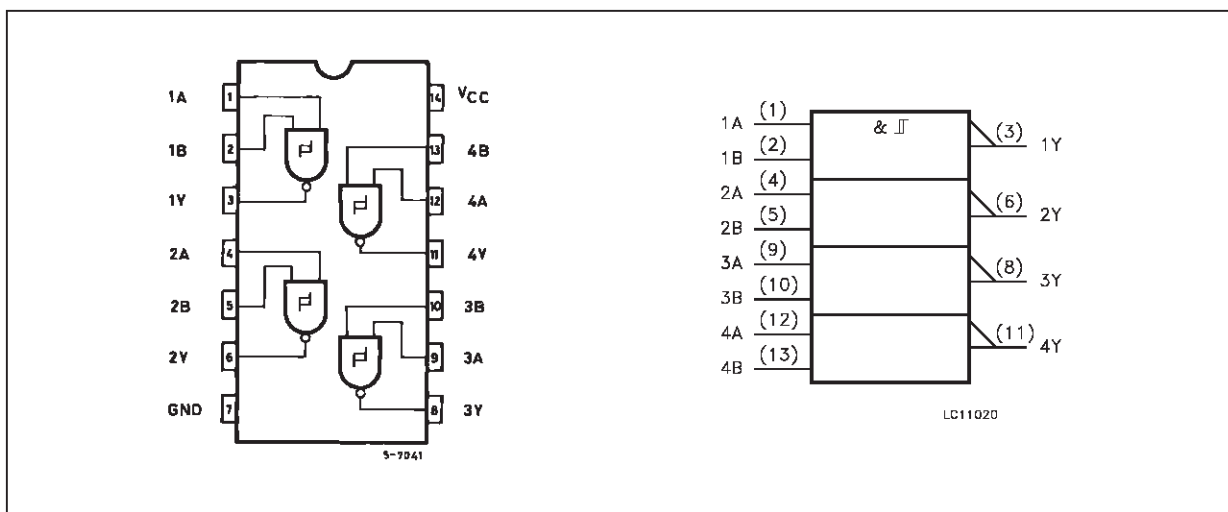


configuration and function are identical to those of the M74HCT00.

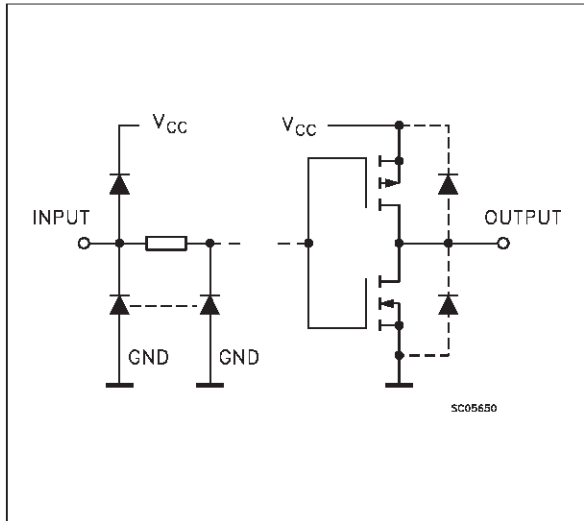
The hysteresis characteristics (around 15% V_{CC}) of all inputs allow slowly charging input signals to be transformed into sharply defined jitter-free output signals.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	Data Inputs
2, 5, 10, 13	1B to 4B	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	Vcc	Positive Supply Voltage

TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
 (*) 500 mW: ≅ 65 °C derate 300 mW by 10 mW/°C: 65 °C to 80 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	4.5 to 5.5	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-40 to +85	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit	
				V _{CC} (V)	T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
V _{t+}	High Level Threshold Voltage	4.5		1.2	1.55	1.9	1.2	1.9	V	
		5.5		1.4	1.75	2.1	1.4	2.1		
V _{t-}	Low Level Threshold Voltage	4.5		0.5	0.85	1.2	0.5	1.2	V	
		5.5		0.6	1.1	1.4	0.6	1.4		
V _h	Hysteresis Voltage	4.5		0.4	0.7	1.4	0.4	1.4	V	
		5.5		0.4	0.7	1.5	0.4	1.5		
V _{OH}	High Level Output Voltage	4.5	V _I ^(*) =	I _O =-50 μA	4.4	4.5		4.4	V	
		4.5	V _{IL} or V _{IH}	I _O =-8 mA	4.18	4.31		4.13		
V _{OL}	Low Level Output Voltage	4.5	V _I ^(*) =	I _O =50 μA		0.0	0.1	0.1	V	
		4.5	V _{IH}	I _O =8 mA		0.17	0.26	0.33		
I _I	Input Leakage Current	5.5	V _I = 5.5V or GND				±0.1	±1.0	μA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND				1	10	μA	

(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Test Condition		Value					Unit	
				V _{CC} (V)	T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	4.5			7.0	15.0		19.0	ns	
t _{PLH} t _{PHL}	Propagation Delay Time	4.5			20.0	33.0		41.0	ns	

(*) Voltage range is 3.3V ± 0.3V

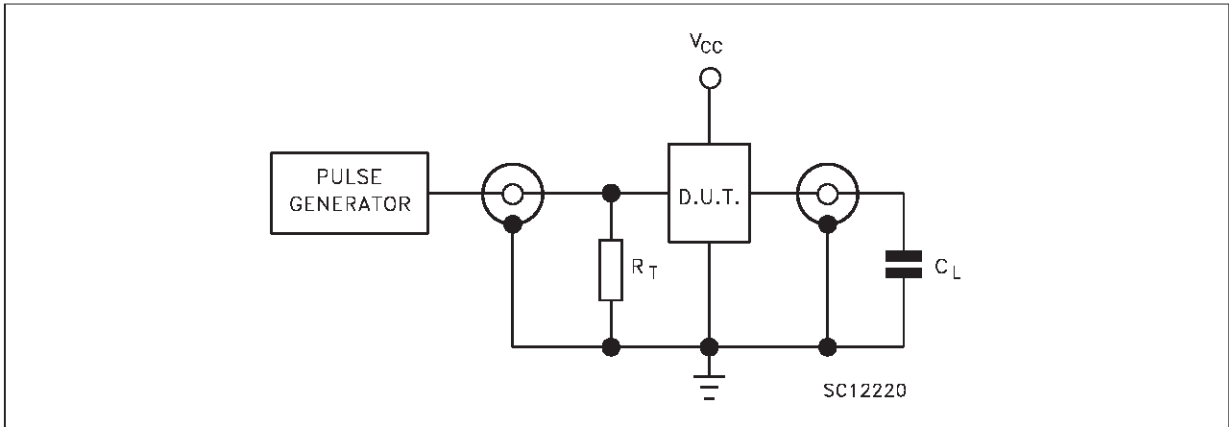
(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit	
					T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
C _{IN}	Input Capacitance			3.5					pF	
C _{PD}	Power Dissipation Capacitance (note 1)			20					pF	

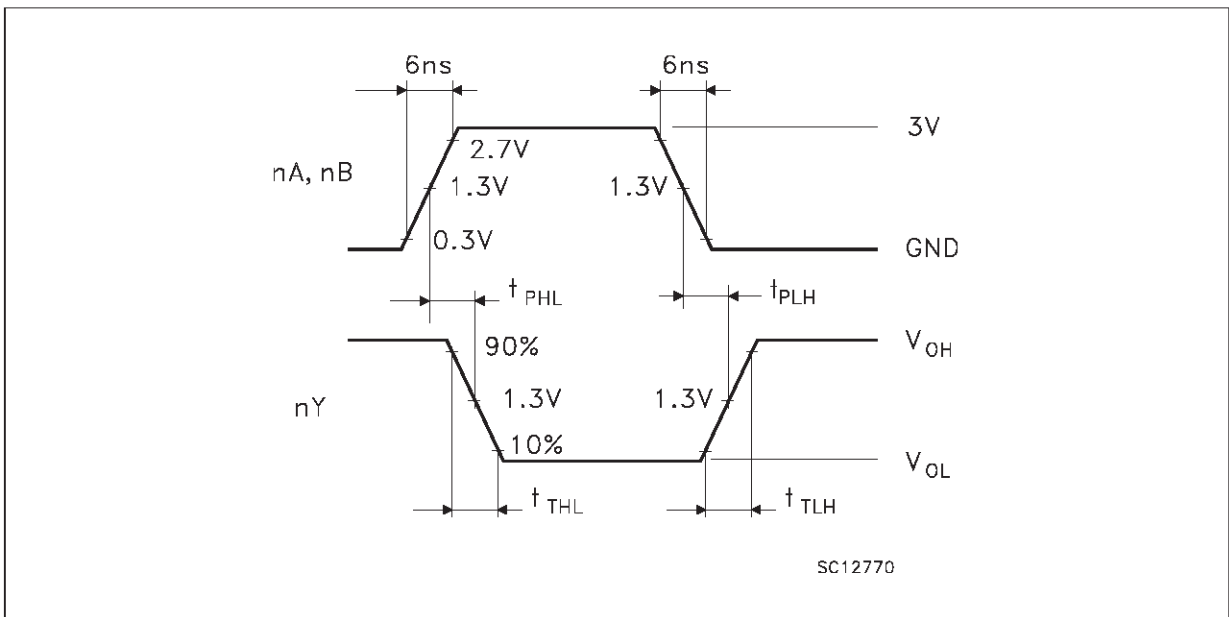
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} • V_{CC} • f_{IN} + I_{CC}/4 (per Gate)

TEST CIRCUIT



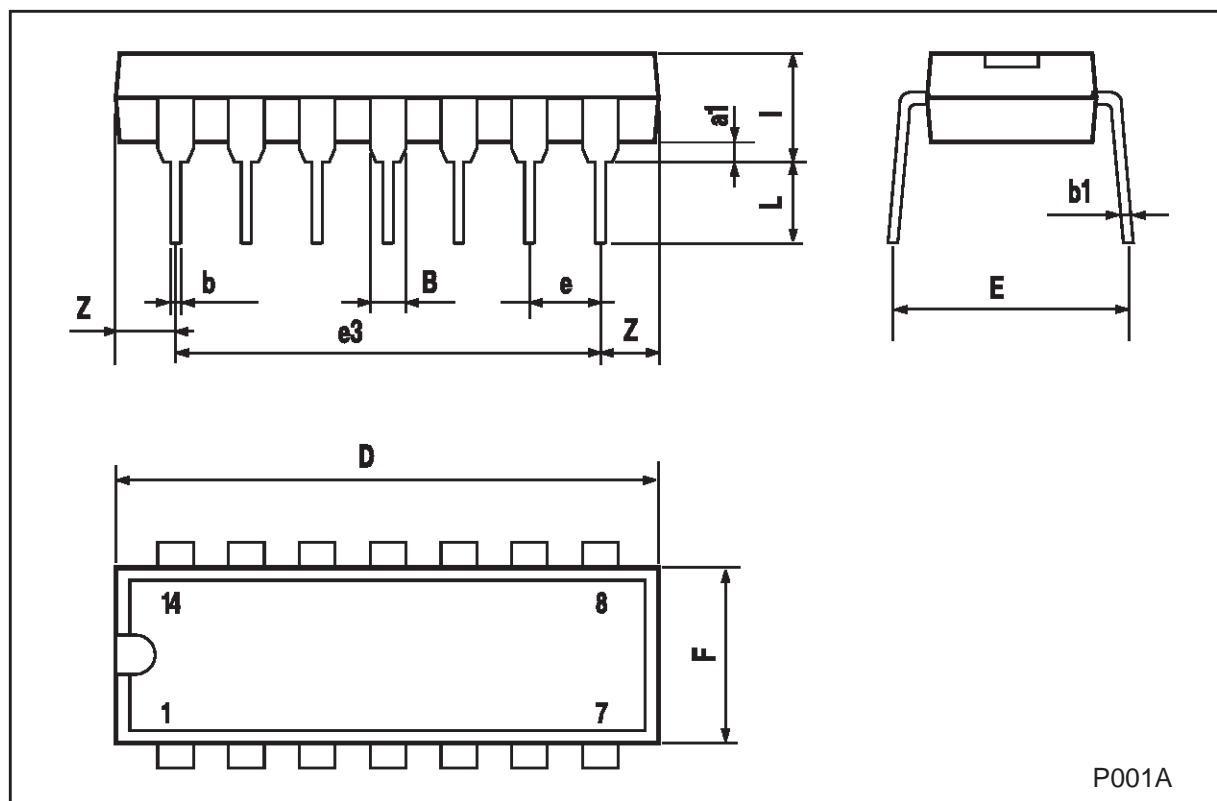
$C_L = 15/50$ pF or equivalent (includes jig and probe capacitance)
 $R_T = Z_{out}$ of pulse generator (typically 50Ω)

WAVEFORM: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



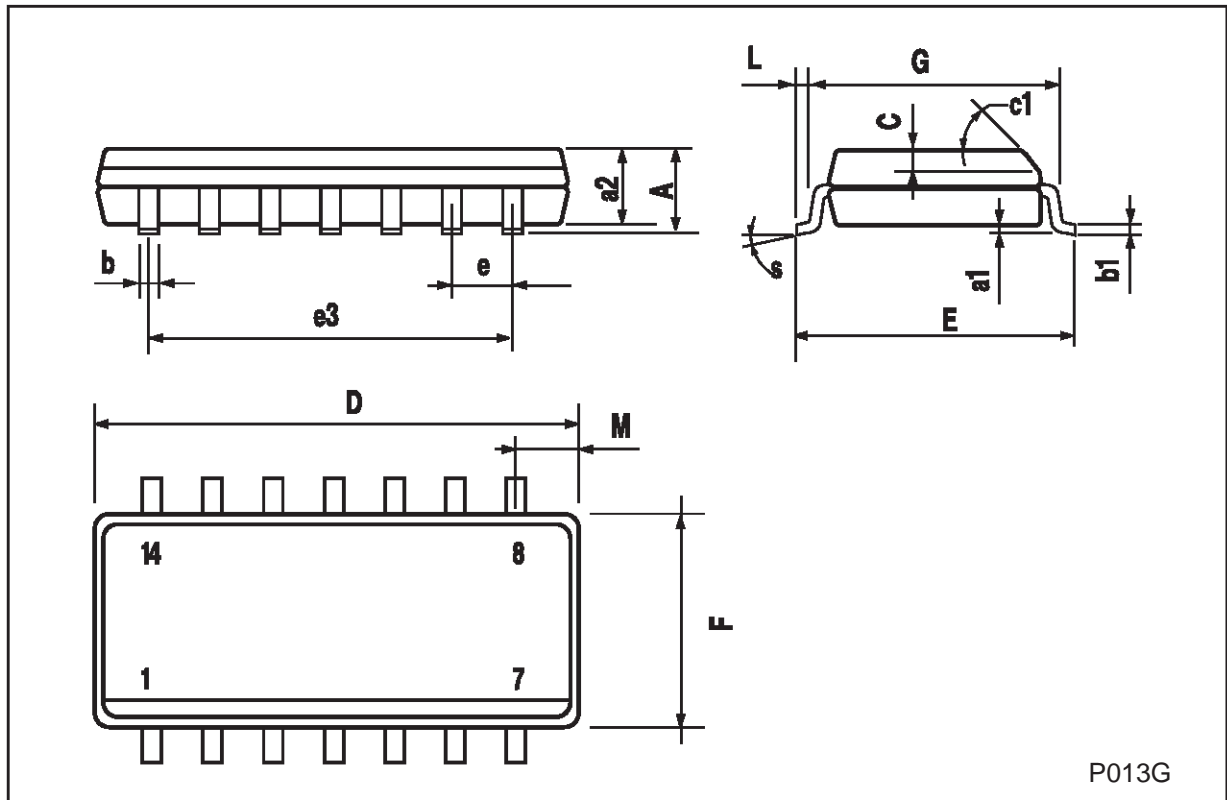
Plastic DIP-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



SO-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



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