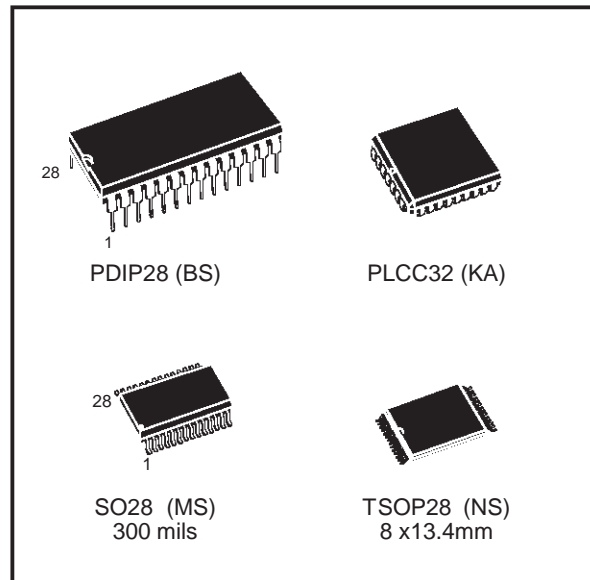




# M28C16A M28C17A

## 16 Kbit (2Kb x8) Parallel EEPROM

- FAST ACCESS TIME:
  - 150ns at 5V
  - 250ns at 3V
- SINGLE SUPPLY VOLTAGE:
  - 5V ± 10% for M28C16A and M28C17A
  - 2.7V to 3.6V for M28C16-xxW
- LOW POWER CONSUMPTION
- FAST WRITE CYCLE
  - 32 Bytes Page Write Operation
  - Byte or Page Write Cycle: 5ms
- ENHANCED END OF WRITE DETECTION
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABILITY SINGLE POLYSILICON, CMOS TECHNOLOGY
  - Endurance >100,000 Erase/Write Cycles
  - Data Retention >40 Years
- JEDEC APPROVED BYTEWIDE PIN OUT



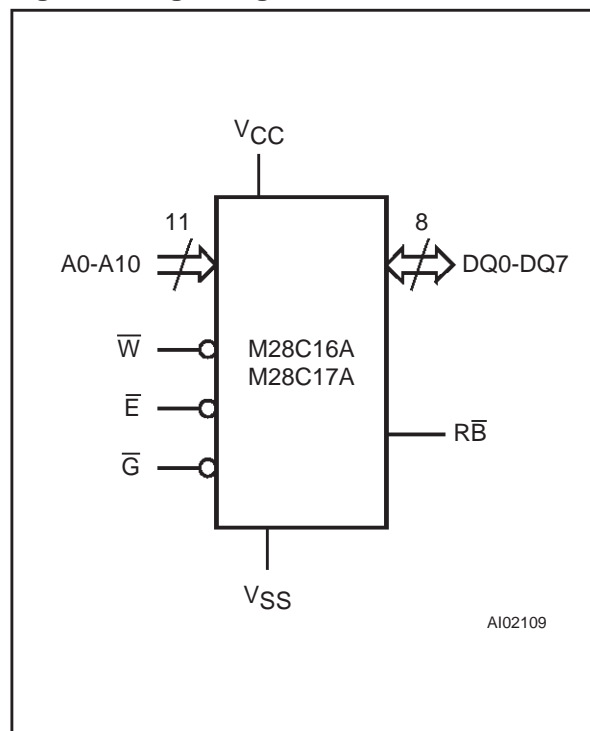
### DESCRIPTION

The M28C16A and M28C17A are 2K x8 low power Parallel EEPROM fabricated with STMicroelectronics proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 5V or 3V power supply.

**Table 1. Signal Names**

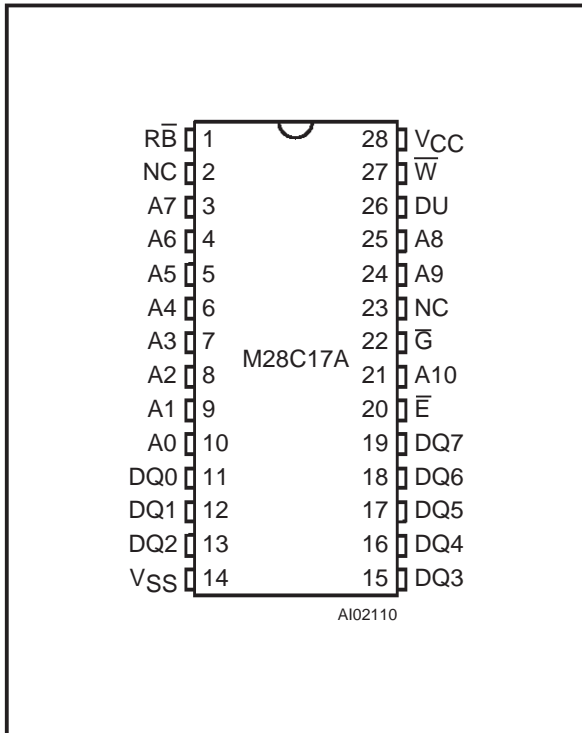
|                 |                     |
|-----------------|---------------------|
| A0-A10          | Address Input       |
| DQ0-DQ7         | Data Input / Output |
| $\overline{W}$  | Write Enable        |
| $\overline{E}$  | Chip Enable         |
| $\overline{G}$  | Output Enable       |
| $\overline{RB}$ | Ready / Busy        |
| V <sub>CC</sub> | Supply Voltage      |
| V <sub>SS</sub> | Ground              |

**Figure 1. Logic Diagram**



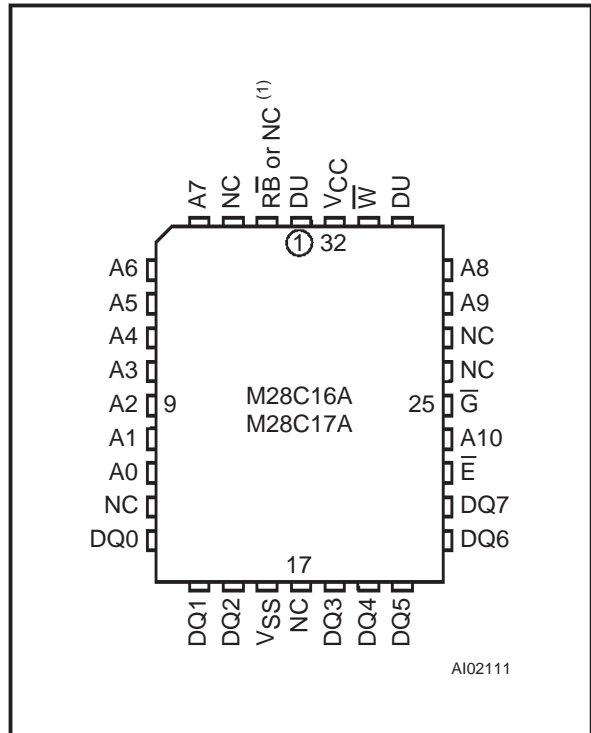
# M28C16A, M28C17A

**Figure 2A. DIP Pin Connections**



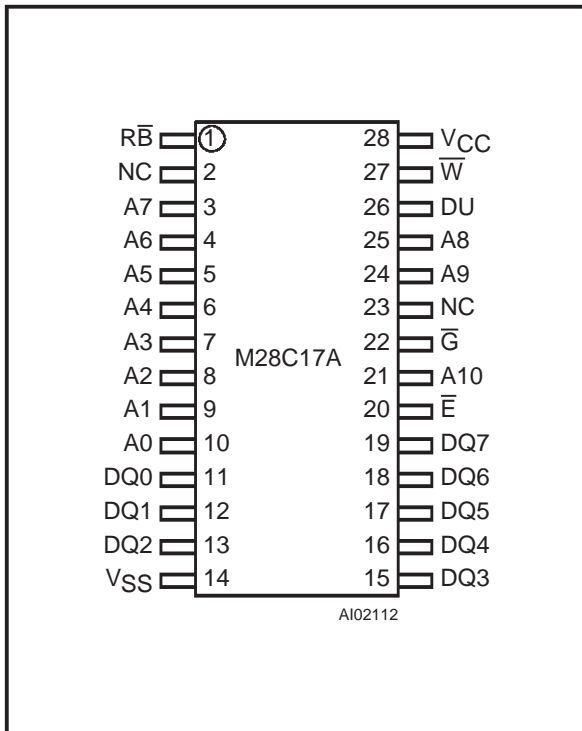
**Warning:** NC = Not Connected, DU = Don't Use.

**Figure 2B. LCC Pin Connections**



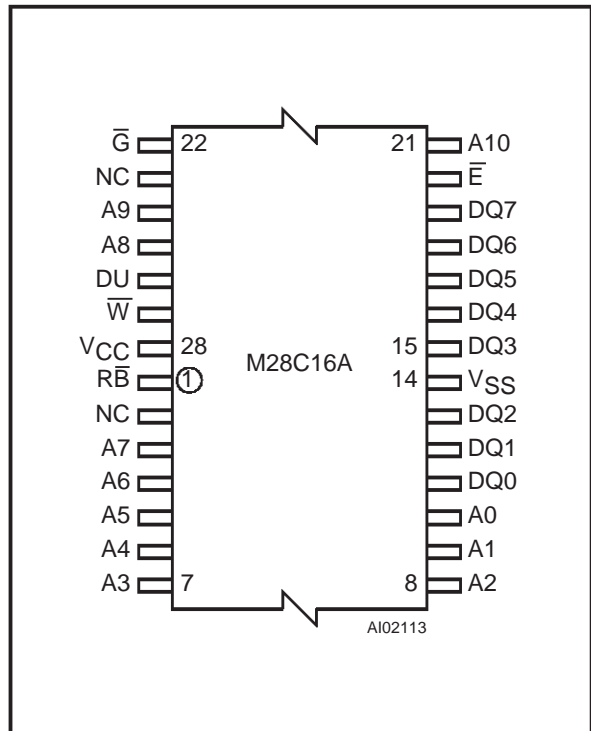
**Warning:** NC = Not Connected, DU = Don't Use.  
**Note:** 1. Pin 2 is either RB for M28C17A or NC for M28C16A.

**Figure 2C. SO Pin Connections**



**Warning:** NC = Not Connected, DU = Don't Use.

**Figure 2D. TSOP Pin Connections**



**Warning:** NC = Not Connected, DU = Don't Use.

**Table 2. Absolute Maximum Ratings** <sup>(1)</sup>

| Symbol           | Parameter  | Value                         | Unit |
|------------------|--|-------------------------------|------|
| T <sub>A</sub>   | Ambient Operating Temperature <sup>(2)</sup>       | – 40 to 85                    | °C   |
| T <sub>STG</sub> | Storage Temperature Range                          | – 65 to 150                   | °C   |
| V <sub>CC</sub>  | Supply Voltage                                     | – 0.3 to 6.5                  | V    |
| V <sub>IO</sub>  | Input/Output Voltage                               | – 0.3 to V <sub>CC</sub> +0.6 | V    |
| V <sub>I</sub>   | Input Voltage                                      | – 0.3 to 6.5                  | V    |
| V <sub>ESD</sub> | Electrostatic Discharge Voltage (Human Body model) | 3000                          | V    |

**Notes:** 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2. Depends on range.

**Table 3. Operating Modes**

| Mode                    | $\bar{E}$       | $\bar{G}$       | $\bar{W}$       | DQ0 - DQ7        |
|-------------------------|-----------------|-----------------|-----------------|------------------|
| Read                    | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | Data Out         |
| Write                   | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | Data In          |
| Standby / Write Inhibit | V <sub>IH</sub> | X               | X               | Hi-Z             |
| Write Inhibit           | X               | X               | V <sub>IH</sub> | Data Out or Hi-Z |
| Write Inhibit           | X               | V <sub>IL</sub> | X               | Data Out or Hi-Z |
| Output Disable          | X               | V <sub>IH</sub> | X               | Hi-Z             |

**Note:** X = V<sub>IH</sub> or V<sub>IL</sub>

**DESCRIPTION** (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking mode with Ready/Busy, Data Polling and Toggle Bit. The M28C16A/17A supports 32 byte page write operation.

**PIN DESCRIPTION**

**Addresses (A0-A10).** The address inputs select an 8-bit memory location during a read or write operation.

**Chip Enable ( $\bar{E}$ ).** The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

**Output Enable ( $\bar{G}$ ).** The Output Enable input controls the data output buffers and is used to initiate read operations.

**Data In/Out (DQ0 - DQ7).** Data is written to or read from the M28C16A/17A through the I/O pins.

**Write Enable ( $\bar{W}$ ).** The Write Enable input controls the writing of data to the M28C16A/17A.

**Ready/Busy ( $\bar{R}\bar{B}$ ).** Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle. Ready/Busy is available for the M28C17A in PDIP, PLCC and SO packages, and for the M28C16A in TSOP only.

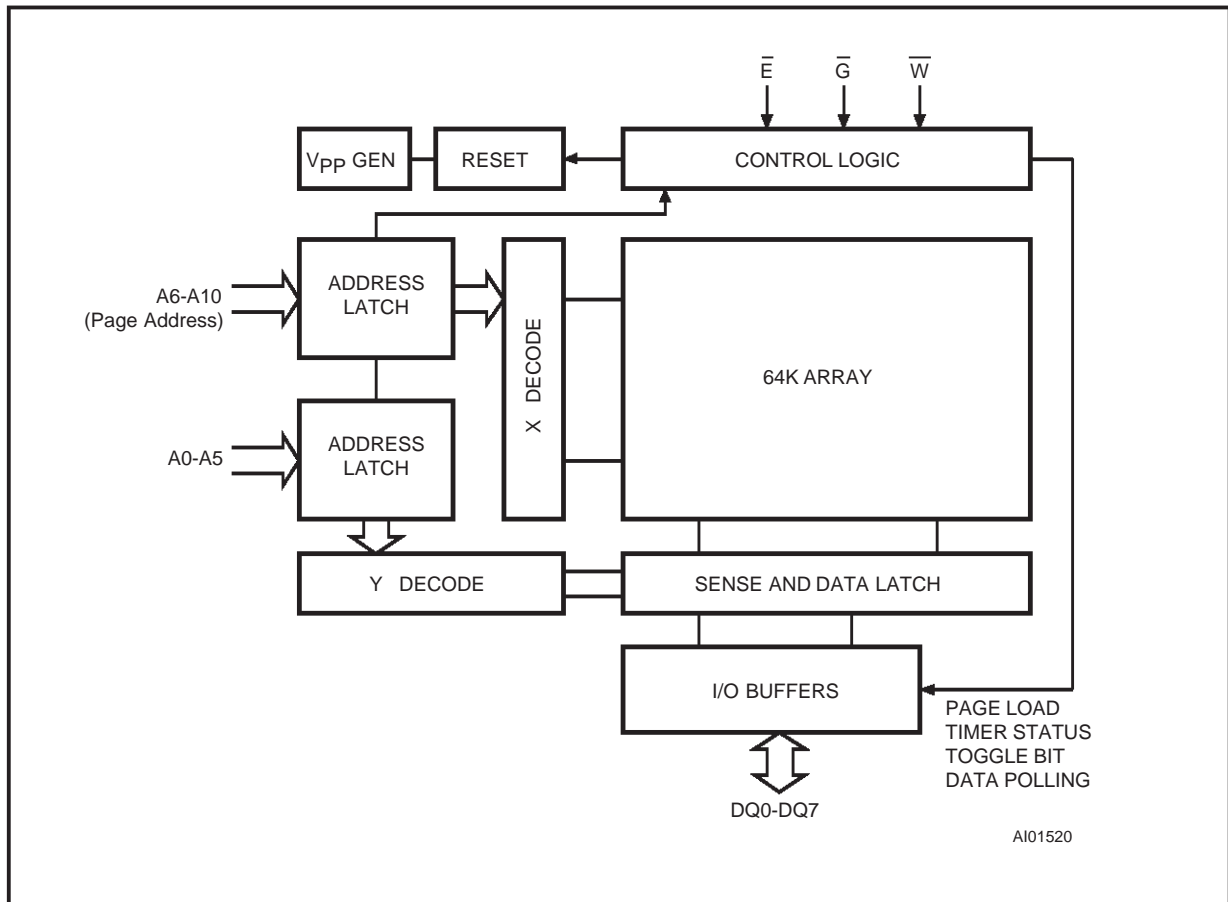
**OPERATION**

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming circuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 7.

**Read**

The M28C16A/17A is accessed like a static RAM. When  $\bar{E}$  and  $\bar{G}$  are low with  $\bar{W}$  high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either  $\bar{G}$  or  $\bar{E}$  is high.

Figure 3. Block Diagram



**OPERATION (cont'd)**

**Write**

Write operations are initiated when both  $\overline{W}$  and  $\overline{E}$  are low and  $\overline{G}$  is high. The M28C16A/17A supports both  $\overline{E}$  and  $\overline{W}$  controlled write cycles. The Address is latched by the falling edge of  $\overline{E}$  or  $\overline{W}$  which ever occurs last and the Data on the rising edge of  $\overline{E}$  or  $\overline{W}$  which ever occurs first. Once initiated the write operation is internally timed until completion.

**Page Write**

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a

programming cycle. All bytes must be located in a single page address, that is A5 - A10 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data up to a maximum of  $t_{WHWH}$  after the rising edge of  $\overline{E}$  or  $\overline{W}$  which ever occurs first. If a transition of  $\overline{E}$  or  $\overline{W}$  is not detected within  $t_{WHWH}$ , the internal programming cycle will start.

**Microcontroller Control Interface**

The M28C16A/17A provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the  $\overline{RB}$  signal on a separate pin.

Figure 4. Status Bit Assignment

|     |     |      |      |      |      |      |      |
|-----|-----|------|------|------|------|------|------|
| DQ7 | DQ6 | DQ5  | DQ4  | DQ3  | DQ2  | DQ1  | DQ0  |
| DP  | TB  | PLTS | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

DP = Data Polling  
 TB = Toggle Bit  
 PLTS = Page Load Timer Status

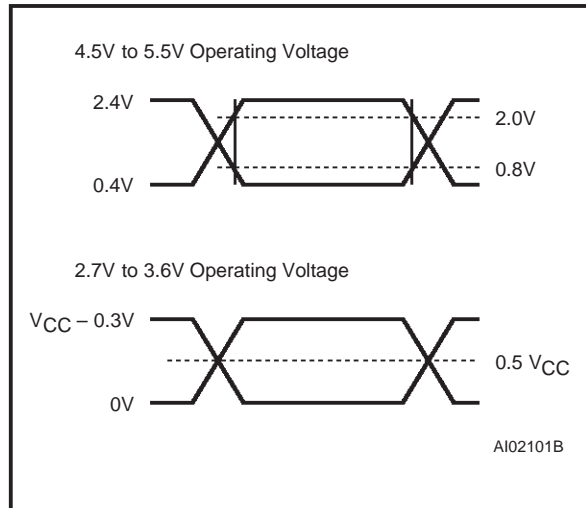
**Data Polling bit (DQ7).** During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

**Table 4. AC Measurement Conditions**

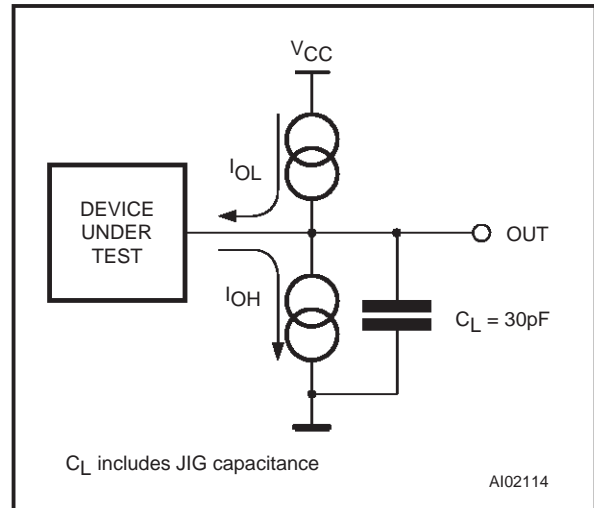
|                                       |              |
|---------------------------------------|--------------|
| Input Rise and Fall Times             | ≤ 20ns       |
| Input Pulse Voltages                  | 0.4V to 2.4V |
| Input and Output Timing Ref. Voltages | 0.8V to 2.0V |

Note that Output Hi-Z is defined as the point where data is no longer driven.

**Figure 5. AC Testing Input Output Waveforms**



**Figure 6. AC Testing Equivalent Load Circuit**



**Table 5. Capacitance<sup>(1)</sup>**  
( $T_A = 25\text{ }^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

| Symbol    | Parameter          | Test Condition | Min | Max | Unit |
|-----------|--------------------|----------------|-----|-----|------|
| $C_{IN}$  | Input Capacitance  | $V_{IN} = 0V$  |     | 6   | pF   |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ |     | 12  | pF   |

Note: 1. Sampled only, not 100% tested.

**Table 6. Read Mode DC Characteristics for M28C16A and M28C17A**  
( $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ ,  $V_{CC} = 4.5V\text{ to }5.5V$ )

| Symbol          | Parameter                            | Test Condition   | Min  | Max            | Unit    |
|-----------------|--------------------------------------|--|------|----------------|---------|
| $I_{LI}$        | Input Leakage Current                | $0V \leq V_{IN} \leq V_{CC}$                           |      | 10             | $\mu A$ |
| $I_{LO}$        | Output Leakage Current               | $0V \leq V_{IN} \leq V_{CC}$                           |      | 10             | $\mu A$ |
| $I_{CC}^{(1)}$  | Supply Current (TTL and CMOS inputs) | $\bar{E} = V_{IL}, \bar{G} = V_{IL}, f = 5\text{ MHz}$ |      | 25             | mA      |
| $I_{CC1}^{(1)}$ | Supply Current (Standby) TTL         | $\bar{E} = V_{IH}$                                     |      | 1              | mA      |
| $I_{CC2}^{(1)}$ | Supply Current (Standby) CMOS        | $\bar{E} > V_{CC} - 0.3V$                              |      | 50             | $\mu A$ |
| $V_{IL}$        | Input Low Voltage                    |  | -0.3 | 0.8            | V       |
| $V_{IH}$        | Input High Voltage                   |  | 2    | $V_{CC} + 0.5$ | V       |
| $V_{OL}$        | Output Low Voltage                   | $I_{OL} = 2.1\text{ mA}$                               |      | 0.4            | V       |
| $V_{OH}$        | Output High Voltage                  | $I_{OH} = -400\text{ }\mu A$                           | 2.4  |                | V       |

Note: 1. All I/O's open circuit.

## M28C16A, M28C17A

**Table 7. Power Up Timing for M28C16A and M28C17A <sup>(1)</sup>**  
( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ )

| Symbol    | Parameter  | Min | Max | Unit          |
|-----------|--|-----|-----|---------------|
| $t_{PUR}$ | Time Delay to Read Operation                               |     | 1   | $\mu\text{s}$ |
| $t_{PUW}$ | Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$ ) |     | 10  | ms            |
| $V_{WI}$  | Write Inhibit Threshold                                    | 1.5 | 2.5 | V             |

**Note:** 1. Sampled only, not 100% tested.

**Table 8. Read Mode DC Characteristics for M28C16A-W**  
( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

| Symbol          | Parameter                            | Test Condition   | Min          | Max            | Unit          |
|-----------------|--------------------------------------|--|--------------|----------------|---------------|
| $I_{LI}$        | Input Leakage Current                | $0\text{V} \leq V_{IN} \leq V_{CC}$                              |              | 10             | $\mu\text{A}$ |
| $I_{LO}$        | Output Leakage Current               | $0\text{V} \leq V_{IN} \leq V_{CC}$                              |              | 10             | $\mu\text{A}$ |
| $I_{CC}^{(1)}$  | Supply Current (TTL and CMOS inputs) | $\overline{E} = V_{IL}, \overline{G} = V_{IL}, f = 5\text{ MHz}$ |              | 15             | mA            |
| $I_{CC2}^{(1)}$ | Supply Current (Standby) CMOS        | $\overline{E} > V_{CC} - 0.3\text{V}$                            |              | 20             | $\mu\text{A}$ |
| $V_{IL}$        | Input Low Voltage                    |  | -0.3         | 0.6            | V             |
| $V_{IH}$        | Input High Voltage                   |  | 2            | $V_{CC} + 0.5$ | V             |
| $V_{OL}$        | Output Low Voltage                   | $I_{OL} = 2.1\text{ mA}$   |              | $0.2 V_{CC}$   | V             |
| $V_{OH}$        | Output High Voltage                  | $I_{OH} = -400\ \mu\text{A}$                                     | $0.8 V_{CC}$ |                | V             |

**Note:** 1. All I/O's open circuit.

**Table 9. Power Up Timing for M28C16A-W <sup>(1)</sup>**  
( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

| Symbol    | Parameter  | Min | Max | Unit          |
|-----------|--|-----|-----|---------------|
| $t_{PUR}$ | Time Delay to Read Operation                               |     | 1   | $\mu\text{s}$ |
| $t_{PUW}$ | Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$ ) |     | 10  | ms            |
| $V_{WI}$  | Write Inhibit Threshold                                    | 1.5 | 2.5 | V             |

**Note:** 1. Sampled only, not 100% tested.

**Table 10. Read Mode AC Characteristics for M28C16A and M28C17A**  
 ( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ )

| Symbol           | Alt       | Parameter                               | Test Condition                                 | M28C16A / M28C17A |     |     |     | Unit |
|------------------|-----------|---|--|-------------------|-----|-----|-----|------|
|                  |           |   |  | -15               |     | -20 |     |      |
|                  |           |   |  | min               | max | min | max |      |
| $t_{AVQV}$       | $t_{ACC}$ | Address Valid to Output Valid           | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ |                   | 150 |     | 200 | ns   |
| $t_{ELQV}$       | $t_{CE}$  | Chip Enable Low to Output Valid         | $G = V_{IL}$                                   |                   | 150 |     | 200 | ns   |
| $t_{GLQV}$       | $t_{OE}$  | Output Enable Low to Output Valid       | $\overline{E} = V_{IL}$                        |                   | 70  |     | 80  | ns   |
| $t_{EHQZ}^{(1)}$ | $t_{DF}$  | Chip Enable High to Output Hi-Z         | $\overline{G} = V_{IL}$                        | 0                 | 50  | 0   | 60  | ns   |
| $t_{GHQZ}^{(1)}$ | $t_{DF}$  | Output Enable High to Output Hi-Z       | $\overline{E} = V_{IL}$                        | 0                 | 50  | 0   | 60  | ns   |
| $t_{AXQX}$       | $t_{OH}$  | Address Transition to Output Transition | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 0                 |     | 0   |     | ns   |

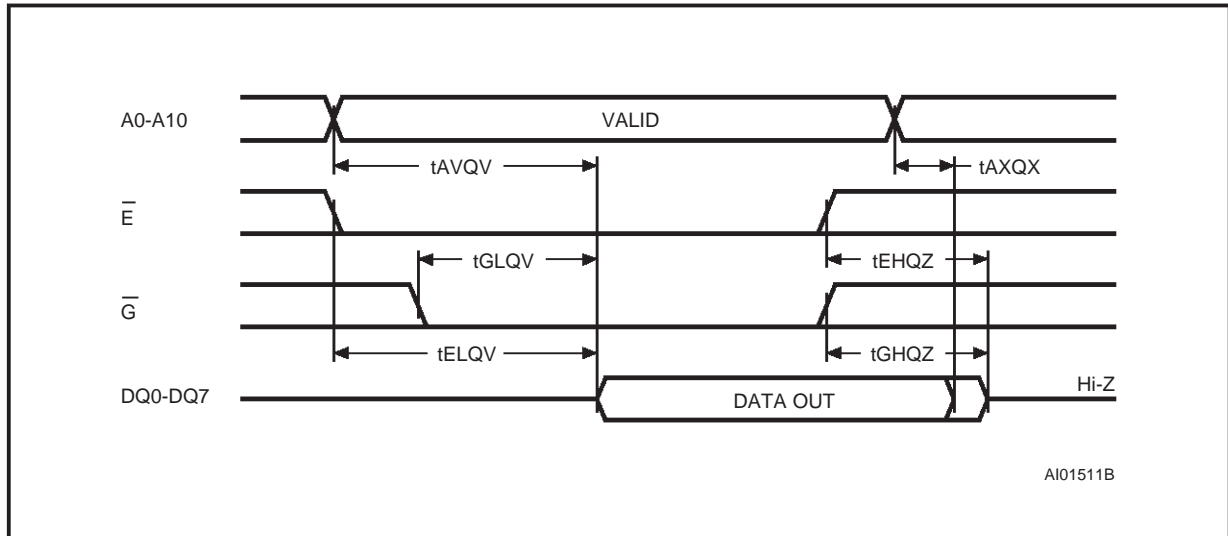
Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

**Table 11. Read Mode AC Characteristics for M28C16-W**  
 ( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

| Symbol           | Alt       | Parameter                               | Test Condition                                 | M28C16A / M28C17A |     |     |     | Unit |
|------------------|-----------|---|--|-------------------|-----|-----|-----|------|
|                  |           |   |  | -25               |     | -30 |     |      |
|                  |           |   |  | min               | max | min | max |      |
| $t_{AVQV}$       | $t_{ACC}$ | Address Valid to Output Valid           | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ |                   | 250 |     | 300 | ns   |
| $t_{ELQV}$       | $t_{CE}$  | Chip Enable Low to Output Valid         | $G = V_{IL}$                                   |                   | 250 |     | 300 | ns   |
| $t_{GLQV}$       | $t_{OE}$  | Output Enable Low to Output Valid       | $\overline{E} = V_{IL}$                        |                   | 100 |     | 100 | ns   |
| $t_{EHQZ}^{(1)}$ | $t_{DF}$  | Chip Enable High to Output Hi-Z         | $\overline{G} = V_{IL}$                        | 0                 | 70  | 0   | 80  | ns   |
| $t_{GHQZ}^{(1)}$ | $t_{DF}$  | Output Enable High to Output Hi-Z       | $\overline{E} = V_{IL}$                        | 0                 | 70  | 0   | 80  | ns   |
| $t_{AXQX}$       | $t_{OH}$  | Address Transition to Output Transition | $\overline{E} = V_{IL}, \overline{G} = V_{IL}$ | 0                 |     | 0   |     | ns   |

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Figure 7. Read Mode AC Waveforms



Note: Write Enable ( $\bar{W}$ ) = High

**Toggle bit (DQ6).** The M28C16A/17A offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any address in the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

**Page Load Timer Status bit (DQ5).** In the Page Write mode data may be latched by  $\bar{E}$  or  $\bar{W}$  up to  $t_{WHWH}$  after the previous byte. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low ( $t_{PLTS}$ ). DQ5 Low indicates the timer is running, High



**Table 12. Write Mode AC Characteristics for M28C16A and M28C17A**  
 ( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $5.5\text{V}$ )

| Symbol      | Alt       | Parameter                              | Test Condition                                 | Min | Max | Unit          |
|-------------|-----------|--|--|-----|-----|---------------|
| $t_{AVWL}$  | $t_{AS}$  | Address Valid to Write Enable Low      | $\overline{E} = V_{IL}, \overline{G} = V_{IH}$ | 0   |     | ns            |
| $t_{AVEL}$  | $t_{AS}$  | Address Valid to Chip Enable Low       | $\overline{G} = V_{IH}, \overline{W} = V_{IL}$ | 0   |     | ns            |
| $t_{ELWL}$  | $t_{CES}$ | Chip Enable Low to Write Enable Low    | $\overline{G} = V_{IH}$                        | 0   |     | ns            |
| $t_{GHWL}$  | $t_{OES}$ | Output Enable High to Write Enable Low | $\overline{E} = V_{IL}$                        | 0   |     | ns            |
| $t_{GHLEL}$ | $t_{OES}$ | Output Enable High to Chip Enable Low  | $\overline{W} = V_{IL}$                        | 0   |     | ns            |
| $t_{WLEL}$  | $t_{WES}$ | Write Enable Low to Chip Enable Low    | $\overline{G} = V_{IH}$                        | 0   |     | ns            |
| $t_{WLAX}$  | $t_{AH}$  | Write Enable Low to Address Transition |  | 100 |     | ns            |
| $t_{ELAX}$  | $t_{AH}$  | Chip Enable Low to Address Transition  |  | 100 |     | ns            |
| $t_{WLDV}$  | $t_{DV}$  | Write Enable Low to Input Valid        | $\overline{E} = V_{IL}, \overline{G} = V_{IH}$ |     | 1   | $\mu\text{s}$ |
| $t_{ELDV}$  | $t_{DV}$  | Chip Enable Low to Input Valid         | $\overline{G} = V_{IH}, \overline{W} = V_{IL}$ |     | 1   | $\mu\text{s}$ |
| $t_{ELEH}$  | $t_{WP}$  | Chip Enable Low to Chip Enable High    |  | 100 |     | ns            |
| $t_{WHEH}$  | $t_{CEH}$ | Write Enable High to Chip Enable High  |  | 0   |     | ns            |
| $t_{WHGL}$  | $t_{OEH}$ | Write Enable High to Output Enable Low |  | 0   |     | ns            |
| $t_{EHGL}$  | $t_{OEH}$ | Chip Enable High to Output Enable Low  |  | 0   |     | ns            |
| $t_{EHWH}$  | $t_{WEH}$ | Chip Enable High to Write Enable High  |  | 0   |     | ns            |
| $t_{WHDX}$  | $t_{DH}$  | Write Enable High to Input Transition  |  | 0   |     | ns            |
| $t_{EHDX}$  | $t_{DH}$  | Chip Enable High to Input Transition   |  | 0   |     | ns            |
| $t_{WHWL}$  | $t_{WPH}$ | Write Enable High to Write Enable Low  |  | 200 |     | ns            |
| $t_{WLWH}$  | $t_{WP}$  | Write Enable Low to Write Enable High  |  | 100 |     | ns            |
| $t_{WHWH}$  | $t_{BLC}$ | Byte Load Repeat Cycle Time            |  | 0.2 | 30  | $\mu\text{s}$ |
| $t_{WHRH}$  | $t_{WC}$  | Write Cycle Time                       |  |     | 5   | ms            |
| $t_{WHRL}$  | $t_{DB}$  | Write Enable High to Ready/Busy Low    | Note 1   |     | 100 | ns            |
| $t_{EHRL}$  | $t_{DB}$  | Chip Enable High to Ready/Busy Low     | Note 1   |     | 100 | ns            |
| $t_{DVWH}$  | $t_{DS}$  | Data Valid before Write Enable High    |  | 50  |     | ns            |
| $t_{DVEH}$  | $t_{DS}$  | Data Valid before Chip Enable High     |  | 50  |     | ns            |

Note: 1. With a 3.3 k $\Omega$  external pull-up resistor.

## M28C16A, M28C17A

**Table 13. Write Mode AC Characteristics for M28C16-W**  
( $T_A = -40$  to  $85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

| Symbol      | Alt       | Parameter                              | Test Condition                       | Min | Max | Unit          |
|-------------|-----------|--|--------------------------------------|-----|-----|---------------|
| $t_{AVWL}$  | $t_{AS}$  | Address Valid to Write Enable Low      | $\bar{E} = V_{IL}, \bar{G} = V_{IH}$ | 0   |     | ns            |
| $t_{AVEL}$  | $t_{AS}$  | Address Valid to Chip Enable Low       | $\bar{G} = V_{IH}, \bar{W} = V_{IL}$ | 0   |     | ns            |
| $t_{ELWL}$  | $t_{CES}$ | Chip Enable Low to Write Enable Low    | $\bar{G} = V_{IH}$                   | 0   |     | ns            |
| $t_{GHWL}$  | $t_{OES}$ | Output Enable High to Write Enable Low | $\bar{E} = V_{IL}$                   | 0   |     | ns            |
| $t_{GHLEL}$ | $t_{OES}$ | Output Enable High to Chip Enable Low  | $\bar{W} = V_{IL}$                   | 0   |     | ns            |
| $t_{WLEL}$  | $t_{WES}$ | Write Enable Low to Chip Enable Low    | $\bar{G} = V_{IH}$                   | 0   |     | ns            |
| $t_{WLAX}$  | $t_{AH}$  | Write Enable Low to Address Transition |                                      | 200 |     | ns            |
| $t_{ELAX}$  | $t_{AH}$  | Chip Enable Low to Address Transition  |                                      | 200 |     | ns            |
| $t_{WLDV}$  | $t_{DV}$  | Write Enable Low to Input Valid        | $\bar{E} = V_{IL}, \bar{G} = V_{IH}$ |     | 1   | $\mu\text{s}$ |
| $t_{ELDV}$  | $t_{DV}$  | Chip Enable Low to Input Valid         | $\bar{G} = V_{IH}, \bar{W} = V_{IL}$ |     | 1   | $\mu\text{s}$ |
| $t_{ELEH}$  | $t_{WP}$  | Chip Enable Low to Chip Enable High    |                                      | 200 |     | ns            |
| $t_{WHEH}$  | $t_{CEH}$ | Write Enable High to Chip Enable High  |                                      | 0   |     | ns            |
| $t_{WHGL}$  | $t_{OEH}$ | Write Enable High to Output Enable Low |                                      | 0   |     | ns            |
| $t_{EHGL}$  | $t_{OEH}$ | Chip Enable High to Output Enable Low  |                                      | 0   |     | ns            |
| $t_{EHWH}$  | $t_{WEH}$ | Chip Enable High to Write Enable High  |                                      | 0   |     | ns            |
| $t_{WHDX}$  | $t_{DH}$  | Write Enable High to Input Transition  |                                      | 0   |     | ns            |
| $t_{EHDX}$  | $t_{DH}$  | Chip Enable High to Input Transition   |                                      | 0   |     | ns            |
| $t_{WHWL}$  | $t_{WPH}$ | Write Enable High to Write Enable Low  |                                      | 200 |     | ns            |
| $t_{WLWH}$  | $t_{WP}$  | Write Enable Low to Write Enable High  |                                      | 200 |     | ns            |
| $t_{WHWH}$  | $t_{BLC}$ | Byte Load Repeat Cycle Time            |                                      | 0.4 | 50  | $\mu\text{s}$ |
| $t_{WHRH}$  | $t_{WC}$  | Write Cycle Time                       |                                      |     | 5   | ms            |
| $t_{WHRL}$  | $t_{DB}$  | Write Enable High to Ready/Busy Low    | Note 1                               |     | 250 | ns            |
| $t_{EHRL}$  | $t_{DB}$  | Chip Enable High to Ready/Busy Low     | Note 1                               |     | 250 | ns            |
| $t_{DVWH}$  | $t_{DS}$  | Data Valid before Write Enable High    |                                      | 50  |     | ns            |
| $t_{DVEH}$  | $t_{DS}$  | Data Valid before Chip Enable High     |                                      | 50  |     | ns            |

Note: 1. With a 3.3 k $\Omega$  external pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

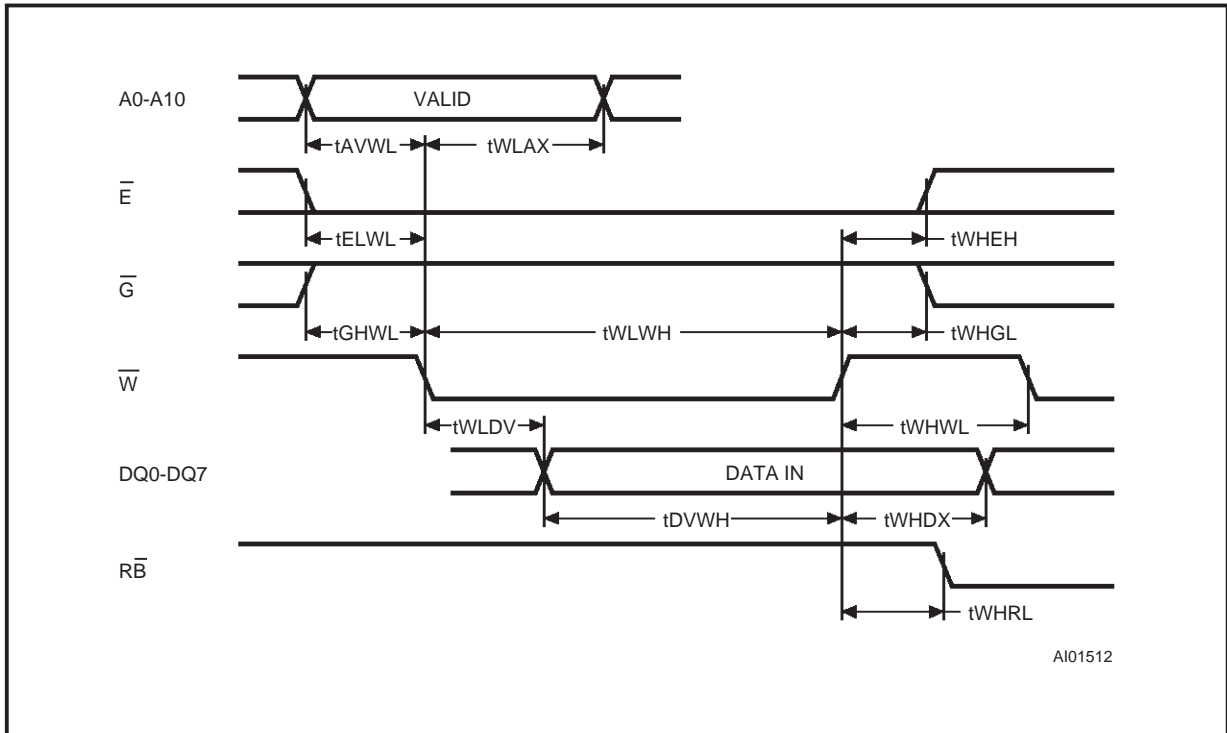


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

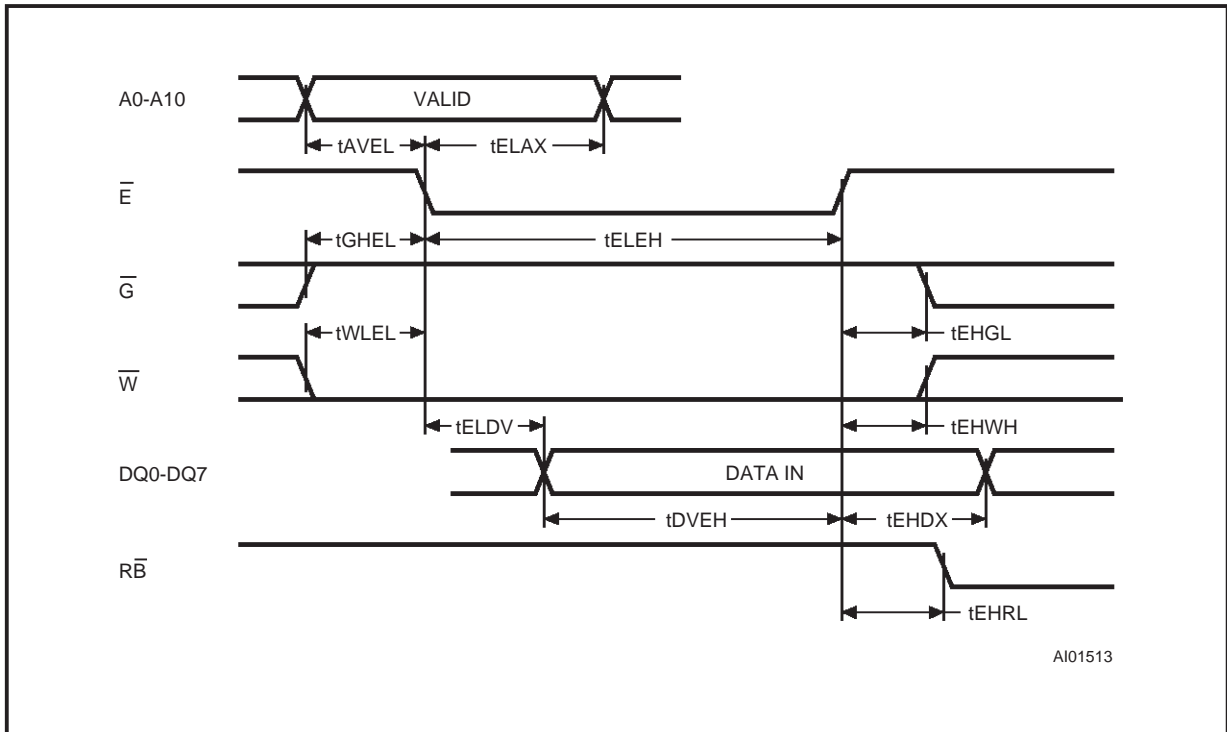


Figure 10. Page Write Mode AC Waveforms - Write Enable Controlled

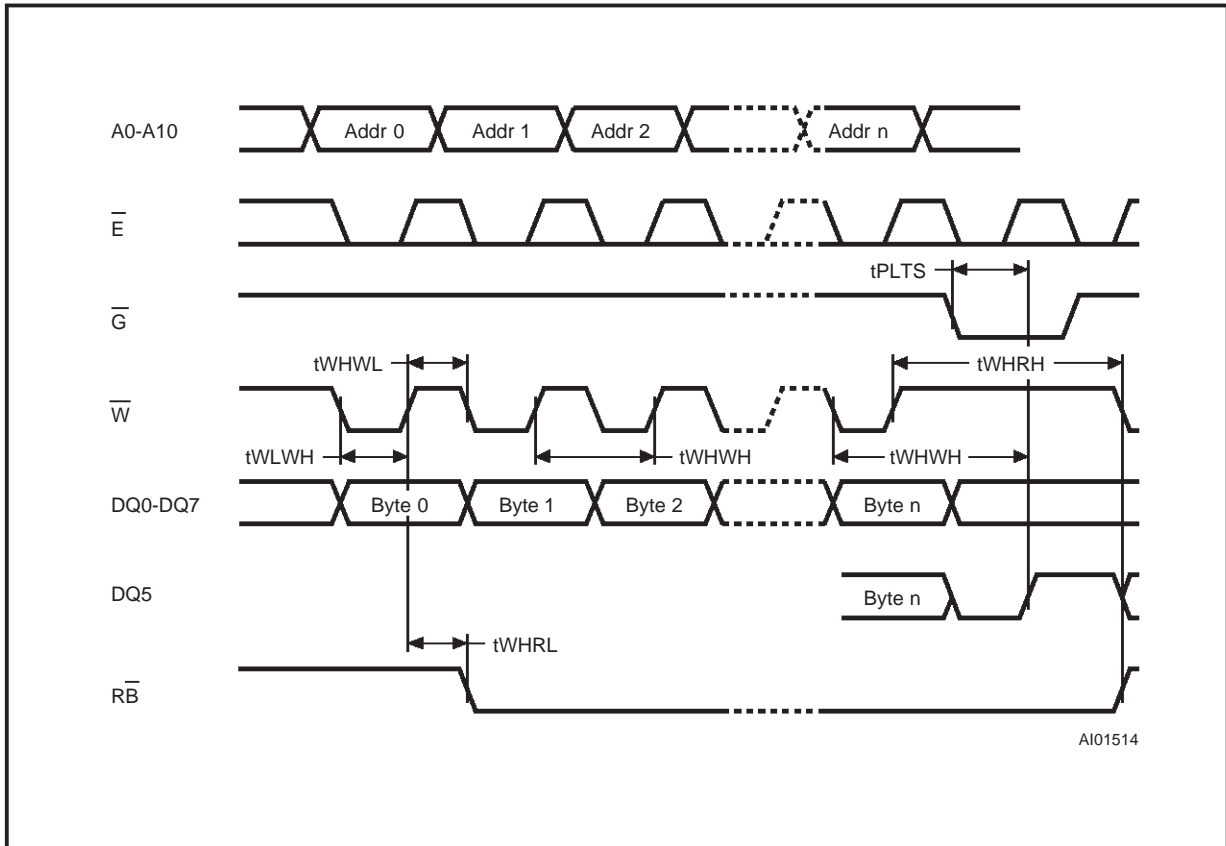


Figure 11. Data Polling Waveform Sequence

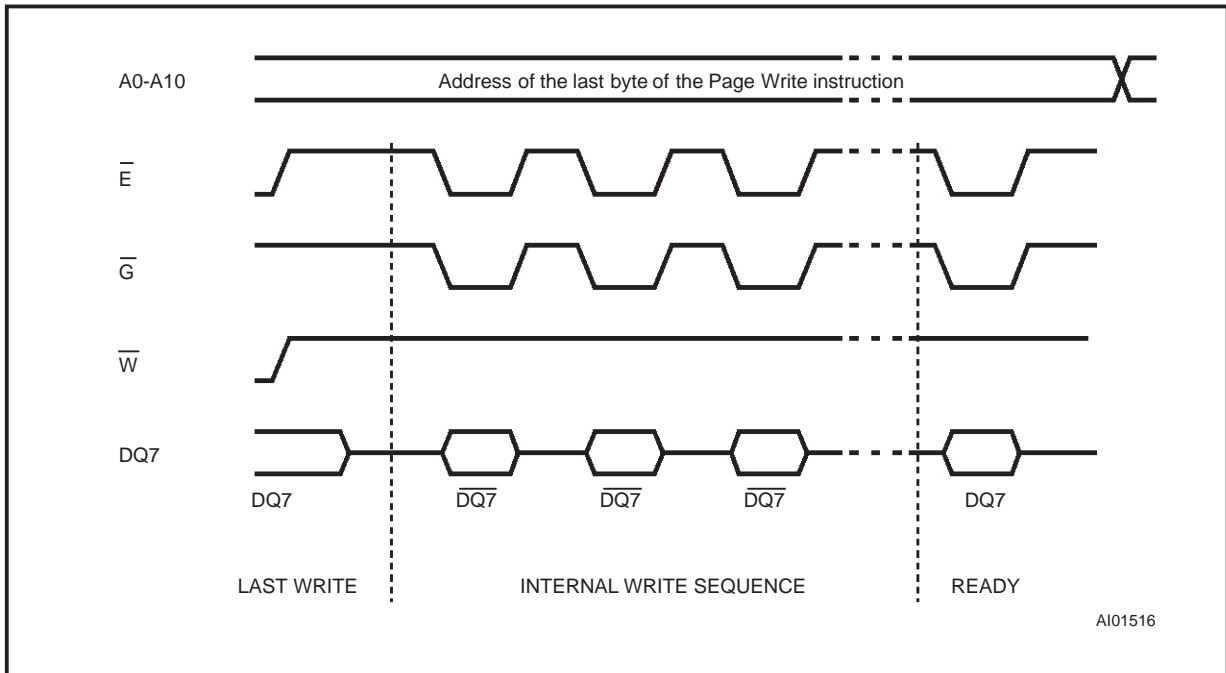
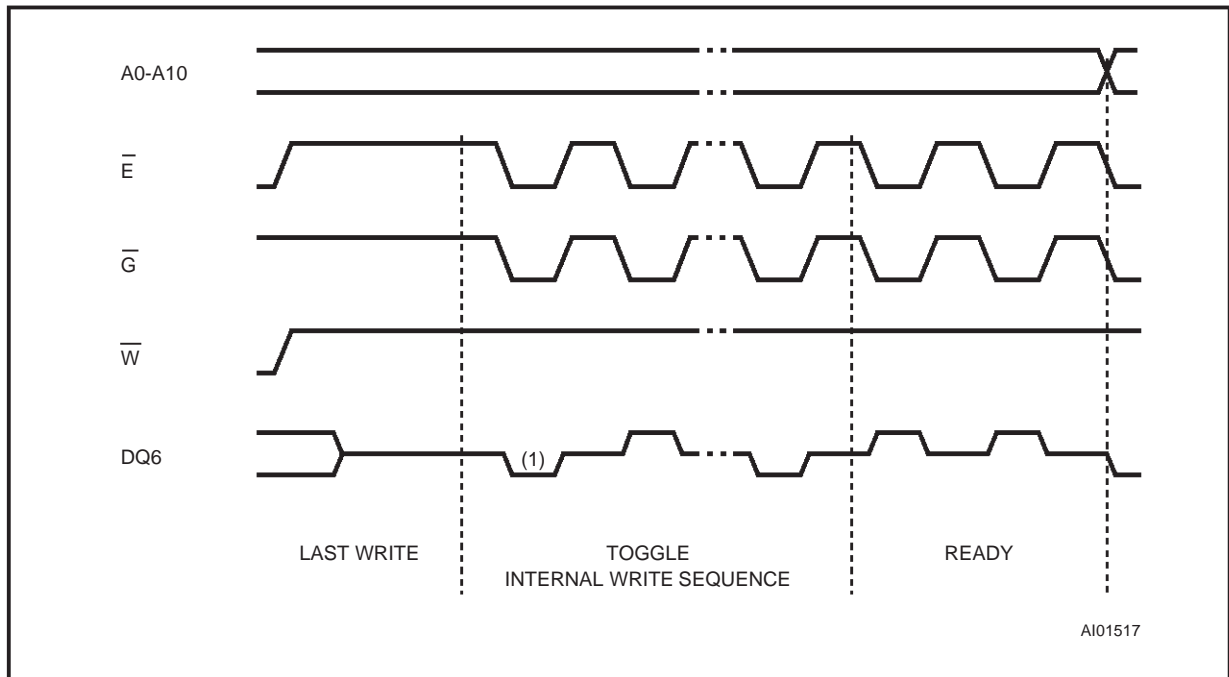
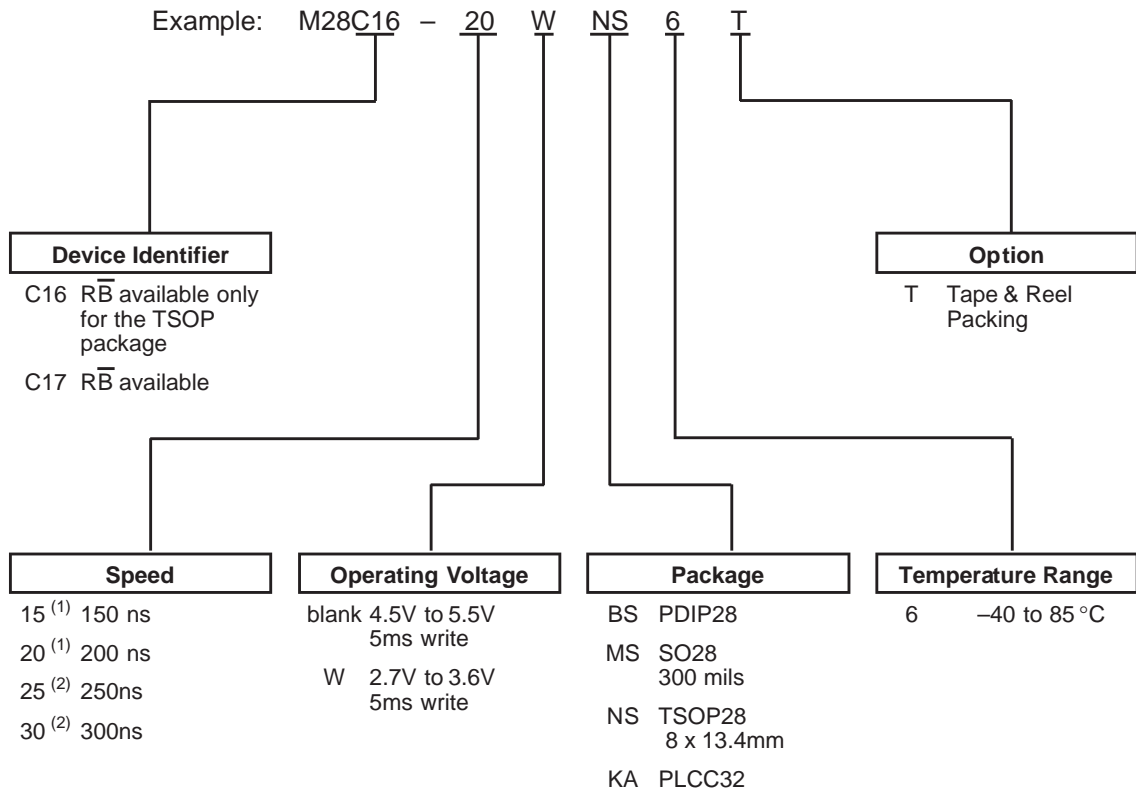


Figure 12. Toggle Bit Waveform Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME



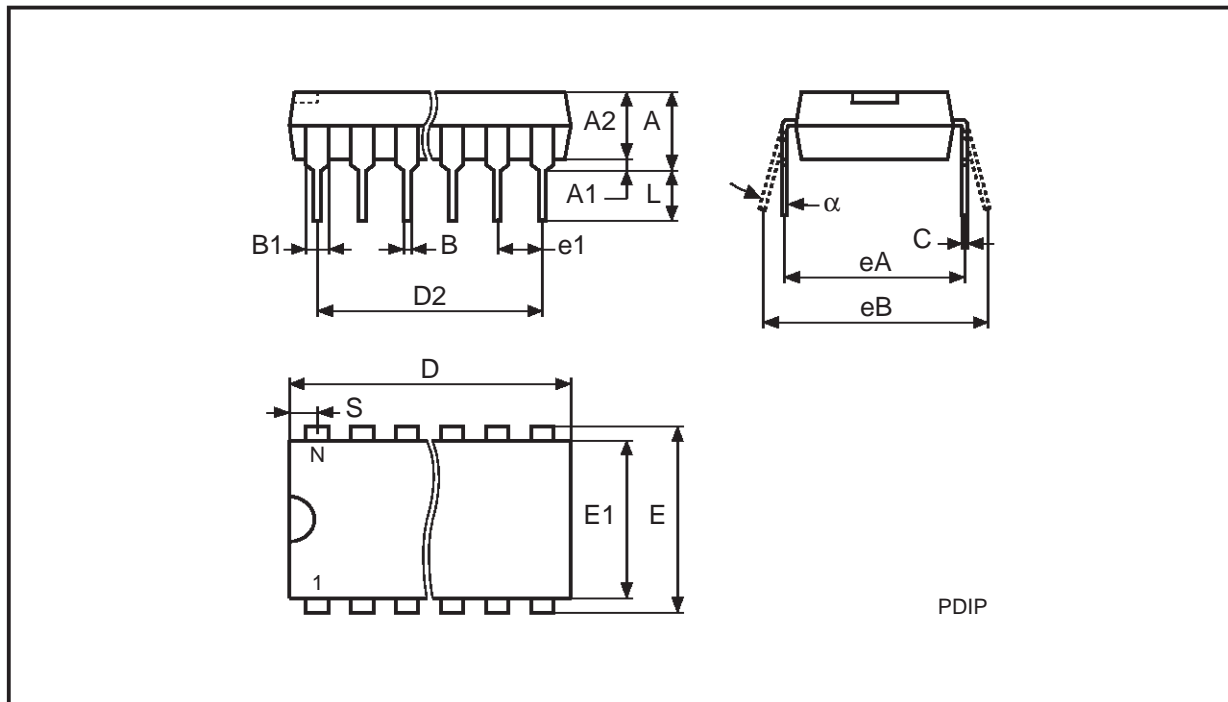
**Notes:** 1. Available for M28C16A and M28C17A only.  
2. Available for "W" Operating Voltage only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

**PDIP28 - 28 pin Plastic DIP, 600 mils width**

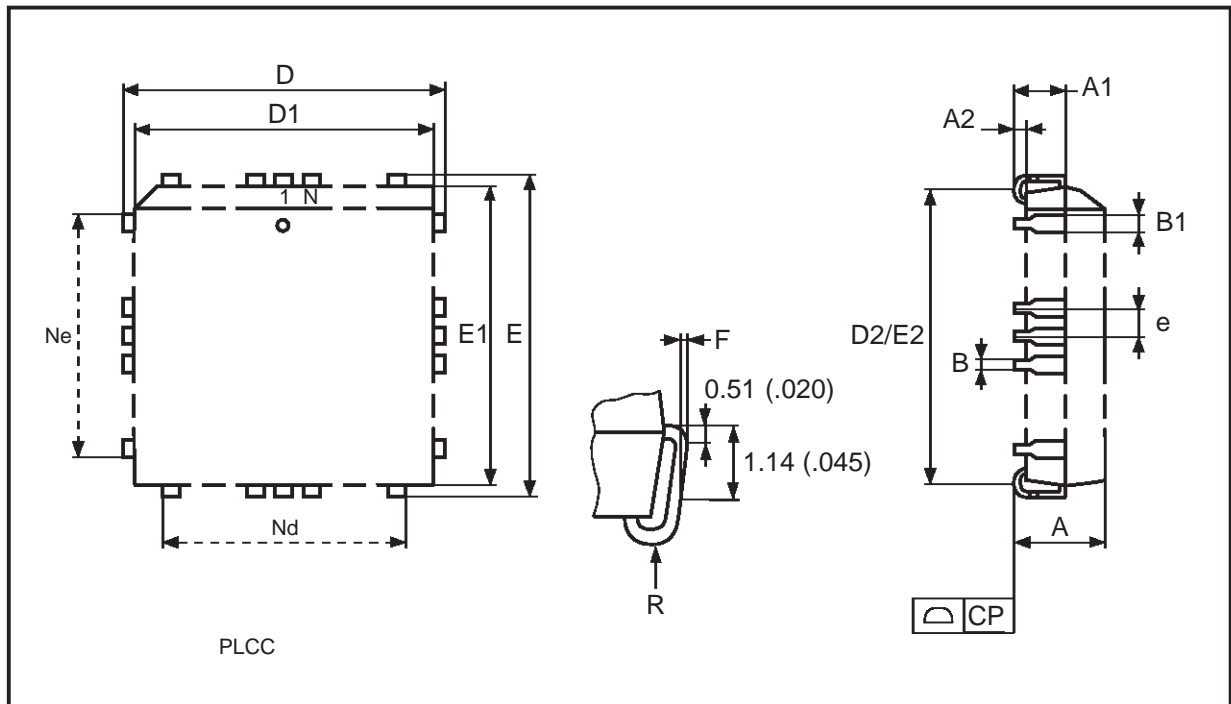
| Symb     | mm    |       |       | inches |       |       |  |
|----------|-------|-------|-------|--------|-------|-------|--|
|          | Typ   | Min   | Max   | Typ    | Min   | Max   |  |
| A        |       | –     | 5.08  |        | –     | 0.200 |  |
| A1       |       | 0.38  | –     |        | 0.015 | –     |  |
| A2       |       | 3.56  | 4.06  |        | 0.140 | 0.160 |  |
| B        |       | 0.38  | 0.51  |        | 0.015 | 0.020 |  |
| B1       | 1.52  | –     | –     | 0.060  | –     | –     |  |
| C        |       | 0.20  | 0.30  |        | 0.008 | 0.012 |  |
| D        |       | 36.83 | 37.34 |        | 1.450 | 1.470 |  |
| D2       | 33.02 | –     | –     | 1.300  | –     | –     |  |
| E        | 15.24 | –     | –     | 0.600  | –     | –     |  |
| E1       |       | 13.59 | 13.84 |        | 0.535 | 0.545 |  |
| e1       | 2.54  | –     | –     | 0.100  | –     | –     |  |
| eA       | 14.99 | –     | –     | 0.590  | –     | –     |  |
| eB       |       | 15.24 | 17.78 |        | 0.600 | 0.700 |  |
| L        |       | 3.18  | 3.43  |        | 0.125 | 0.135 |  |
| S        |       | 1.78  | 2.08  |        | 0.070 | 0.082 |  |
| $\alpha$ |       | 0°    | 10°   |        | 0°    | 10°   |  |
| N        |       | 28    |       |        |       | 28    |  |



Drawing is not to scale.

**PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular**

| Symb | mm   |       |       | inches |       |       |
|------|------|-------|-------|--------|-------|-------|
|      | Typ  | Min   | Max   | Typ    | Min   | Max   |
| A    |      | 2.54  | 3.56  |        | 0.100 | 0.140 |
| A1   |      | 1.52  | 2.41  |        | 0.060 | 0.095 |
| A2   |      | –     | 0.38  |        | –     | 0.015 |
| B    |      | 0.33  | 0.53  |        | 0.013 | 0.021 |
| B1   |      | 0.66  | 0.81  |        | 0.026 | 0.032 |
| D    |      | 12.32 | 12.57 |        | 0.485 | 0.495 |
| D1   |      | 11.35 | 11.56 |        | 0.447 | 0.455 |
| D2   |      | 9.91  | 10.92 |        | 0.390 | 0.430 |
| E    |      | 14.86 | 15.11 |        | 0.585 | 0.595 |
| E1   |      | 13.89 | 14.10 |        | 0.547 | 0.555 |
| E2   |      | 12.45 | 13.46 |        | 0.490 | 0.530 |
| e    | 1.27 | –     | –     | 0.050  | –     | –     |
| F    |      | 0.00  | 0.25  |        | 0.000 | 0.010 |
| R    | 0.89 | –     | –     | 0.035  | –     | –     |
| N    |      | 32    |       |        | 32    |       |
| Nd   |      | 7     |       |        | 7     |       |
| Ne   |      | 9     |       |        | 9     |       |
| CP   |      |       | 0.10  |        |       | 0.004 |

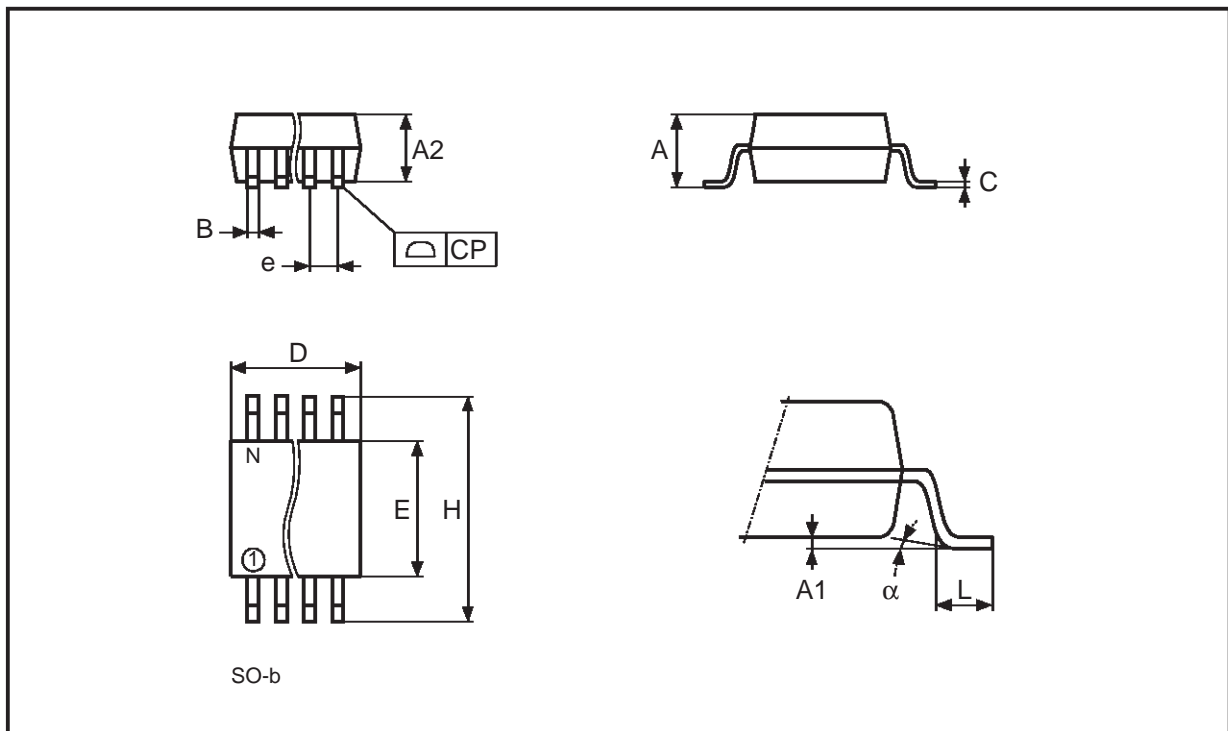


Drawing is not to scale.



## SO28 - 28 lead Plastic Small Outline, 300 mils body width

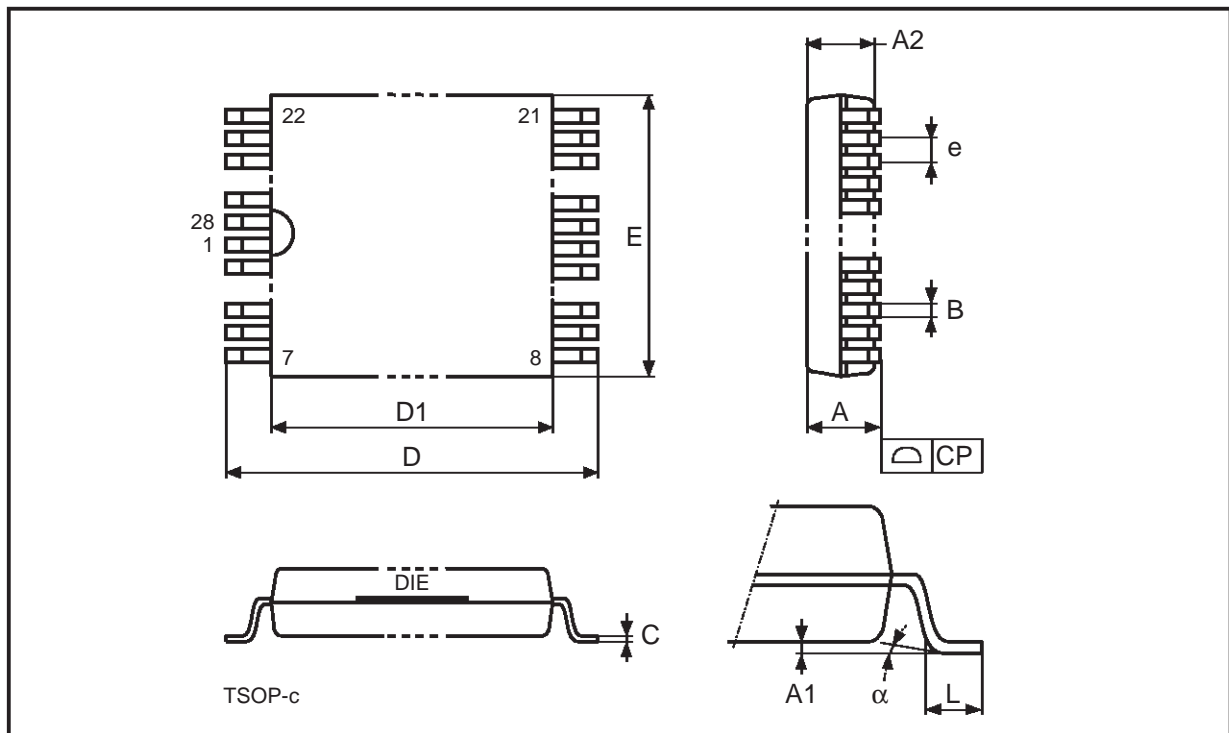
| Symb     | mm   |       |       | inches |       |       |  |
|----------|------|-------|-------|--------|-------|-------|--|
|          | Typ  | Min   | Max   | Typ    | Min   | Max   |  |
| A        |      | 2.46  | 2.64  |        | 0.097 | 0.104 |  |
| A1       |      | 0.13  | 0.29  |        | 0.005 | 0.011 |  |
| A2       |      | 2.29  | 2.39  |        | 0.090 | 0.094 |  |
| B        |      | 0.35  | 0.48  |        | 0.014 | 0.019 |  |
| C        |      | 0.23  | 0.32  |        | 0.009 | 0.013 |  |
| D        |      | 17.81 | 18.06 |        | 0.701 | 0.711 |  |
| E        |      | 7.42  | 7.59  |        | 0.292 | 0.299 |  |
| e        | 1.27 | –     | –     | 0.050  | –     | –     |  |
| H        |      | 10.16 | 10.41 |        | 0.400 | 0.410 |  |
| L        |      | 0.61  | 1.02  |        | 0.024 | 0.040 |  |
| $\alpha$ |      | 0°    | 8°    |        | 0°    | 8°    |  |
| N        |      | 28    |       |        | 28    |       |  |
| CP       |      |       | 0.10  |        |       | 0.004 |  |



Drawing is not to scale.

**TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm**

| Symb     | mm   |       |       | inches |       |       |
|----------|------|-------|-------|--------|-------|-------|
|          | Typ  | Min   | Max   | Typ    | Min   | Max   |
| A        |      |       | 1.25  |        |       | 0.049 |
| A1       |      |       | 0.20  |        |       | 0.008 |
| A2       |      | 0.95  | 1.15  |        | 0.037 | 0.045 |
| B        |      | 0.17  | 0.27  |        | 0.007 | 0.011 |
| C        |      | 0.10  | 0.21  |        | 0.004 | 0.008 |
| D        |      | 13.20 | 13.60 |        | 0.520 | 0.535 |
| D1       |      | 11.70 | 11.90 |        | 0.461 | 0.469 |
| E        |      | 7.90  | 8.10  |        | 0.311 | 0.319 |
| e        | 0.55 | -     | -     | 0.022  | -     | -     |
| L        |      | 0.50  | 0.70  |        | 0.020 | 0.028 |
| $\alpha$ |      | 0°    | 5°    |        | 0°    | 5°    |
| N        | 28   |       |       | 28     |       |       |
| CP       |      |       | 0.10  |        |       | 0.004 |



Drawing is not to scale.

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