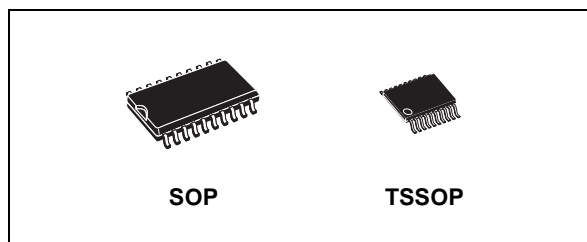




# 74LVX574

## LOW VOLTAGE CMOS OCTAL D-TYPE FLIP-FLOP (3-STATE NON INV.) WITH 5V TOLERANT INPUTS

- HIGH SPEED:  
 $f_{MAX} = 125\text{MHz}$  (TYP.) at  $V_{CC} = 3.3\text{V}$
- 5V TOLERANT INPUTS
- POWER-DOWN PROTECTION ON INPUTS
- INPUT VOLTAGE LEVEL:  
 $V_{IL} = 0.8\text{V}$ ,  $V_{IH} = 2\text{V}$  at  $V_{CC} = 3\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\ \mu\text{A}$  (MAX.) at  $T_A = 25^\circ\text{C}$
- LOW NOISE:  
 $V_{OLP} = 0.3\text{V}$  (TYP.) at  $V_{CC} = 3.3\text{V}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 4\ \text{mA}$  (MIN) at  $V_{CC} = 3\text{V}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}(\text{OPR}) = 2\text{V}$  to  $3.6\text{V}$  (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
SOP	74LVX574M	74LVX574MTR
TSSOP		74LVX574TTR

### DESCRIPTION

The 74LVX574 is a low voltage CMOS OCTAL D-TYPE FLIP-FLOP with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

This 8 bit D-Type flip-flop is controlled by a clock input (CK) and an output enable input ( $\overline{\text{OE}}$ ). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the

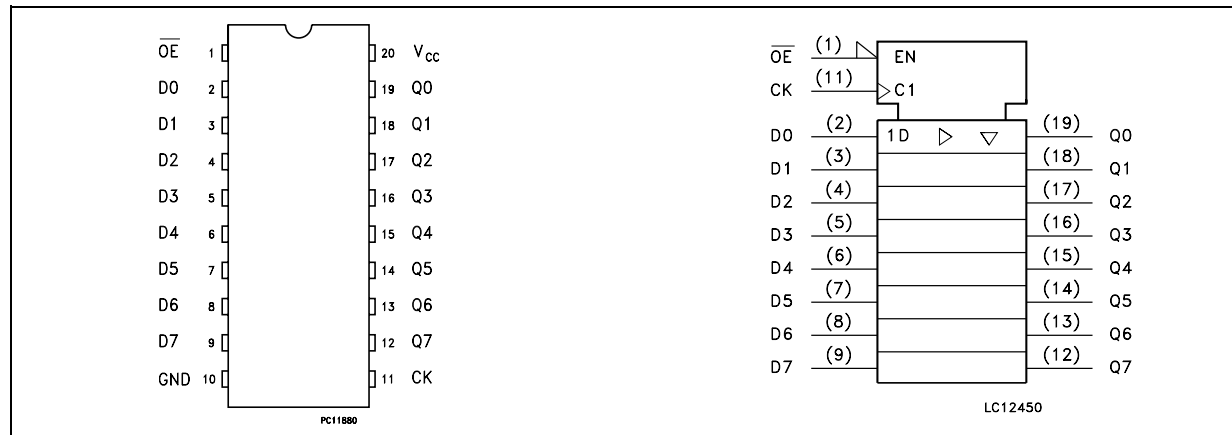
D inputs. While the ( $\overline{\text{OE}}$ ) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state. The output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V. It combines high speed performance with the true CMOS low power consumption.

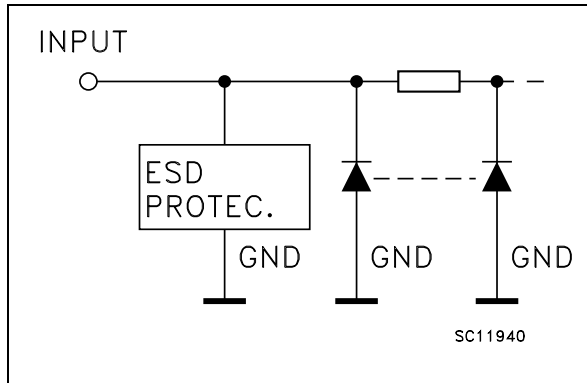
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# 74LVX574

## INPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

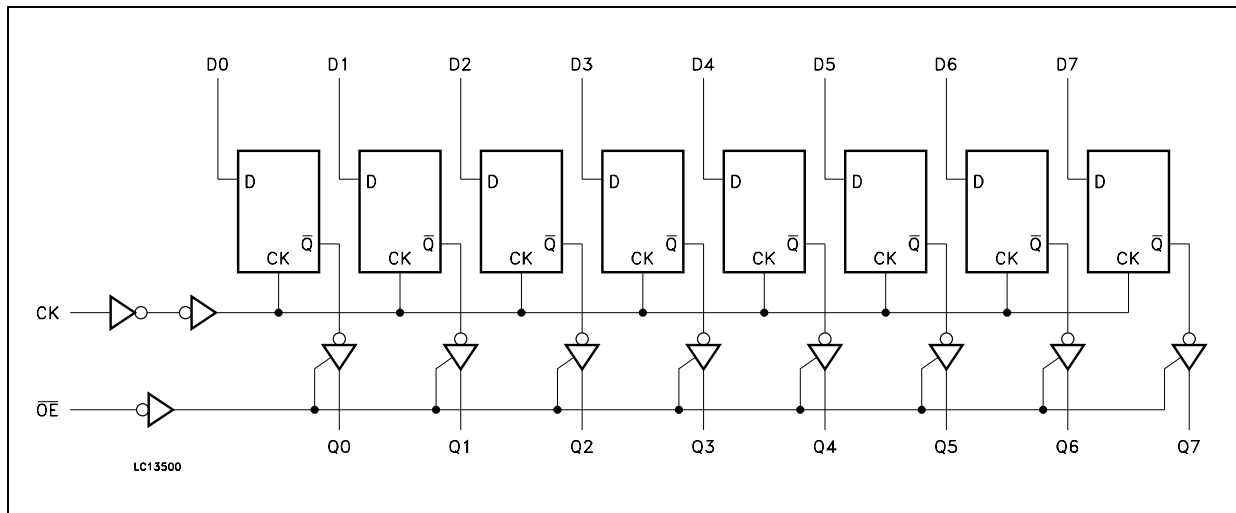
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{OE}}$	3-State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Outputs
11	CK	Clock Input (LOW-to-HIGH Edge Triggered)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

## TRUTH TABLE

INPUTS			OUTPUT
$\overline{\text{OE}}$	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X : Don't Care  
Z : High Impedance

## LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (note 1)	2 to 3.6	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time (note 2) ( $V_{CC} = 3V$ )	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2)  $V_{IN}$  from 0.8V to 2.0V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit		
				$T_A = 25^{\circ}C$			-40 to 85 $^{\circ}C$		-55 to 125 $^{\circ}C$			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
$V_{IH}$	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		3.0			2.0			2.0		2.0		
		3.6			2.4			2.4		2.4		
$V_{IL}$	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		3.0					0.8		0.8		0.8	
		3.6					0.8		0.8		0.8	
$V_{OH}$	High Level Output Voltage	2.0	$I_O = -50 \mu A$	1.9	2.0		1.9		1.9			V
		3.0	$I_O = -50 \mu A$	2.9	3.0		2.9		2.9			
		3.0	$I_O = -4 mA$	2.58			2.48		2.4			
$V_{OL}$	Low Level Output Voltage	2.0	$I_O = 50 \mu A$		0.0	0.1		0.1		0.1		V
		3.0	$I_O = 50 \mu A$		0.0	0.1		0.1		0.1		
		3.0	$I_O = 4 mA$			0.36		0.44		0.55		
$I_{OZ}$	High Impedance Output Leakage Current	3.6	$V_I = V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND			$\pm 0.25$		$\pm 2.5$		$\pm 2.5$	$\mu A$	
$I_I$	Input Leakage Current	3.6	$V_I = 5V$ or GND			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu A$	
$I_{CC}$	Quiescent Supply Current	3.6	$V_I = V_{CC}$ or GND			4		40		40	$\mu A$	

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C <sub>L</sub> = 50 pF		0.3	0.8					V
V <sub>OLV</sub>				-0.8	-0.3						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	3.3		2.0							
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CK to Q	2.7	15		9.2	14.5	1.0	17.5	1.0	17.5	ns
		2.7	50		11.5	18.0	1.0	21.0	1.0	21.0	
		3.3(*)	15		8.5	13.2	1.0	15.5	1.0	15.5	
		3.3(*)	50		11.0	16.7	1.0	19.0	1.0	19.0	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	2.7	15		9.8	15.0	1.0	18.5	1.0	18.5	ns
		2.7	50		11.4	18.5	1.0	22.0	1.0	22.0	
		3.3(*)	15		8.2	12.8	1.0	15.0	1.0	15.0	
		3.3(*)	50		10.7	16.3	1.0	18.5	1.0	18.5	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	2.7	50		12.1	19.1	1.0	22.0	1.0	22.0	ns
		3.3(*)	50		11.0	15.0	1.0	17.0	1.0	17.0	
t <sub>w</sub>	CK pulse Width, HIGH	2.7	50		6.5			7.5		7.5	ns
		3.3(*)	50		5.0			5.0		5.0	
t <sub>s</sub>	Setup Time D to CK HIGH or LOW	2.7	50		5.0			5.0		5.0	ns
		3.3(*)	50		3.5			3.5		3.5	
t <sub>h</sub>	Hold Time D to CK HIGH or LOW	2.7	50		1.5			1.5		1.5	ns
		3.3(*)	50		1.5			1.5		1.5	
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	15		60	115		50		48	MHz
		2.7	50		45	60		40		40	
		3.3(*)	15		80	125		65		60	
		3.3(*)	50		50	75		45		40	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew Time (note 1,2)	2.7	50		0.5	1.0		1.5		1.5	ns
		3.3(*)	50		0.5	1.0		1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

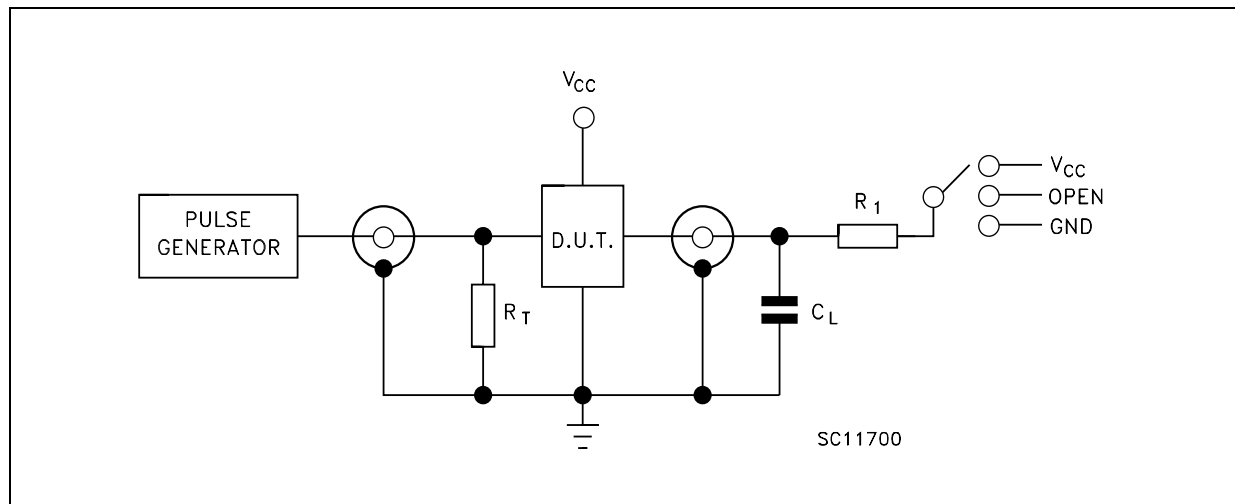
(\*) Voltage range is 3.3V ± 0.3V

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	3.3			4	10		10		10	pF
C <sub>OUT</sub>	Output Capacitance	3.3			6						pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	3.3	f <sub>IN</sub> = 10MHz		27						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$  (per circuit)

## TEST CIRCUIT



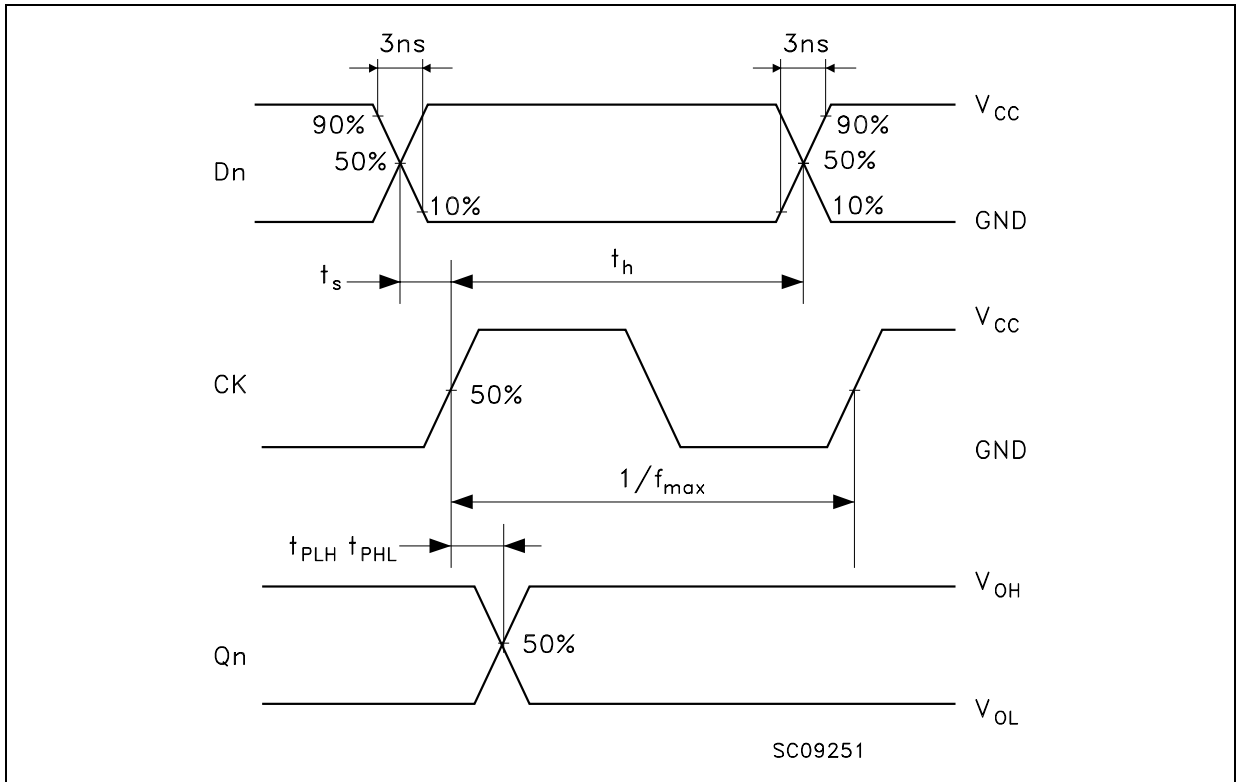
TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	V <sub>CC</sub>
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

C<sub>L</sub> = 15/50pF or equivalent (includes jig and probe capacitance)

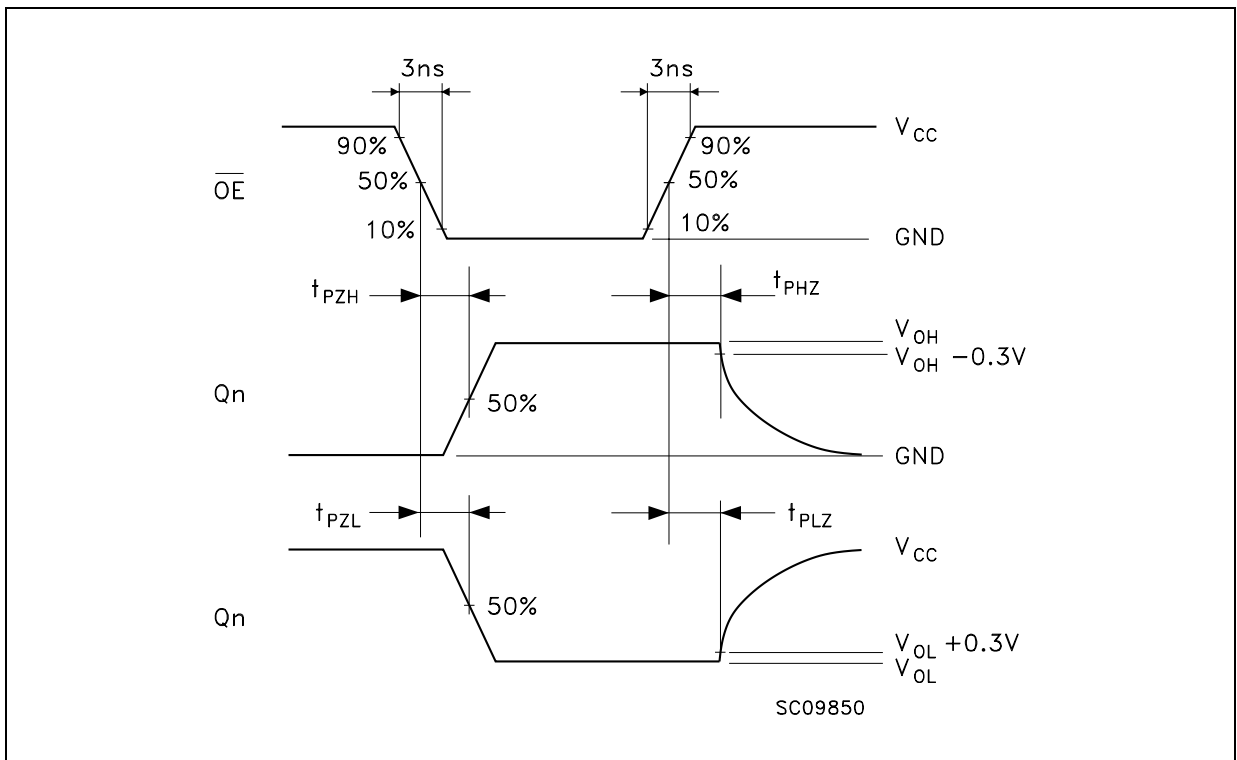
R<sub>L</sub> = R<sub>1</sub> = 1KΩ or equivalent

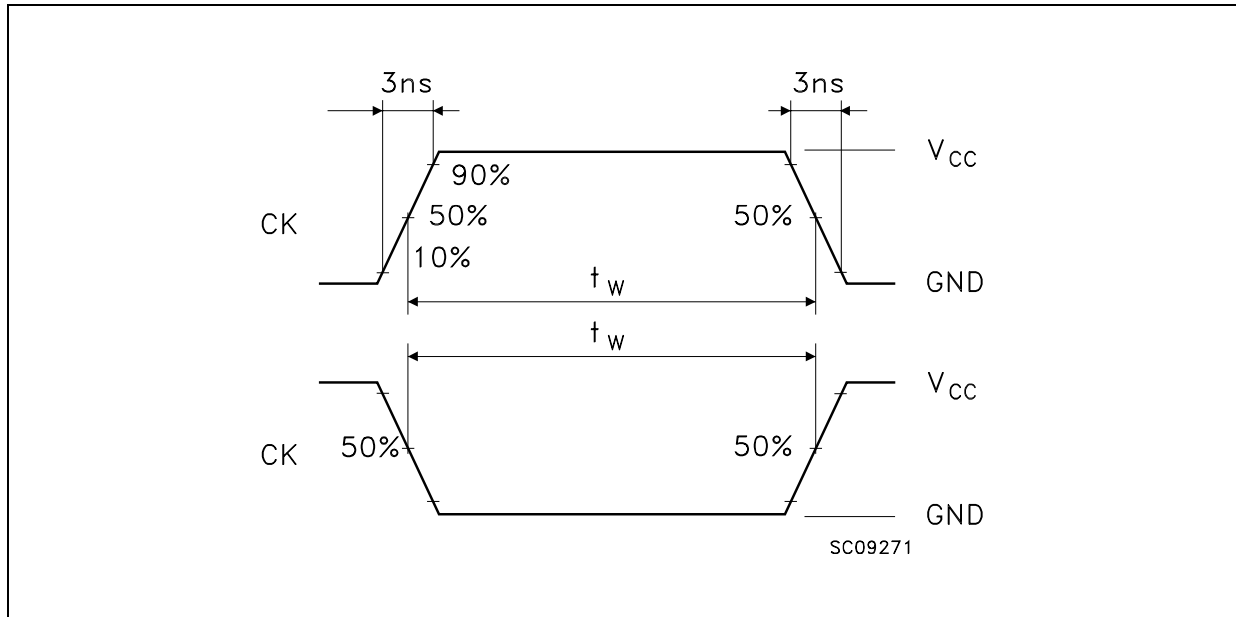
R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAYS SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



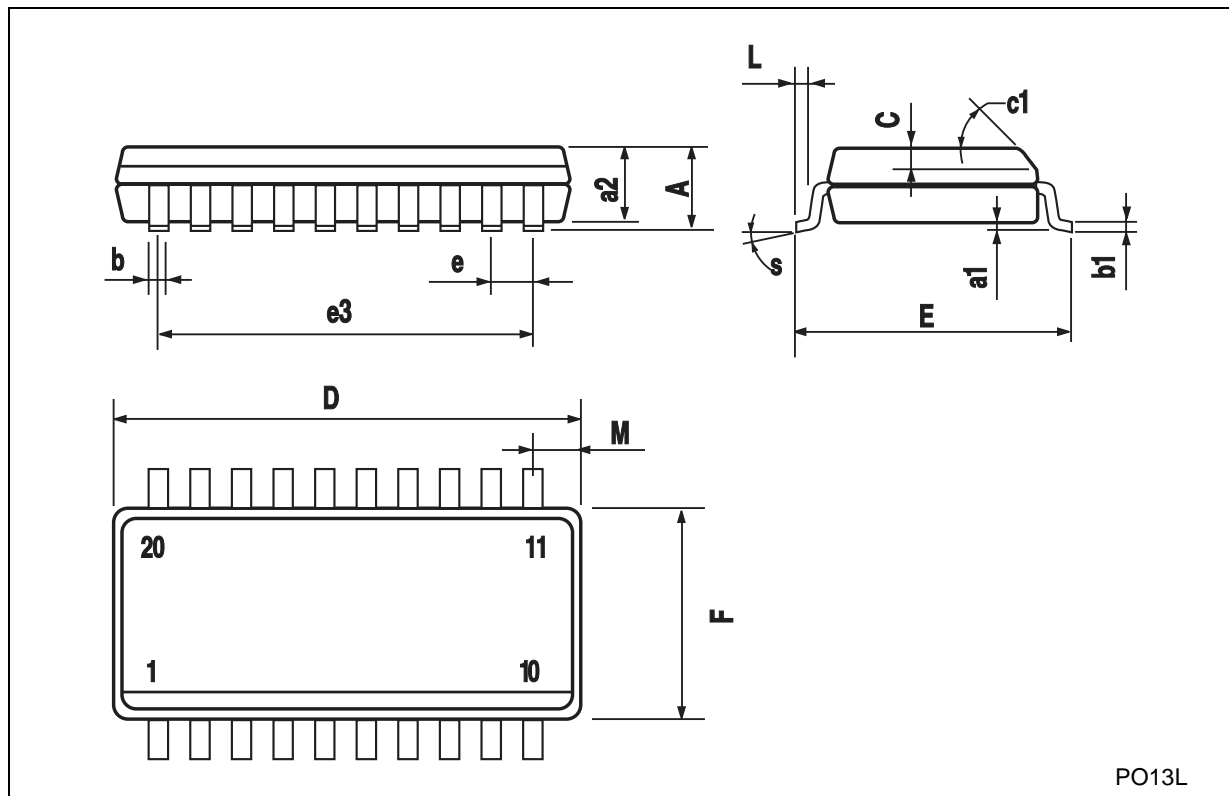
WAVEFORM 2 : OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)



**WAVEFORM 3 : CK MINIMUM PULSE WIDTH** (f=1MHz; 50% duty cycle)

## SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L



## TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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