

CXK591000TM/YM/M -55LL/70LL/10LL

131,072-word × 9-bit High Speed CMOS Static RAM

Description

The CXK591000TM/YM/M is a high speed CMOS static RAM organized as 131,072-words by 9 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Special feature are low power consumption and high speed.

The CXK591000TM/YM/M is a suitable RAM for portable equipment with battery back up and parity bit.

Features

- Fast access time

CXK591000TM/YM/M	(Access time)
-55LL	55ns (Max.)
-70LL	70ns (Max.)
-10LL	100ns (Max.)

- Low standby current

CXK591000TM/YM/M	
-55LL/70LL/10LL	24µA (Max.)

- Low data retention current

CXK591000TM/YM/M	
-55LL/70LL/10LL	14µA (Max.)

- Single +5V supply: 5V ± 10%.

- Low voltage data retention: 2.0V (Min.)

- Broad package line-up

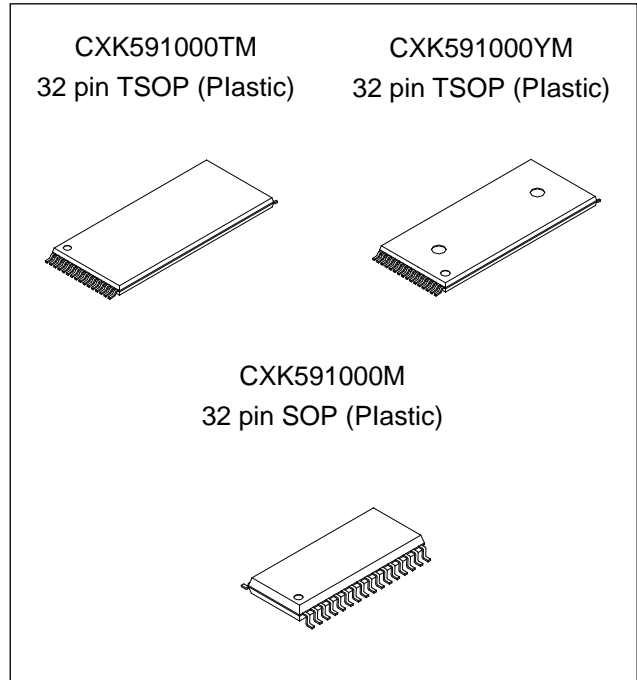
CXK591000TM/YM	8mm × 20mm 32 pin TSOP Package
CXK591000M	525mil 32 pin SOP Package

Function

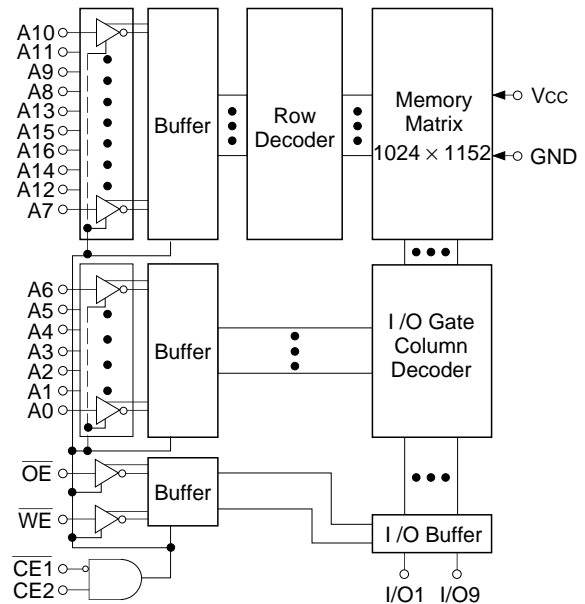
131072 word × 9 bit static RAM

Structure

Silicon gate CMOS IC

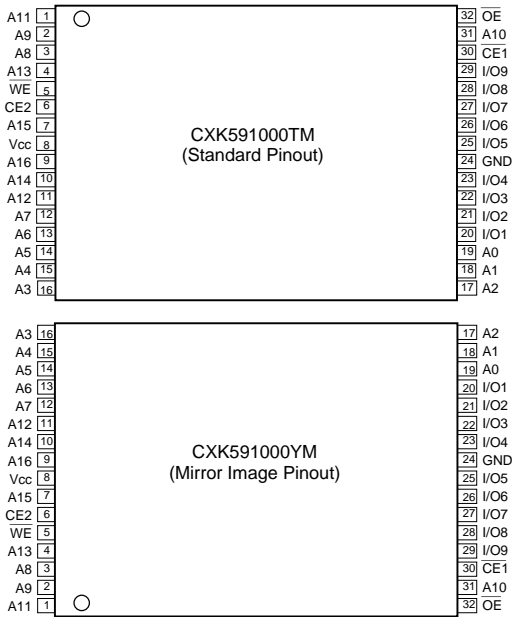


Block Diagram



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O9	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5* to Vcc + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to Vcc + 0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature · time	T _{solder}	235 · 10	°C · s

* V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	Vcc Current
H	×	×	×	Not selected	High Z	IsB1, IsB2
×	L	×	×	Not selected	High Z	IsB1, IsB2
L	H	H	H	Output disable	High Z	Icc1, Icc2, Icc3
L	H	L	H	Read	Data out	Icc1, Icc2, Icc3
L	H	×	L	Write	Data in	Icc1, Icc2, Icc3

×: "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• **DC Characteristics**

(V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	System	Test conditions	Min.	Typ.*	Max.	Unit	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	+1	μA	
Output leakage current	I _{LO}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}	-1	—	+1	μA	
Operating power supply current	I _{CC1}	$\overline{CE1} = V_{IL}$, CE2 = V _{IH} V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA	—	8	17	mA	
Average operating current	I _{CC2}	Min. cycle duty = 100% I _{OUT} = 0mA	-55LL	—	50	100	mA
			-70LL	—	45	80	
			-10LL	—	40	70	
Standby current	I _{SB1}	CE2 ≤ 0.2V CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	0 to +70°C	—	—	24	μA
			0 to +40°C	—	—	5	
			+25°C	—	0.8	2.4	
	I _{SB2}	$\overline{CE1} = V_{IH}$ or CE2 = V _{IL}	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V	

* V_{CC} = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

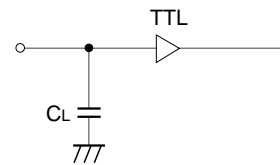
AC Characteristics

• **AC test conditions**

(V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

• **Test circuit**

Item	Conditions	
Input pulse high level	V _{IH} = 2.2V	
Input pulse low level	V _{IL} = 0.8V	
Input rise time	tr = 5ns	
Input fall time	tf = 5ns	
Input and output reference level	1.5V	
Output load conditions	-55LL	C _L * = 30pF, 1TTL
	-70LL/10LL	C _L * = 100pF, 1TTL



* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	-55LL		-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	55	—	70	—	100	—	ns
Address access time	t_{AA}	—	55	—	70	—	100	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	55	—	70	—	100	ns
Chip enable access time (CE2)	t_{CO2}	—	55	—	70	—	100	ns
Output enable to output valid	t_{OE}	—	30	—	40	—	50	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1} , t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1} , t_{HZ2}^*	—	25	—	25	—	35	ns
Output disable to output in high Z (\overline{OE})	t_{OHZ}^*	—	25	—	25	—	35	ns

* t_{HZ1} , t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

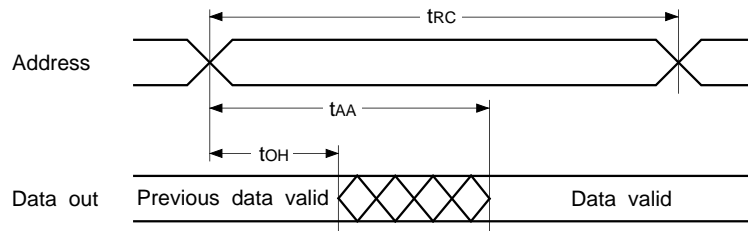
• Write cycle

Item	Symbol	-55LL		-70LL		-10LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	55	—	70	—	100	—	ns
Address valid to end of write	t_{AW}	50	—	60	—	70	—	ns
Chip enable to end of write	t_{CW}	50	—	60	—	70	—	ns
Data to write time overlap	t_{DW}	25	—	30	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	40	—	50	—	60	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}^*	—	25	—	25	—	30	ns

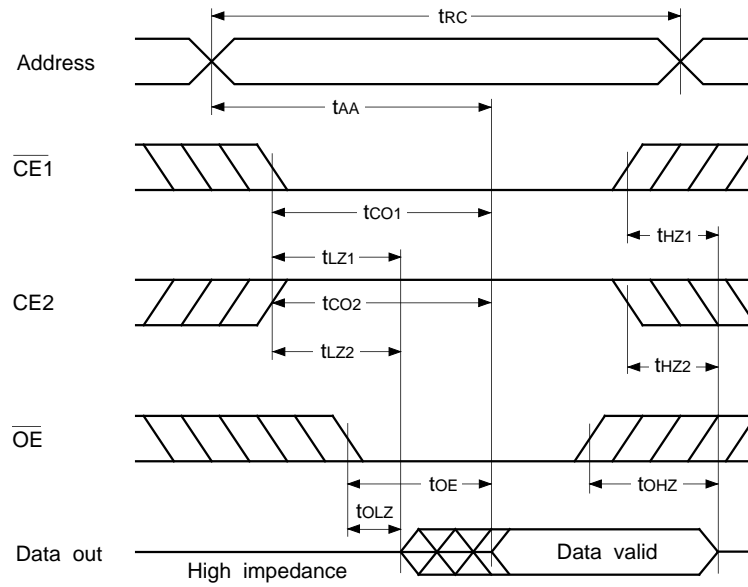
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

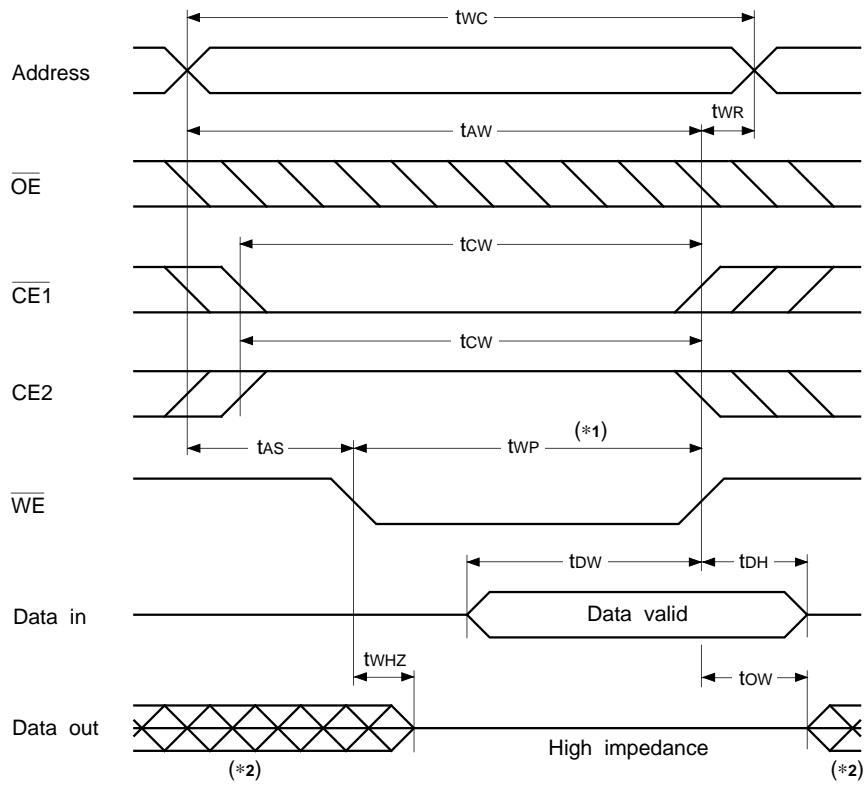
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



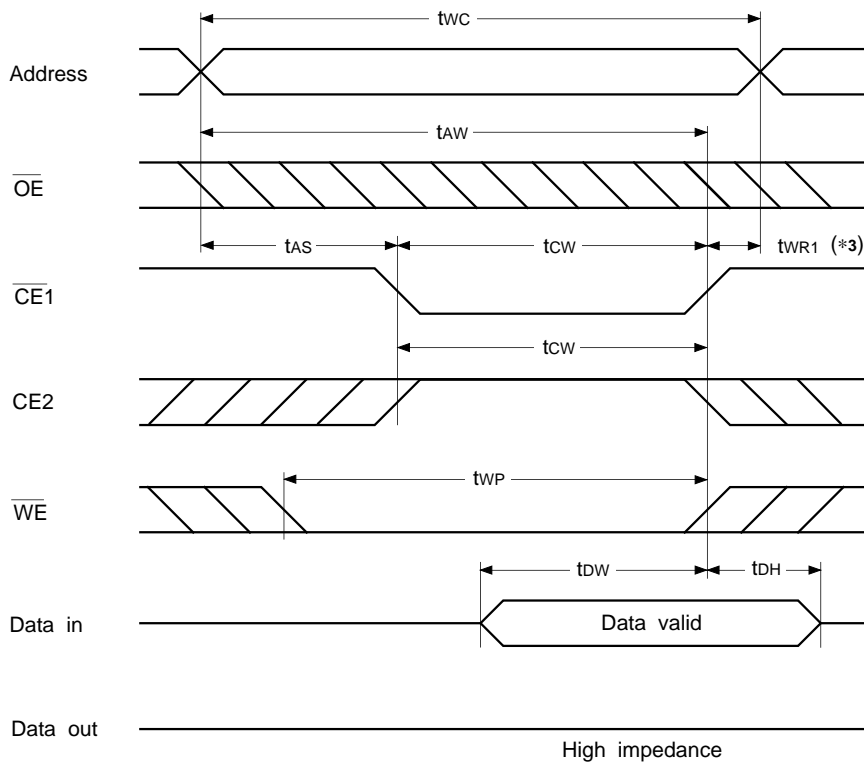
- Read cycle (2) : $\overline{WE} = V_{IH}$



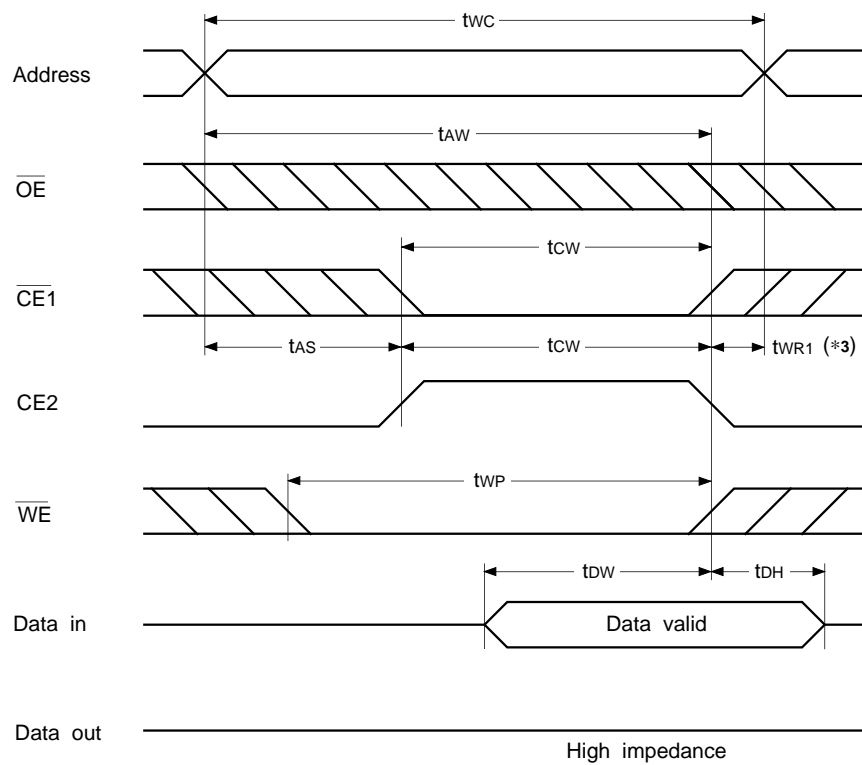
• Write cycle (1) : \overline{WE} control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



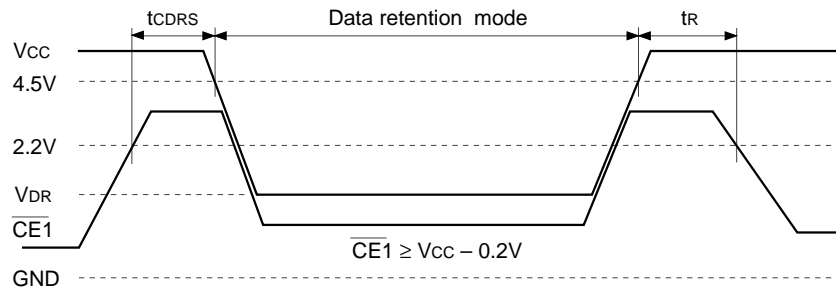
*1 Write is executed when both $\overline{CE1}$ and \overline{WE} are at low and CE2 is at high simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

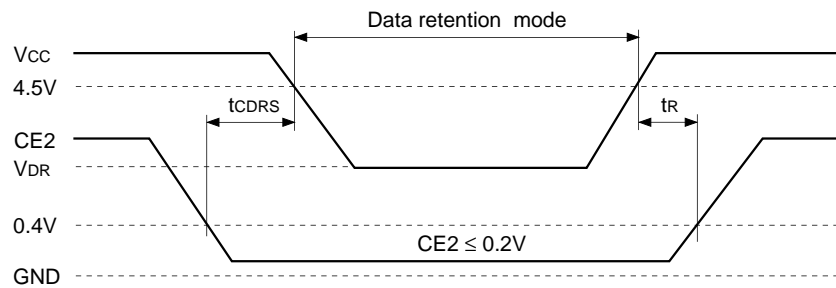
*3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



- Low supply voltage data retention waveform (2) (CE2 control)



Data Retention Characteristics

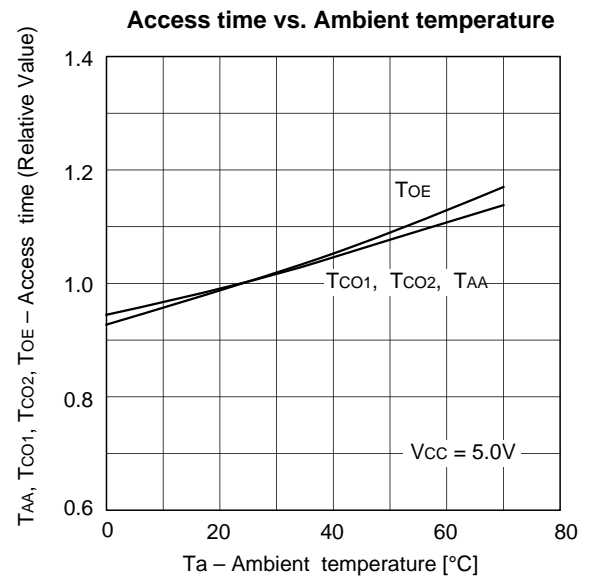
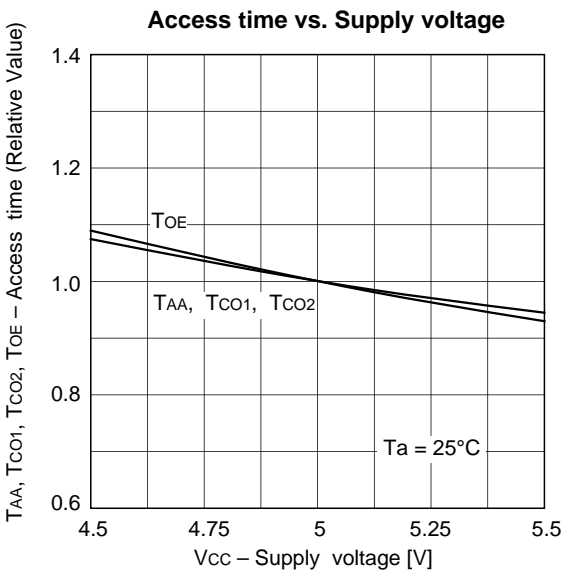
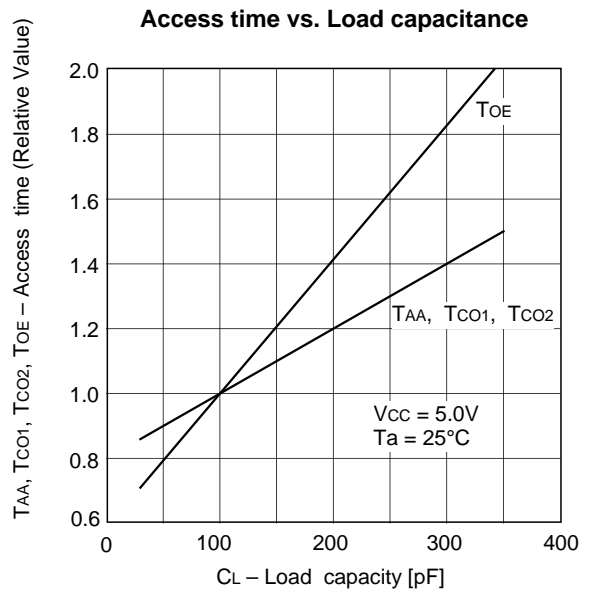
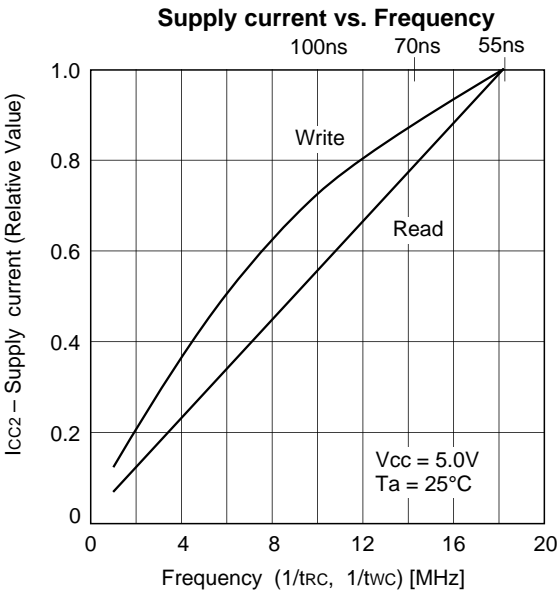
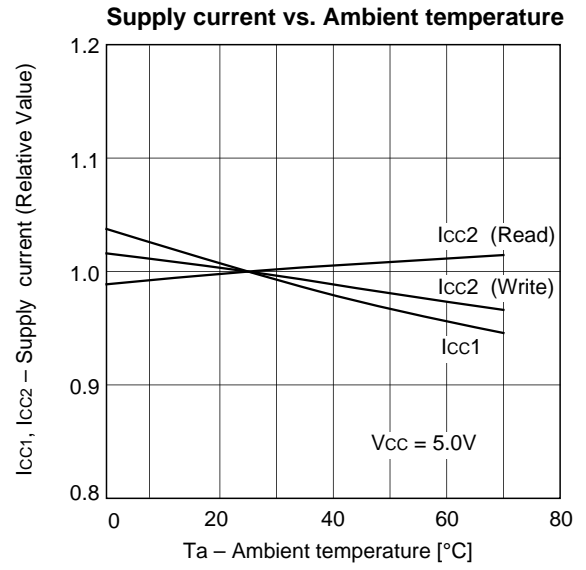
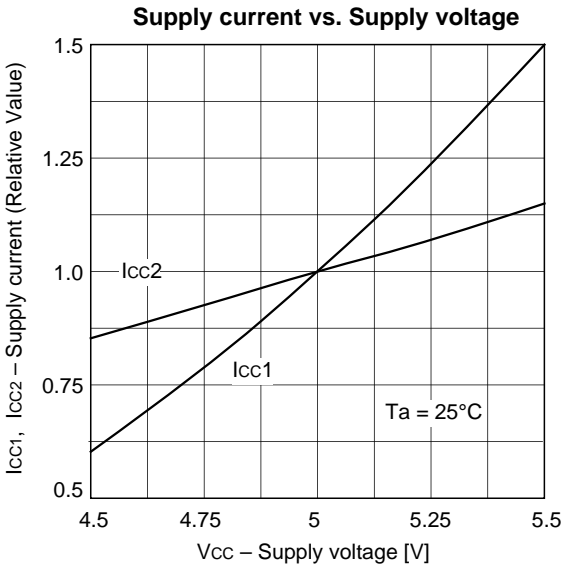
($T_a = 0$ to $+70^\circ\text{C}$)

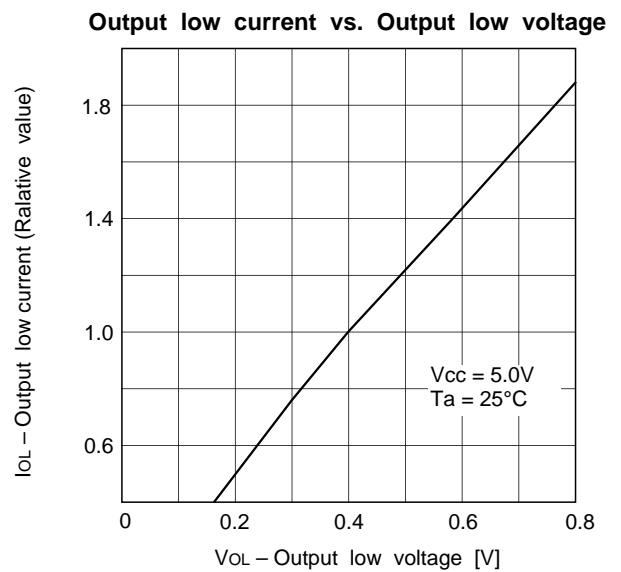
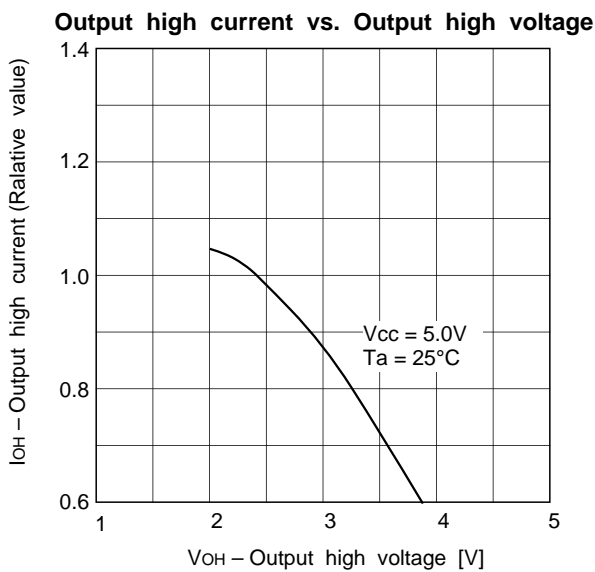
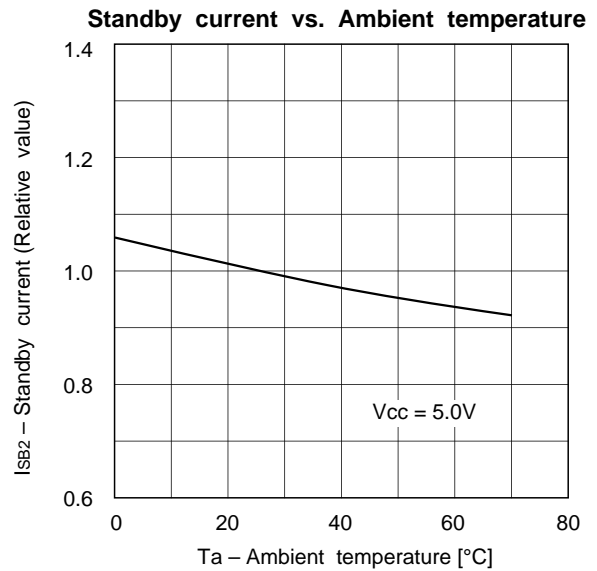
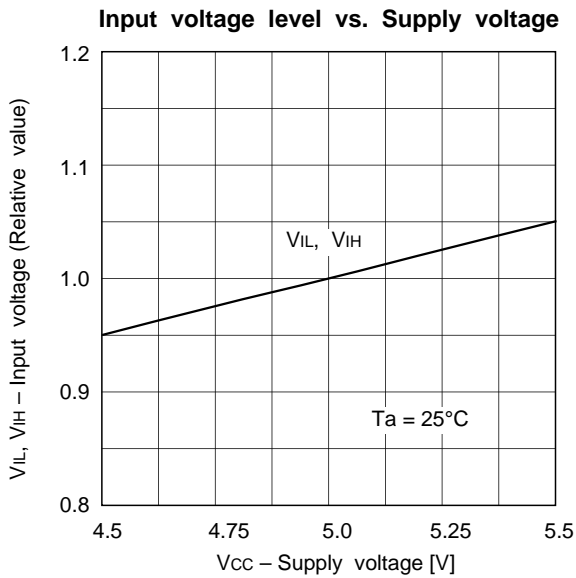
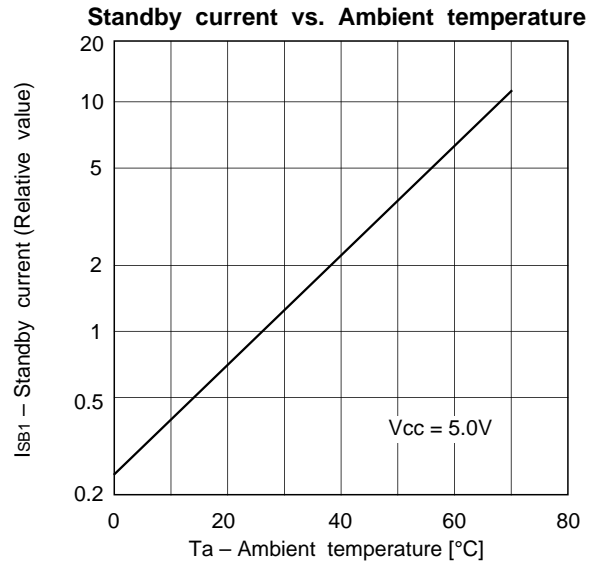
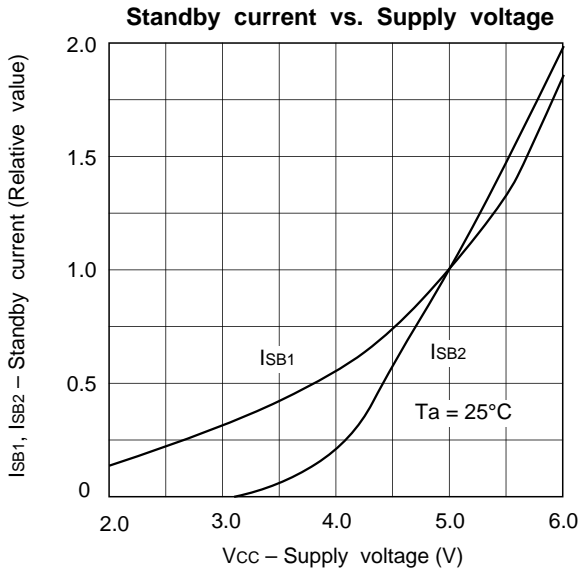
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit	
Data retention voltage	V_{DR}	*1	2.0	—	5.5	V	
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V}^{*1}$	0 to $+70^\circ\text{C}$	—	—	14	μA
			0 to $+40^\circ\text{C}$	—	—	3	
			$+25^\circ\text{C}$	—	0.5	1.4	
	I_{CCDR2}	$V_{CC} = 2.0$ to 5.5V^{*1}	—	0.8^{*2}	24	μA	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t_R		5	—	—	ms	

*1 $\overline{CE1} \geq V_{CC} - 0.2\text{V}$, $CE2 \geq V_{CC} - 0.2\text{V}$ ($\overline{CE1}$ control) or $CE2 \leq 0.2\text{V}$ (CE2 control)

*2 $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

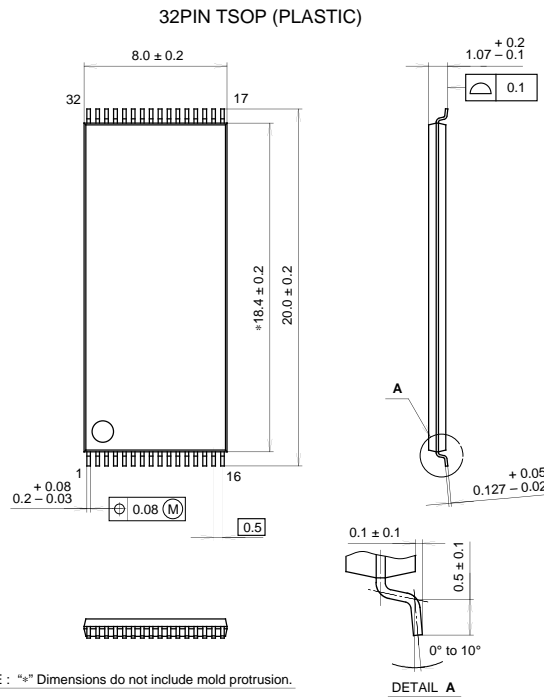
Example of Representative Characteristics





Package Outline Unit: mm

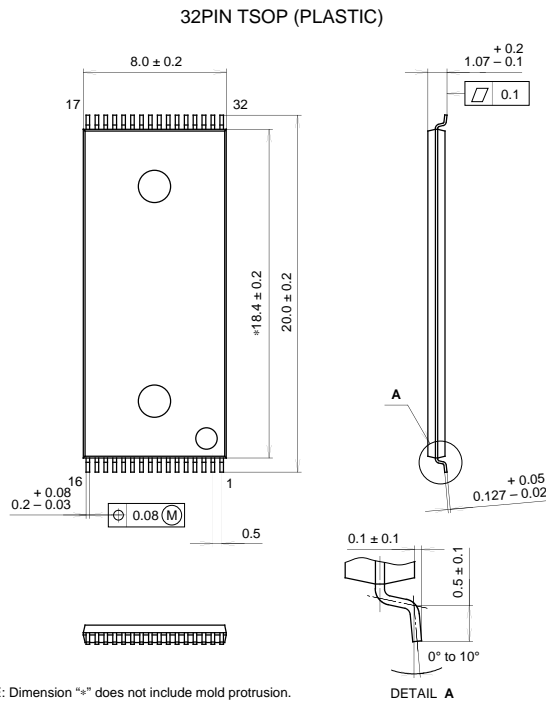
CXK591000TM



PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	TSOP032-P-0820	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE		LEAD MATERIAL	42 ALLOY
		PACKAGE WEIGHT	0.3g

CXK591000YM

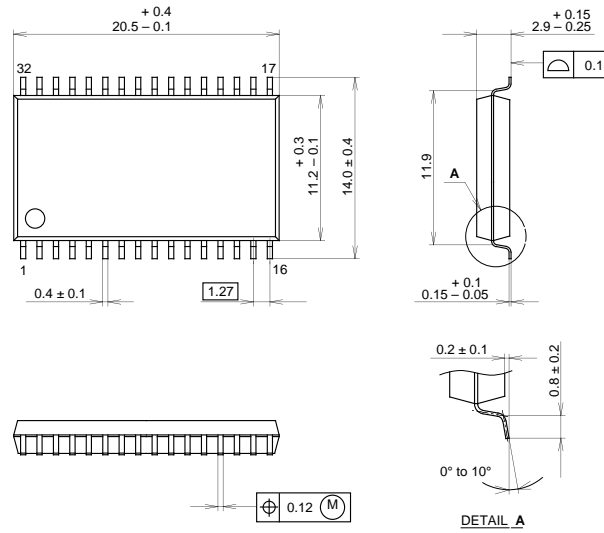


PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01R	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	TSOP032-P-0820-B	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE		LEAD MATERIAL	42 ALLOY
		PACKAGE WEIGHT	0.3g

CXK591000M

32PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	SOP032-P-0525
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.2g