SiI140/SiI140A
PanelLink® Digital Transmitter

Silicon Image

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General Description

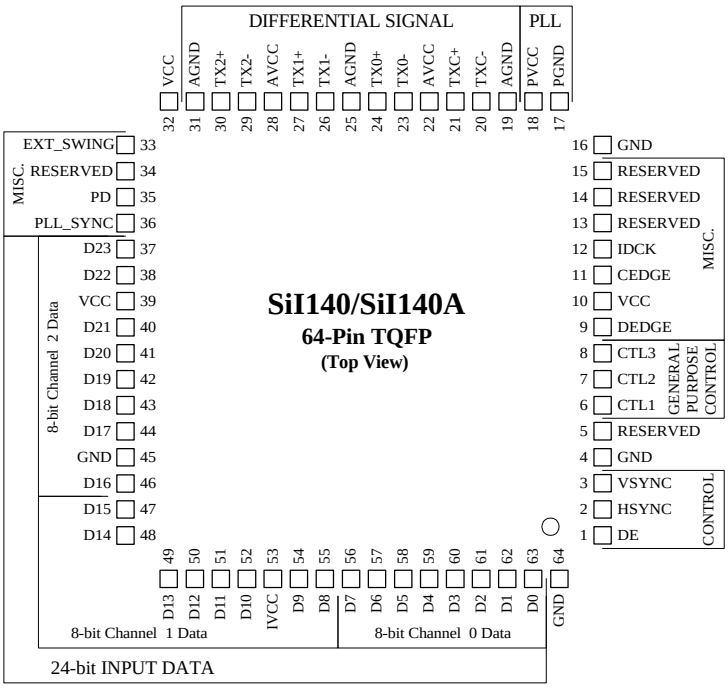
Ideal for LCD desktop monitor applications, the SiI140/SiI140A uses PanelLink Digital technology to support displays ranging from VGA to High Refresh XGA (25-86 MHz). The SiI140/SiI140A transmitter supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 pixel/clock mode and also features an inter-pair skew tolerance up to 1 full input clock cycle and a highly jitter tolerant PLL design. Since all PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed digital design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

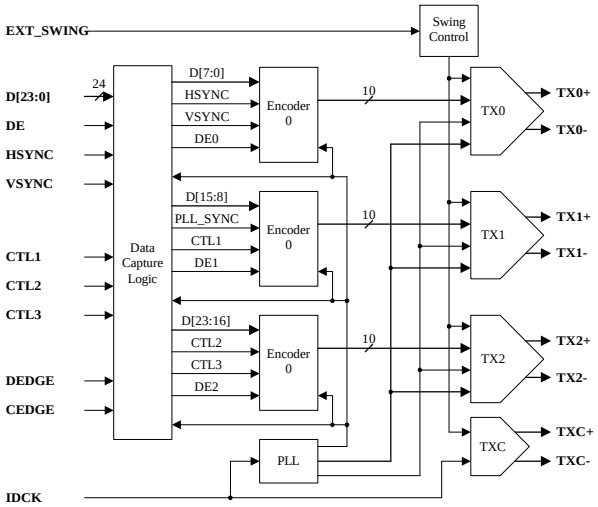
Features

- High Bandwidth: 25-86 MHz (VGA to High Refresh SXGA)
- Low Power: 3.3V core operation & power-down mode
- High Skew Tolerance: 1 full input clock cycle (15ns at 65 MHz)
- Pin-compatible with SiI100
- Sync Detect: for Plug & Display "Hot Plugging"
- Cable Distant Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)

SiI140/SiI140A Pin Diagram



Functional Block Diagram



PanelLink™ DIGITAL

Absolute Maximum Conditions

Note: Permanent device damage may occur if absolute maximum conditions are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3	4.0	V
V_I	Input Voltage	-0.3	V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3	V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25	105	°C
T_{STG}	Storage Temperature	-40	125	°C
P_{PD}	Package Power Dissipation		1	W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Core Supply Voltage applies to VCC, AVCC, PVCC	3.00	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

Note: [1] Guaranteed by design.

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{IL}	Input Leakage Current		-10		10	µA

Note: [1] Guaranteed by design.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 Ω R_{EXT_SWING} = 850 Ω R_{EXT_SWING} = 680 Ω R_{EXT_SWING} = 400 Ω	 250 310 580	 300 370 650	 350 430 720	 mV mV mV
V_{DOH}	Differential High-level Output Voltage			AVCC		V
I_{DOS}	Differential Short Circuit Current	V_{OUT} = 0 V			5	µA
I_{PD}	Power-down Current[3]				25	µA
I_{CCT}	Transmitter Supply Current	IDCK = 86 MHz R_{EXT_SWING} = 680 Ω Typical Pattern[1]		52	65	mA
		DCLK = 86 MHz R_{EXT_SWING} = 680 Ω Worst Case Pattern[2]		56	68	mA

Notes: [1] The Typical Pattern contains a gray scale area, checkerboard area, and text.
[2] Black and white checkerboard pattern, each checker is one pixel wide.
[3] The value shown assumes the digital inputs to the SiI140/SiI140A are not toggling.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIP}	IDCK Period		11.6		50	ns
F_{CIP}	IDCK Frequency		20		86	MHz
T_{CIH}	IDCK High Time @ 86 MHz		3.7			ns
T_{CIL}	IDCK Low Time @ 86 MHz		3.3			ns
T_{IJIT}	Worst Case IDCK Clock Jitter[2,3]				2	ns
T_{SIDF}	Data/Control Setup Time to IDCK falling	CEDGE, DEDGE = 0	1			ns
T_{HIDF}	Data/Control Hold Time to IDCK falling	CEDGE, DEDGE = 0	2.6			ns
T_{SIDR}	Data/Control Setup Time to IDCK rising[1]	CEDGE, DEDGE = 1	2			ns
T_{HIDR}	Data/Control Hold Time to IDCK rising[1]	CEDGE, DEDGE = 1	3			ns
T_{DDF}	VSYNC, HSYNC, and CTL[3:1] Delay from DE falling edge		T_{CIP}			ns
T_{DDR}	VSYNC, HSYNC, and CTL[3:1] Delay from DE rising edge		T_{CIP}			ns
T_{LDE}	DE low time		$10T_{CIP}$			ns
S_{LHT}	Small Swing Low-to-High Transition Time	C_{LOAD} = 5pF R_{LOAD} = 50Ω R_{EXT_SWING} = 680Ω	0.25	0.3	0.5	ns
S_{HLT}	Small Swing High-to-Low Transition Time	C_{LOAD} = 5pF R_{LOAD} = 50Ω R_{EXT_SWING} = 680Ω	0.25	0.3	0.5	ns

Notes:
1. Guaranteed by design.
2. Jitter can be estimated by: 1) triggering a digital scope at the rising of input clock, and 2) measuring the peak to peak time spread of the rising edge of the input clock 1µs after the trigger.
3. Actual jitter tolerance may be higher depending on the frequency of the jitter.

Timing Diagrams

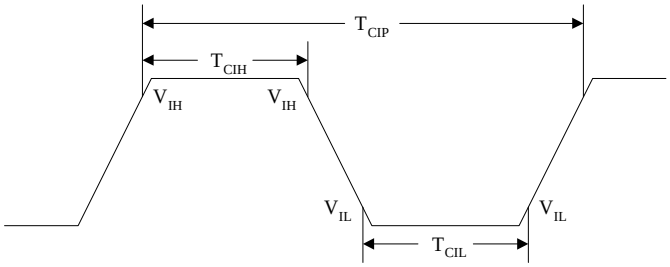


Figure 1. Clock Cycle/High/Low Times

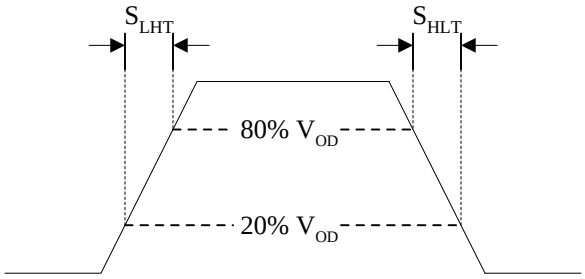


Figure 2. Small Swing Transition Times

Input Timing

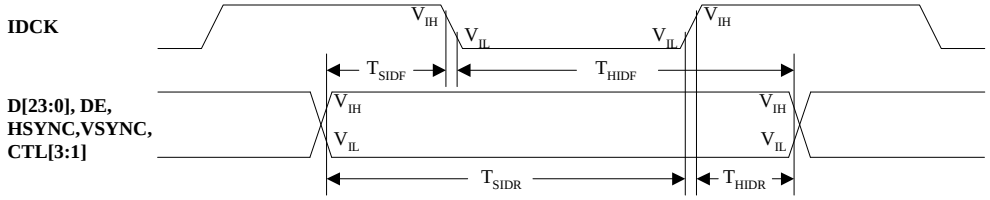


Figure 2. Input Data Setup/Hold Times to IDCK

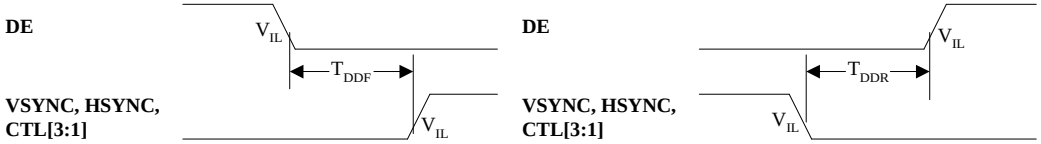


Figure 3. VSYNC, HSYNC, and CTL[3:1] Delay Times from DE

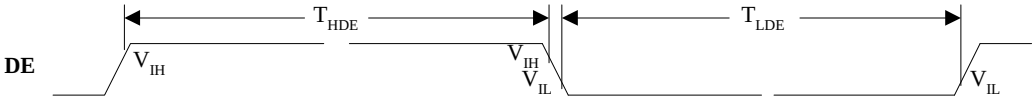


Figure 4. DE High/Low Times

Input Pin Description

Pin Name	Pin #	Type	Description
D23 – D0	See SiI140/ SiI140A Pin Diagram	In	Input Data is [23:0]. Input data is synchronized with input data clock (IDCK). Refer to the TFT Signal Mapping (SiI/AN-0007-A) and DSTN Signal Mapping (SiI/AN-0008-A) application notes which tabulate the relationship between the input data to the transmitter and output data from the receiver.
IDCK	12	In	Input Data Clock. Input data can be valid either on the falling or on the rising edge of IDCK as selected by DEDGE pin.
DE	1	In	Input Data Enable. This signal qualifies the active data period. DE is always required by the SiI140/SiI140A and must be high during active display time and low during blank time.
HSYNC	2	In	Horizontal Sync input control signal.
VSYNC	3	In	Vertical Sync input control signal.
CTL1	6	In	General input control signal 1.
CTL2	7	In	General input control signal 2
CTL3	8	In	General input control signal 3.

Configuration Pin Description

Pin Name	Pin #	Type	Description
DEDGE	9	In	Data Latching Edge. A low level indicates that input data (D[23:0]) will be latched on the falling edge of IDCK while a high level (3.3V) indicates that input data will be latched on the rising edge of IDCK.
CEDGE	11	In	Control Latching Edge. Controls latching edge of control signals DE, HSYNC, VSYNC, and CTL[3:1]. A low level indicates that input data enable and control signals will be latched on the falling edge of IDCK, while a high level (3.3V) indicates that input data enable and control signals will be latched on rising edge of IDCK.

Power Management Pin Description

Pin Name	Pin #	Type	Description
PD	35	In	Power Down (active low). A high level (3.3V) indicates normal operation and a low level indicates power down mode. During power down mode, all data and control inputs are disabled and most internal logic is powered down.

Differential Signal Data Pin Description

Pin Name	Pin #	Type	Description
TX0+	24	Analog	Low Voltage Differential Signal output data pairs.
TX0-	23	Analog	
TX1+	27	Analog	
TX1-	26	Analog	
TX2+	30	Analog	
TX2-	29	Analog	
TXC+	21	Analog	Low Voltage Differential Signal output clock pair.
TXC-	20	Analog	
EXT_ SWING	33	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. The amplitude of the voltage swing is determined by this resistance. For remote display applications, 400 Ω is recommended. For laptop computers, 680 Ω is recommended.

Reserved Pin Description

Pin Name	Pin #	Type	Description
RSVD	5	In	This pin must be tied high, low, or left unconnected. It also may be connected to pin 36 for backward compatibility with the SiI100.
RSVD	13	In	This pin must be tied high.
RSVD	14	In	This pin must be tied high.
RSVD	15	In	This pin must be left unconnected.
RSVD	34	In	This pin must be tied high, low, or left unconnected.

Power and Ground Pin Description

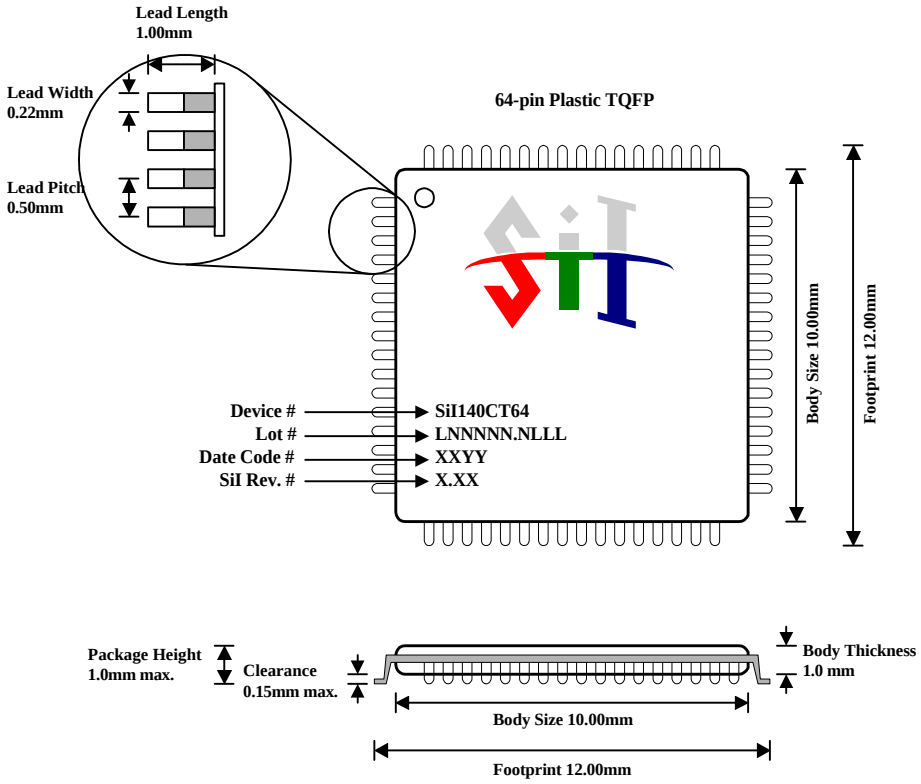
Pin Name	Pin #	Type	Description
VCC	10	Power	Core VCC, must be set to 3.3V.
	32		
	39		
IVCC	53	Power	Input VCC, must be set to 3.3V.
GND	4	Ground	Digital GND.
	16		
	45		
	64		
AVCC	22	Power	Analog VCC, must be set to 3.3V.
	28		
AGND	19	Ground	Analog GND.
	25		
	31		
PVCC	18	Power	PLL VCC, must be set to 3.3V.
PGND	17	Ground	PLL GND.

Application Information

To obtain the most updated Application Notes and other useful information for your design application, please visit the Silicon Image web site at ***www.siimage.com***, or contact your local Silicon Image sales office.

Package Dimensions

64-pin TQFP Package Dimensions



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