Document Title

64Kx16 SUper Low Power and Low Voltage Full CMOS SRAM Data Sheets for 48-CSP

Revision History

Rev. No.	History	Draft Data	Remark
Rev. 0.0	- 1′st edition - Package Dimension Finalized	Feb. 4′th, 1997	Preliminary
Rev. 0.1	- 2′nd edition - Change speed marking method Marking was indicate speed at high power, that change to speed at low power	Apr. 18′th, 1997	Preliminary

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64Kx16 bit Super Low Power and Low Voltage Full CMOS SRAM with 48-CSP(Chip Scale Package)

FEATURES SUMMARY

- Process Technology : 0.4μm Full CMOS
- Organization :64Kx16
- Power Supply Voltage
  KM616FS1000Z Family : 2.3V(Min) ~ 3.3V(Max)
  KM616FR1000Z Family : 1.8V(Min) ~ 2.7V(Max)
- Low Data Retention Voltage : 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type : 48-CSP with 0.75mm ball pitch

GENERAL DESCRIPTION

The KM616FS1000Z and KM616FR1000Z family are fabricated by SAMSUNG′s advanced Full CMOS process technology. The family support various operating temperature ranges and has very small size with 0.75 ball pitch and 6 x 8 ball array. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.Range	Vcc Range (min~max)	Speed(ns)	Power Dissipation		PKG Type
				Standby (I_{SB1})	Operating (I_{CC2})	
KM616FS1000Z	Commercial (0~70°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	5μA (Max)	80mA(Max) 50mA(Max)	48-CSP (6x8 ball area with 0.75mm ball pitch)
KM616FR1000Z		1.8~2.7V	300*@Vcc=2.0±0.2V		25mA(Max)	
KM616FS1000ZI	Industrial (-40~85°C)	2.3~3.3V	100*@Vcc=3.0±0.3V 150*@Vcc=2.5±0.2V	5μA (Max)	80mA(Max) 50mA(Max)	
KM616FR1000ZI		1.8~2.7V	300*@Vcc=2.0±0.2V		25mA(Max)	

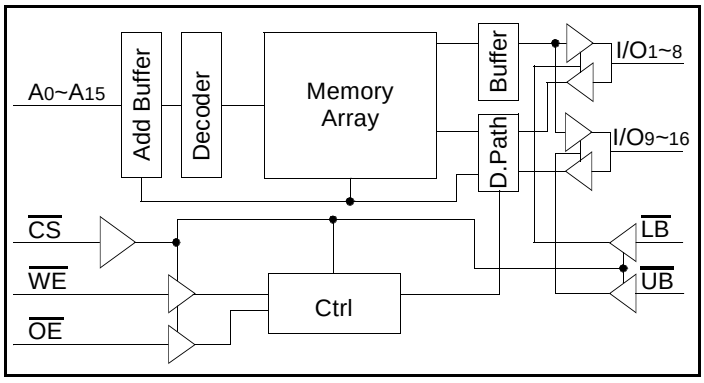
* The parameter is measured with 30pF test load.

48-CSP PIN TOP VIEW

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_9	$\overline{UB}$	A_3	A_4	$\overline{CS}$	I/O_1
C	I/O_{10}	I/O_{11}	A_5	A_6	I/O_2	I/O_3
D	V_{SS}	I/O_{12}	NC	A_7	I/O_4	V_{CC}
E	V_{CC}	I/O_{13}	NC	NC	I/O_5	V_{SS}
F	I/O_{15}	I/O_{14}	A_{14}	A_{15}	I/O_6	I/O_7
G	I/O_{16}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_8
H	NC	A_8	A_9	A_{10}	A_{11}	NC

* See last page for package dimension.

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
A_0~A_{15}	Address Inputs	$\overline{LB}$	Lower Byte($I/O_{1\sim8}$)
$\overline{WE}$	Write Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{OE}$	Output Enable Input	Vss	Ground
I/O_1~I/O_{16}	Data Inputs/Outputs	N.C.	No Connection

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PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70°C)		Industrial Temp Product (-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
KM616FS1000Z-15	48-CSP, 2.5V/3.0V, 150/100ns	KM616FS1000Z-15	48-CSP, 2.5V/3.0V, 150/100ns
KM616FR1000Z-30	48-CSP, 1.8V/2.5V, 300ns	KM616FR1000Z-30	48-CSP, 1.8V/2.5V, 300ns

* The meaning of 2.5V/3.0V, 150/100ns is that the operating V_{CC} is ranged from 2.3V(Min) to 3.3V(Max) with speed 150ns @2.5V±0.2 and 100ns @3.0V±0.3. This type of meaning is applied to other notations like the example.

** In case of KM616FR1000Z-30, there is only one speed bin, 300ns though it supports wide range operating V_{CC}.

ORDERING INFORMATION

KM6 16 X X 1000 X X X - X X

- Blank: : Low Low Power
- Access Time : 7=70ns, 8=85ns, 10=100ns, 12=120ns, 15=150ns, 30=300ns
- Operating Temperature : Blank=Commercial, E=Extended, I=Industrial
- Package Type : G=SOP, T=TSOP Forward R=TSOP Reverse Z=48-CSP with 0.75mm pitch
- Die Version : Blank=1′st generation
- Density : 1000=1Mbit
- S=2.3~3.3V, R=1.8~2.7V
- Process Technology : F-Full CMOS(6-Tr Cell)
- Organization : 16= x16
- SEC Standard SRAM

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.2 to 3.6V[1)]	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V[2)]	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-55 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	KM616FS1000Z KM616FR1000Z
		-40 to 85	°C	KM616FS1000ZI KM616FR1000ZI
Soldering temperature and time	T_{SOLDER}	260°C, 5sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional opera tion should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect r eliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product		Min	Typ**	Max	Unit
Supply voltage	Vcc	KM616FS1000Z Family		2.3	2.5/3.0	3.3	V
		KM616FR1000Z Family		1.8	2.0/2.5	2.7	V
Ground	Vss	All Family		0	0	0	V
Input high voltage	V_{IH}	KM616FS1000Z Family	Vcc=3.0±0.2V	2.2	-	Vcc+0.2	V
			Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
		KM616FR1000Z Family	Vcc=2.5±0.2V	2.0	-	Vcc+0.2	V
			Vcc=2.0±0.2V	1.6	-	Vcc+0.2	V
Input low voltage	V_{IL}	All Family		-0.2***	-	0.6	V

* 1) Commercial Product : T_A=0 to 70°C, unless otherwise specified
2) Industrial Product : T_A=-40 to 85°C, unless otherwise specified
** T_A=25°C
*** V_{IL}(Min)=-1.5V for≤30ns pulse width, not 100% tested

CAPACITANCE* (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

* Capacitance is sampled not, 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions[1]			Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc			-1	-	1	µA
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc			-1	-	1	µA
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL} V_{IN}=V_{IH} or V_{IL}, I_{IO}=0mA		Read	-	-	$10^{5)}$	mA
					Write	-	-	$20^{5)}$	
Average operating current		I_{CC1}	Cycle time=1µs100%duty $\overline{CS}$≤0.2V		Read	-	-	$10^{5)}$	mA
					Write	-	-	$20^{5)}$	
		I_{CC2}	Min cycle, 100% duty I_{IO}=0mA, $\overline{CS}$=V_{IH}	Vcc=3.3V@100ns		-	-	$80^{4)}$	mA
				Vcc=2.7V@150ns		-	-	50	
				Vcc=2.2V@300ns		-	-	25	
Output low voltage		V_{OL}	I_{OL}	Vcc=3.0V	2.1mA	-	-	0.4	V
				Vcc=2.5V	0.5mA	-	-	0.4	
				Vcc=2.0V	0.33mA	-	-	0.4	
Output high voltage		V_{OH}	I_{OH}	Vcc=3.0V	-1.0mA	2.4	-	-	V
				Vcc=2.5V	-0.5mA	2.0	-	-	
				Vcc=2.0V	-0.44mA	1.6	-	-	
Standby Current (TTL)		I_{SB}	$\overline{CS}$=V_{IH}			-	-	0.3	mA
Standby Current (CMOS)	KM616FS1000Z KM616FR1000Z	I_{SB1}	$\overline{CS}$≥Vcc-0.2V Other inputs =0~Vcc	Low Low Power		-	$0.05^{3)}$	$5^{2)}$	µA
	KM616FS1000ZI KM616FR1000ZI			Low Low Power		-	$0.05^{3)}$	$5^{2)}$	µA

1) - Commercial Product
T_A=0 to 70°C, Vcc=2.3(Min) ~ 3.3V(Max) for 616FS1000Z Family, Vcc=1.8V(Min) ~ 2.7V(Max)V for 616FR1000Z Family
- Industrial Product
T_A=-40 to 85°C, Vcc=2.3V(Min) ~ 3.3V(Max) for 616FS1000ZI Family, Vcc=1.8V(Min)~2.7V(Max) for 616FR1000ZI Family.

2) The value has difference by±µA, Measured at Vcc=3.3V(Max)

3) The value is not 100% tested but obtained statistically at Temp=25°C

4) - The value is measured at Vcc=3.0V±0.3V
- I_{CC2}=40mA with 120ns cycle at Vcc=2.5V±0.2V, but this value is not 100% tested but obtained statistically.
- I_{CC2}=25mA with 300ns cycle at Vcc=2.0V±0 .2V, but this value is not 100% tested but obtained statistically.

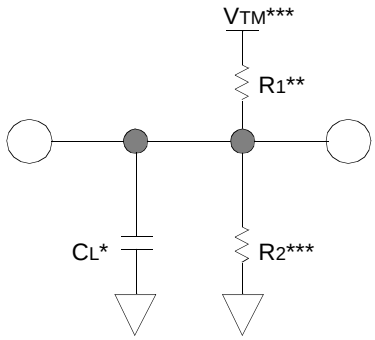
5) The value is measured at Vcc=3.0V±0.3V. The value measured at Vcc=2.5/2.0V is under the value of Vcc=3.0V

AC OPERATING CONDITIONS

TEST CONDITIONS(1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	V_{CC}=3.0V, 2.5V
	0.4 to 1.8V	V_{CC}=2.0V
Input rising and falling time	5ns	-
input and output reference voltage	1.5V	V_{CC}=3.0V
	1.1V	V_{CC}=2.5V
	0.9V	V_{CC}=2.0V,
Output load (See right)	C_L=100pF	See Test Condition #2
	C_L=30pF	

* See test condition of DC Operating characteristics



* Including scope and jig capacitance
**R_1=3070Ω, R_2=3150Ω
***V_{TM}=2.8V for Vcc = 3.0V
2.3V for Vcc = 2.5V
1.8V for Vcc = 2.0V

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Vcc Range	Typical Supply Vcc	Speed	Comments
KM616FR1000Z	0~70°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Commercial
KM616FS1000Z	0~70°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	
KM616FR1000ZI	-40~85°C	1.8(Min)~2.7(Max)	2.0V±0.2 Operation	300*ns	Industrial
KM616FS1000ZI	-40~85°C	2.3(Min)~3.3(Max)	2.5V±0.2 Operation	150*ns	
			3.0V±0.3 Operation	100*ns	

* The parameter is measured with 30pF test load

AC CHARACTERISTICS

Parameter List		Symbol	Speed Bins						Units
			100ns		150ns		300ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	100	-	150	-	300	-	ns
	Address access time	t_{AA}	-	100	-	150	-	300	ns
	Chip select to output	t_{CO1}	-	100	-	150	-	300	ns
	Output enable to valid output	t_{OE}	-	50	-	75	-	150	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	50	-	75	-	150	ns
	Chip select to low-Z output	t_{LZ1},t_{LZ2}	10	-	20	-	50	-	ns
	$\overline{OE}$ & $\overline{LB}$, $\overline{UB}$ to low-Z output	t_{OLZ},t_{BLZ}	5	-	20	-	30	-	ns
	Chip disable to high-Z output	t_{HZ1},t_{HZ2}	0	30	0	40	0	60	ns
	$\overline{OE}$ & $\overline{LB}$, $\overline{UB}$ disable to high-Z	t_{OHZ},t_{BHZ}	0	30	0	40	0	60	ns
	Output hold from address change	t_{OH}	15	-	15	-	30	-	ns
Write	Write cycle time	t_{WC}	100	-	150	-	300	-	ns
	Chip select to end of write	t_{CW}	80	-	120	-	300	-	ns
	Address set-up time	t_{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t_{AW}	80	-	120	-	300	-	ns
	Write pulse width	t_{WP}	70	-	100	-	200	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	80	-	120	-	300	-	ns
	Write recovery	t_{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	30	0	40	0	60	ns
	Data to write time overlap	t_{DW}	40	-	60	-	120	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	20	-	ns

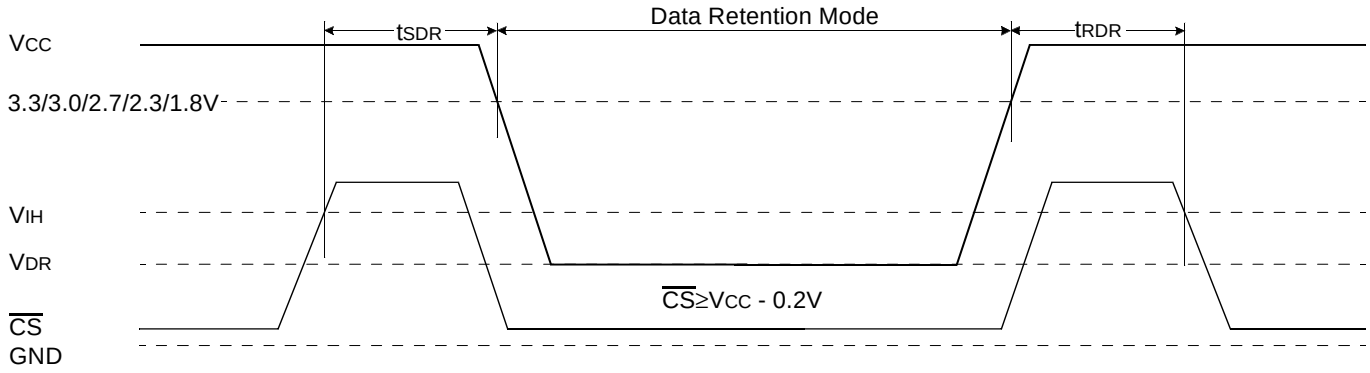
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V		1.5	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V $\overline{CS}$≥Vcc-0.2V	Low Low Power	-	-	5	µA
Data retention set-up time	t_{SDR}	See data retention waveform		0	-	-	ns
Recovery time	t_{RDR}			t_{RC}	-	-	

* 1) Commercial Product : T_A=0 to 70°C, unless otherwise specified
2) Industrial Product : T_A=-40 to 85°C, unless otherwise specified
** T_A=25°C, the value is too small to detect by test machine, 0.01µA statistically

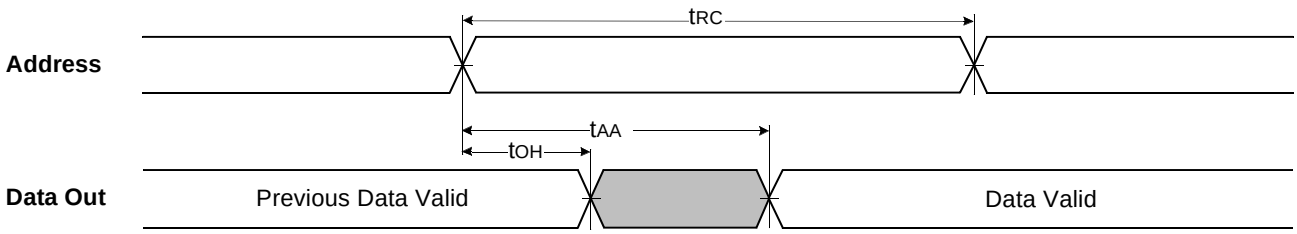
DATA RETENTION TIMING DIAGRAM

($\overline{CS}$ controlled)

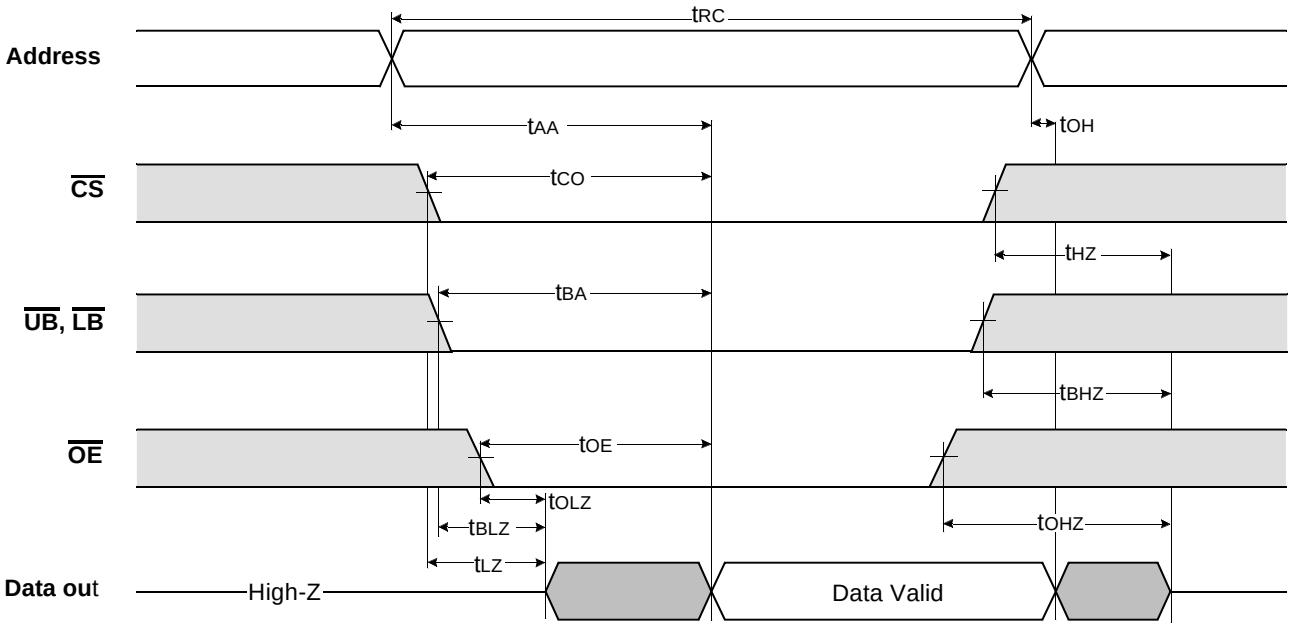


TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or, and $\overline{LB}$=V_{IL})



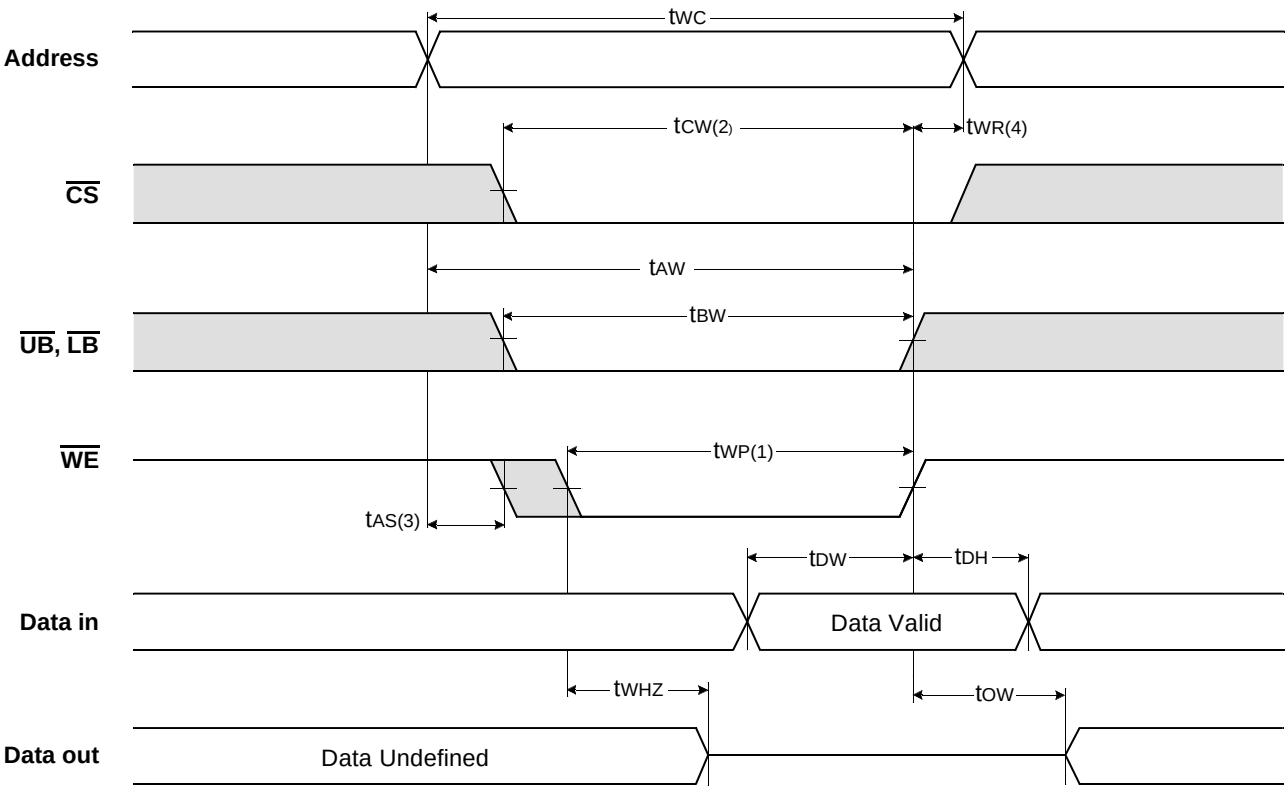
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



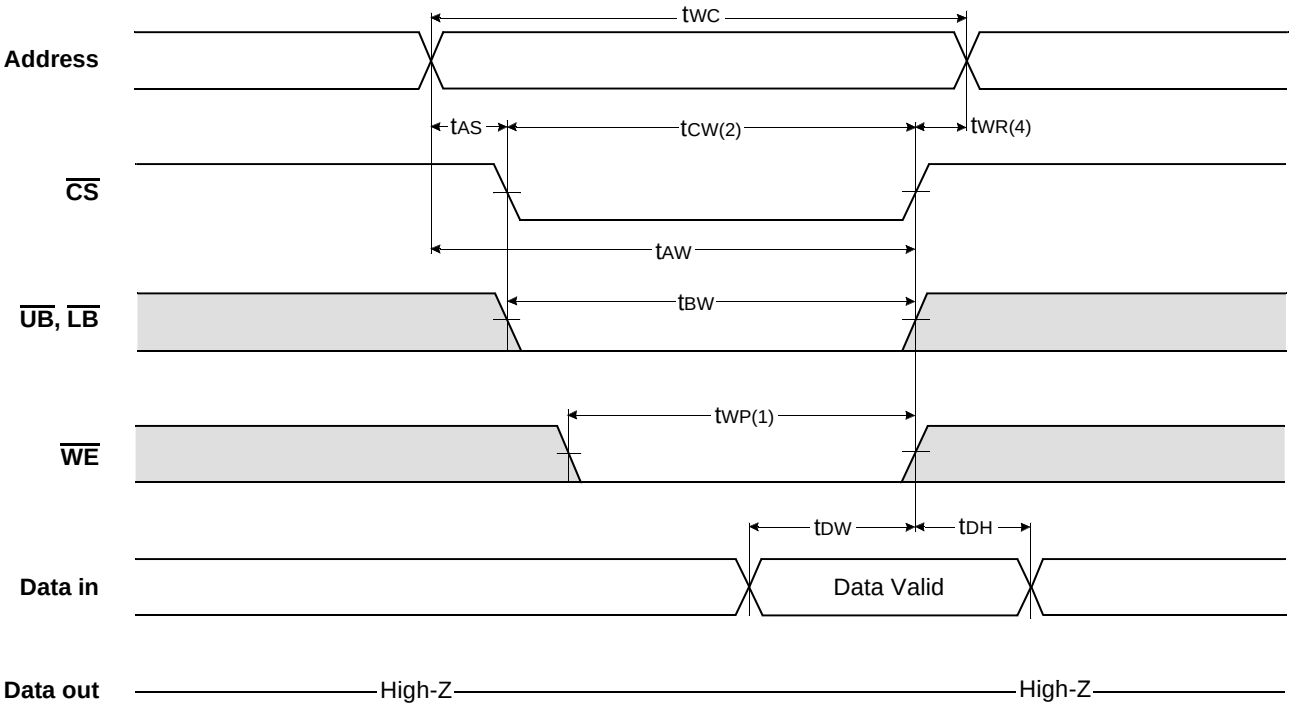
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device .

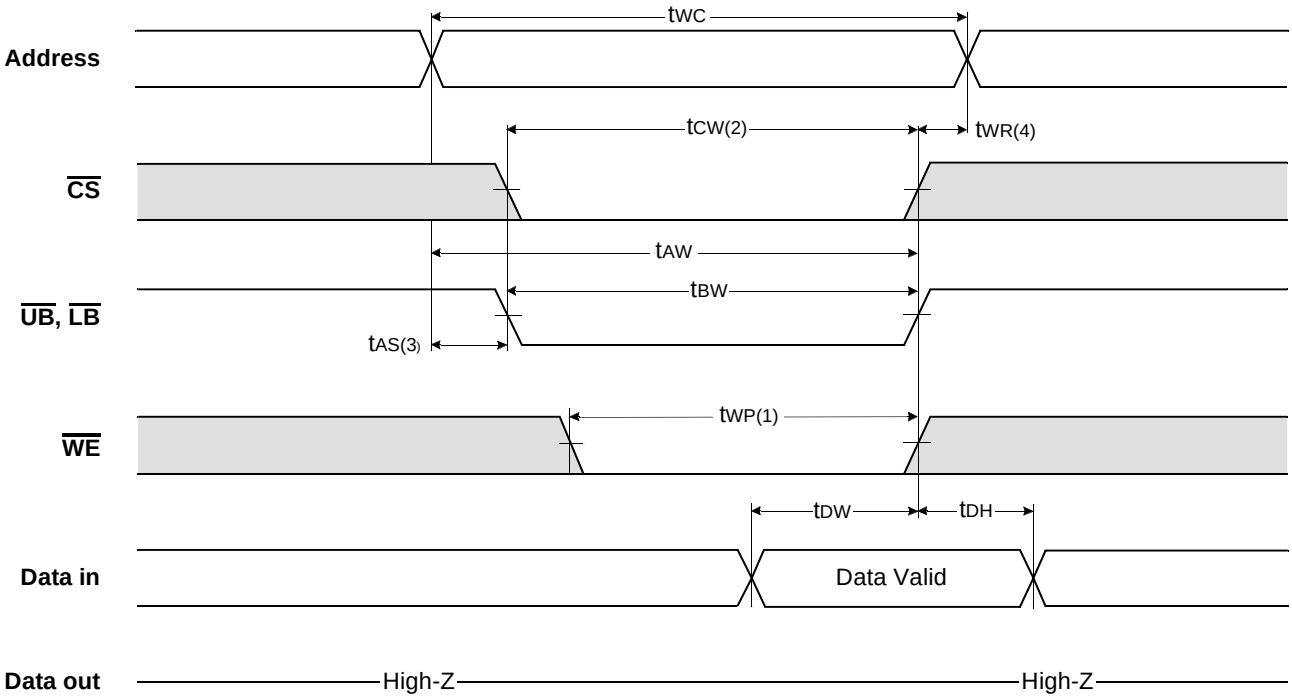
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultenious asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high.
   The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

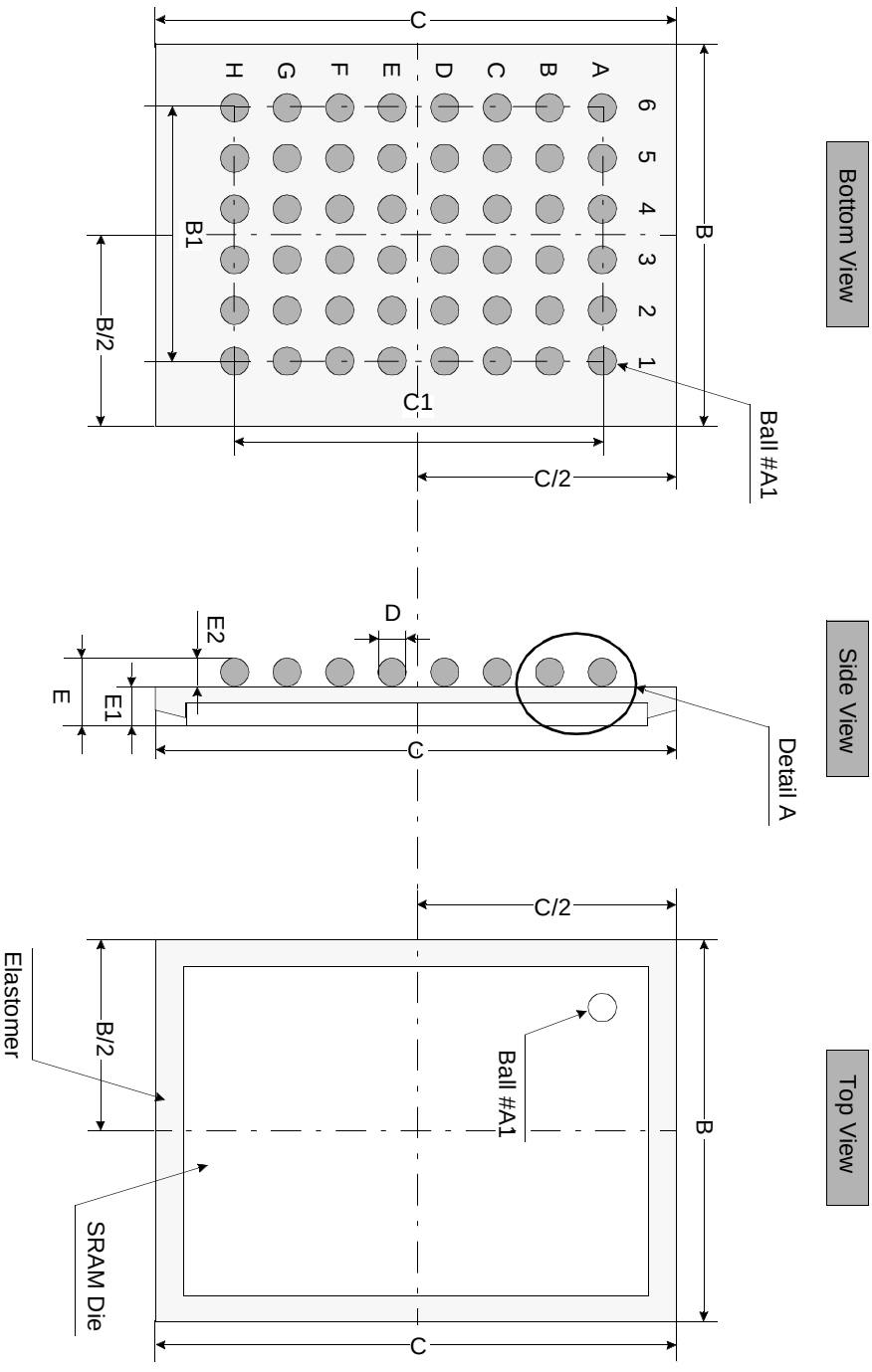
FUNCTIONAL DESCRIPTION

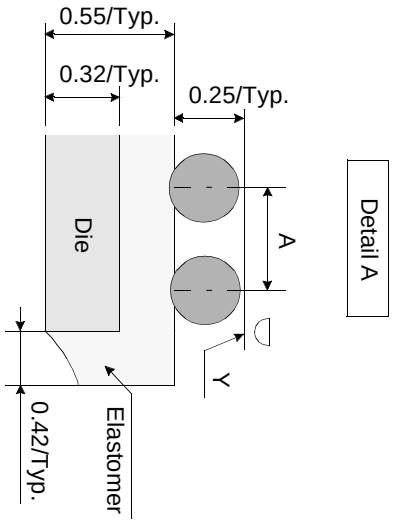
$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O1~8	I/O9~16	Current Mode
H	X	X	X	X	Not Select	High-Z	High-Z	I_{SB1}
L	X	X	H	H	Output Disable	High-Z	High-Z	Icc
L	H	H	X	X	Output Disable	High-Z	High-Z	
L	L	H	H	L	Read	Dout	High-Z	Icc
L	H	L	H	L	Read	High-Z	Dout	
L	L	L	H	L	Read	Dout	Dout	
L	L	H	L	X	Write	Din	High	Icc
L	H	L	L	X	Write	High-Z	Din	
L	L	L	L	X	Write	Din	Din	

* X means don't care (Must be in high or low states)

PACKAGE DIMENSIONS (Units : mm)

	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	0.80	0.81
E1	-	0.55	-
E2	-	0.25	-
Y	-	-	0.08





Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)