

**Document Title****32Kx8 bit Low Power CMOS Static RAM****Revision History**

<b><u>Revision No</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
0.0	Advance information	February 12th 1993	Design target
0.1	Initial draft	November 2nd 1993	Preliminary
1.0	Finalize	September 24th 1994	Final
2.0	Revise - Add 45ns part with 30pF test load	August 12th 1995	Final
3.0	Revise - Change specification format and merge : Commercial, Extended, Industrial product in same datasheets.	April 15th 1996	Final
4.0	Revise - Change Speed bin Erase 45ns part from commercial product and 100ns from extended and industrial product. - Production change Erase Low power product from TSOP package	December 19 1997	Final

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## 32Kx8 bit Low Power CMOS Static RAM

### FEATURES

- Process Technology : 0.7µm CMOS
- Organization : 32Kx8
- Power Supply Voltage : Single 5V±10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 28-DIP-600, 28-SOP-450,  
28-TSOP1 -0813.4F/R

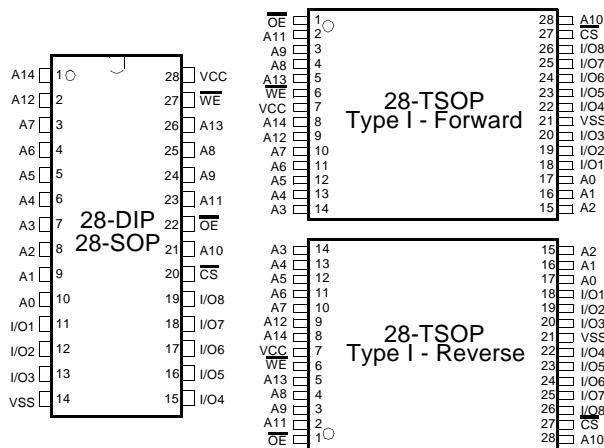
### GENERAL DESCRIPTION

The KM62256C family is fabricated by SAMSUNG's advanced CMOS process technology. The family supports various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

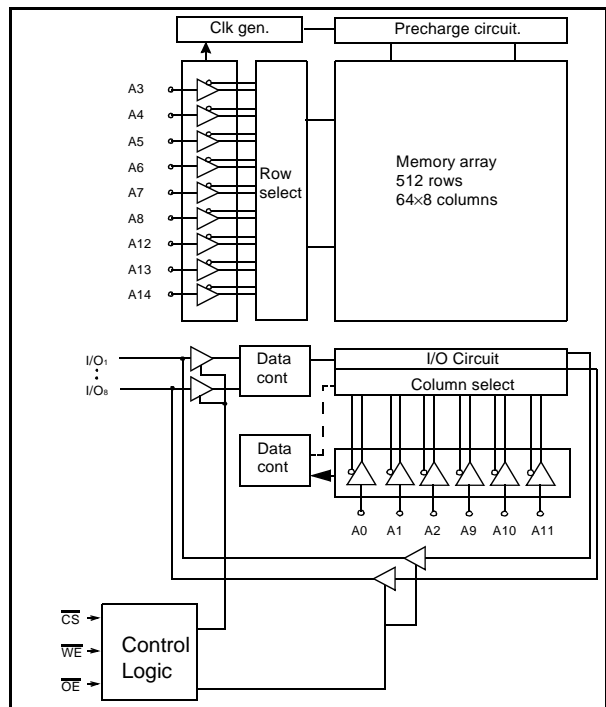
Product Family	Operating Temperature.	Speed(ns)	PKG Type	Power Dissipation	
				Standby (I <sub>SB1</sub> , Max)	Operating (I <sub>CC2</sub> )
KM62256CL	Commercial (0~70°C)	55/70ns	28-DIP, 28-SOP 28-TSOP I R/F	100µA	70mA
KM62256CL-L				20µA	
KM62256CLE	Extended (-25~85°C)	70ns	28-SOP 28-TSOP I R/F	100µA	
KM62256CLE-L				50µA	
KM62256CLI	Industrial (-40~85°C)	70ns	28-SOP 28-TSOP I R/F	100µA	
KM62256CLI-L				50µA	

### PIN DESCRIPTION



Name	Function
A <sub>0</sub> -A <sub>14</sub>	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O <sub>1</sub> -I/O <sub>8</sub>	Data Inputs/Outputs
V <sub>cc</sub>	Power(5V)
V <sub>ss</sub>	Ground

### FUNCTIONAL BLOCK DIAGRAM



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**PRODUCT LIST**

Commercial Temp Product (0~70°C)		Extended Temp Products (-25~85°C)		Industrial Temp Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM62256CLP-5	28-DIP, 55ns, L-pwr	KM62256CLGE-7	28-SOP, 70ns, L-pwr	KM62256CLGI-7	28-SOP, 70ns, L-pwr
KM62256CLP-5L	28-DIP, 55ns, LL-pwr	KM62256CLGE-7L	28-SOP, 70ns, LL-pwr	KM62256CLGI-7L	28-SOP, 70ns, LL-pwr
KM62256CLP-7	28-DIP, 70ns, L-pwr	KM62256CLTGE-7L	28-TSOP F, 70ns, LL-pwr	KM62256CLTGI-7L	28-TSOP F, 70ns, LL-pwr
KM62256CLP-7L	28-DIP, 70ns, LL-pwr	KM62256CLRGE-7L	28-TSOP R, 70ns, LL-pwr	KM62256CLRGI-7L	28-TSOP R, 70ns, LL-pwr
KM62256CLG-5	28-SOP, 55ns, L-pwr				
KM62256CLG-5L	28-SOP, 55ns, LL-pwr				
KM62256CLG-7	28-SOP, 70ns, L-pwr				
KM62256CLG-7L	28-SOP, 70ns, LL-pwr				
KM62256CLTG-5L	28-TSOP F, 55ns, LL-pwr				
KM62256CLTG-7L	28-TSOP F, 70ns, LL-pwr				
KM62256CLRG-5L	28-TSOP R, 55ns, LL-pwr				
KM62256CLRG-7L	28-TSOP R, 70ns, LL-pwr				

Note : LL means Low Low standby current.

**FUNCTIONAL DESCRIPTION**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Power
H	X	X	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X	L	Din	Write	Active

1. X means don't care

**ABSOLUTE MAXIMUM RATINGS <sup>1)</sup>**

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> ,V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	KM62256CL
		-25 to 85	°C	KM62256CLE
		-40 to 85	°C	KM62256CLI
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec(Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS <sup>1)</sup>

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5V <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.5 <sup>3)</sup>	-	0.8	V

### Note

- Commercial Product : T<sub>A</sub>=0 to 70°C, unless otherwise specified  
 Extended Product : T<sub>A</sub>=-25 to 85°C, unless otherwise specified  
 Industrial Product : T<sub>A</sub>=-40 to 85°C, unless otherwise specified
- Overshoot : V<sub>CC</sub>+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot is sampled, not 100% tested

## CAPACITANCE <sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

- Capacitance is sampled, not 100% tested

## DC AND OPERATING CHARACTERISTICS

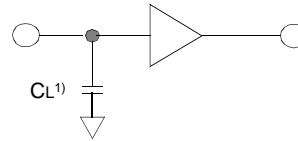
Item	Symbol	Test Conditions	Min	Typ	Max	Unit			
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA			
Output leakage current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA			
Operating power supply current	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	7	15 <sup>1)</sup>	mA			
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA $\overline{CS} \leq 0.2V$ , V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	-	-	7 <sup>2)</sup>	mA			
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	-	-	70	mA			
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V			
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.4	-	-	V			
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}=V_{IH}$ , Other inputs=V <sub>IH</sub> or V <sub>IL</sub>	-	-	1 <sup>3)</sup>	mA			
Standby Current (CMOS)	KM62256CL KM62256CL-L	$\overline{CS} \geq V_{CC}-0.2V$ , Other inputs=0~V <sub>CC</sub>			L(Low Power)	-	2	100	μA
	LL(L Low Power)				-	1	20		
	KM62256CLE KM62256CLE-L				L(Low Power)	-	-	100	μA
	LL(L Low Power)				-	-	50		
KM62256CLI KM62256CLI-L	L(Low Power)	-	-	100	μA				
	LL(L Low Power)	-	-	50					

- 20mA for Extended and Industrial Products
- 10mA for Extended and Industrial Products
- 2mA for Extended and Industrial Products

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V  
 Input rising and falling time : 5ns  
 Input and output reference voltage : 1.5V  
 Output load (See right) :  $C_L = 100\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS ( $V_{CC} = 4.5 \sim 5.5\text{V}$ , KM62256C Family : $T_A = 0$ to $70^\circ\text{C}$ , KM62256CE Family : $T_A = -25$ to $85^\circ\text{C}$ , KM62256CI Family : $T_A = -40$ to $85^\circ\text{C}$ )

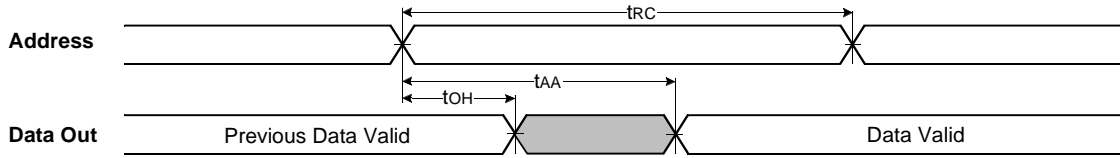
Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	55	-	70	-	ns
	Address access time	t <sub>AA</sub>	-	55	-	70	ns
	Chip select to output	t <sub>CO</sub>	-	55	-	70	ns
	Output enable to valid output	t <sub>OE</sub>	-	25	-	35	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	20	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	20	0	30	ns
	Output hold from address change	t <sub>OH</sub>	5	-	5	-	ns
Write	Write cycle time	t <sub>WC</sub>	55	-	70	-	ns
	Chip select to end of write	t <sub>CW</sub>	45	-	60	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	45	-	60	-	ns
	Write pulse width	t <sub>WP</sub>	40	-	50	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	20	0	25	ns
	Data to write time overlap	t <sub>DW</sub>	25	-	30	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	ns
		End write to output low-Z	t <sub>OW</sub>	5	-	5	-

## DATA RETENTION CHARACTERISTICS

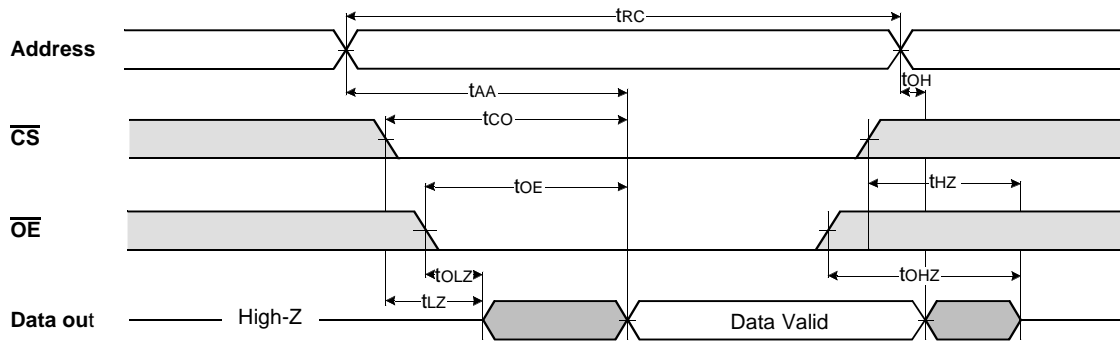
Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	2.0	-	5.5	V	
Data retention current	I <sub>DR</sub>	$V_{CC} = 3.0\text{V}$ $\overline{CS} \geq V_{CC} - 0.2\text{V}$	L-Ver	-	1	50	$\mu\text{A}$
			LL-Ver	-	0.5	10	
			L-Ver	-	-	50	
			LL-Ver	-	-	25	
			L-Ver	-	-	50	
			LL-Ver	-	-	25	
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms	
Recovery time	t <sub>RDR</sub>		5	-	-		

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



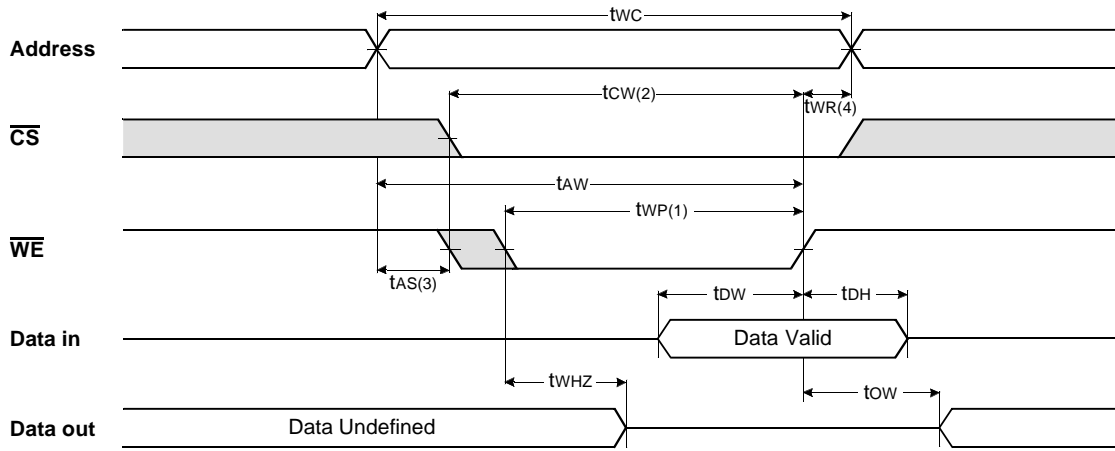
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



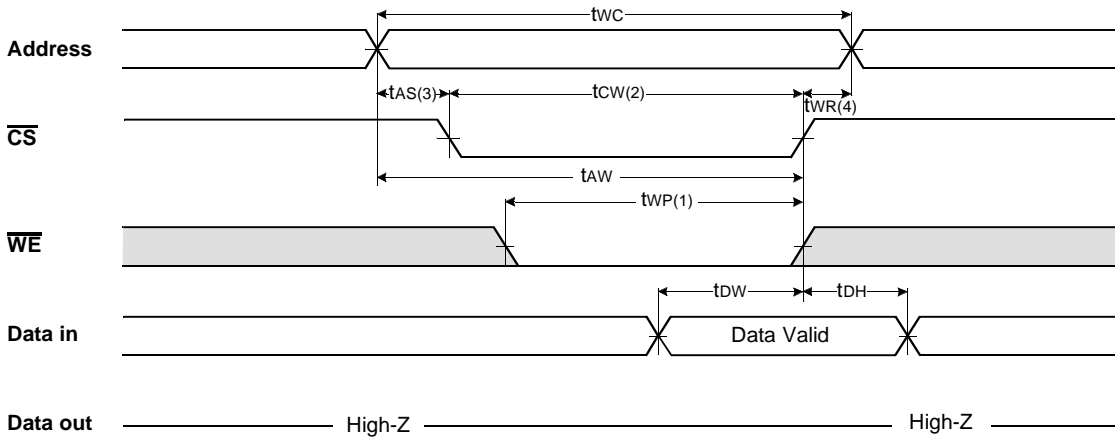
NOTES (READ CYCLE)

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS}$  Controlled)

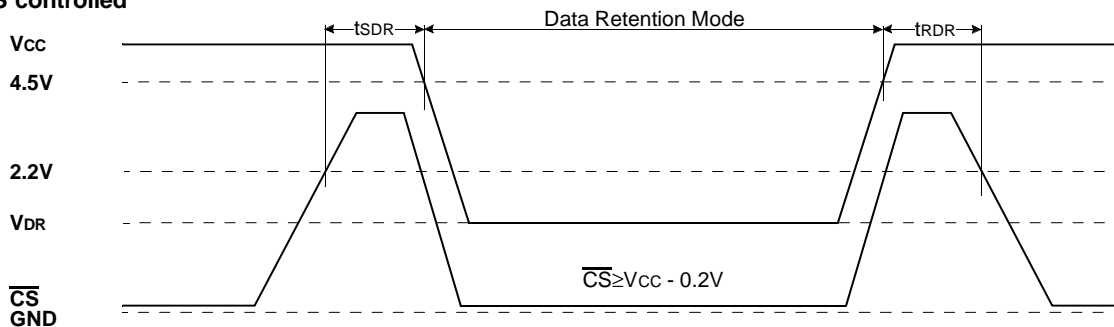


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}$  going Low and  $\overline{WE}$  going low : A write end at the earliest transition among  $\overline{CS}$  going high and  $\overline{WE}$  going high,  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.

DATA RETENTION WAVE FORM

$\overline{CS}$  controlled



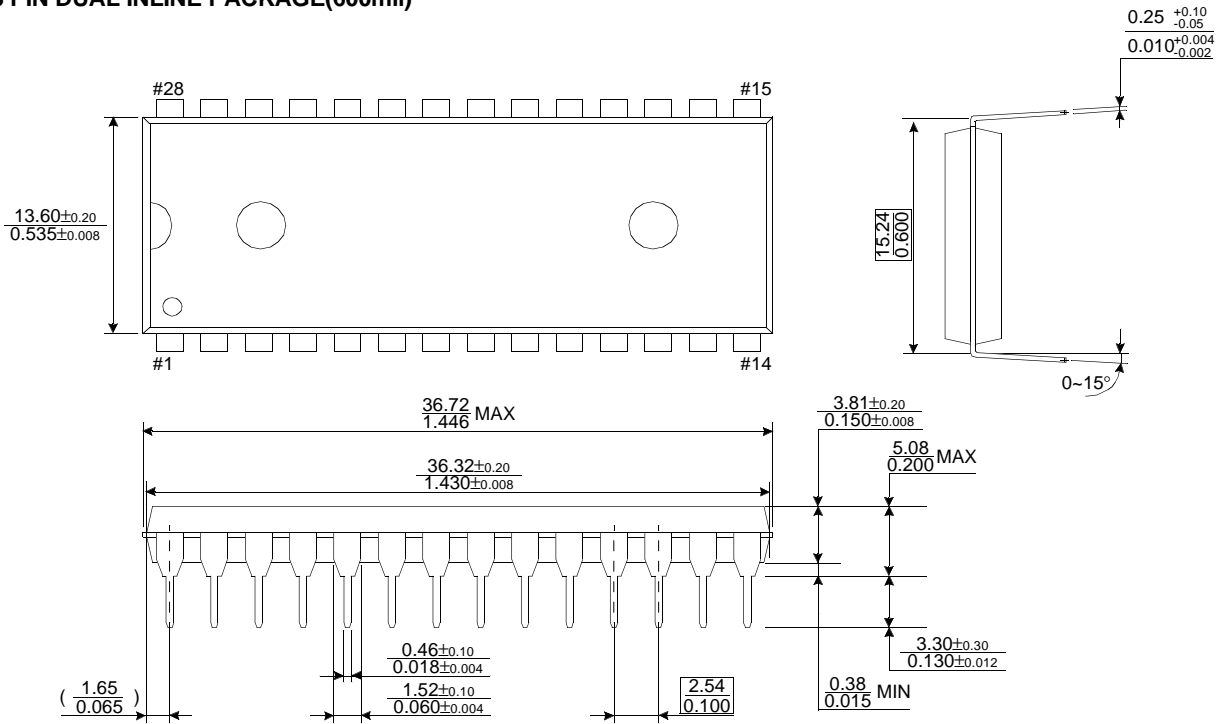
# KM62256C Family

# CMOS SRAM

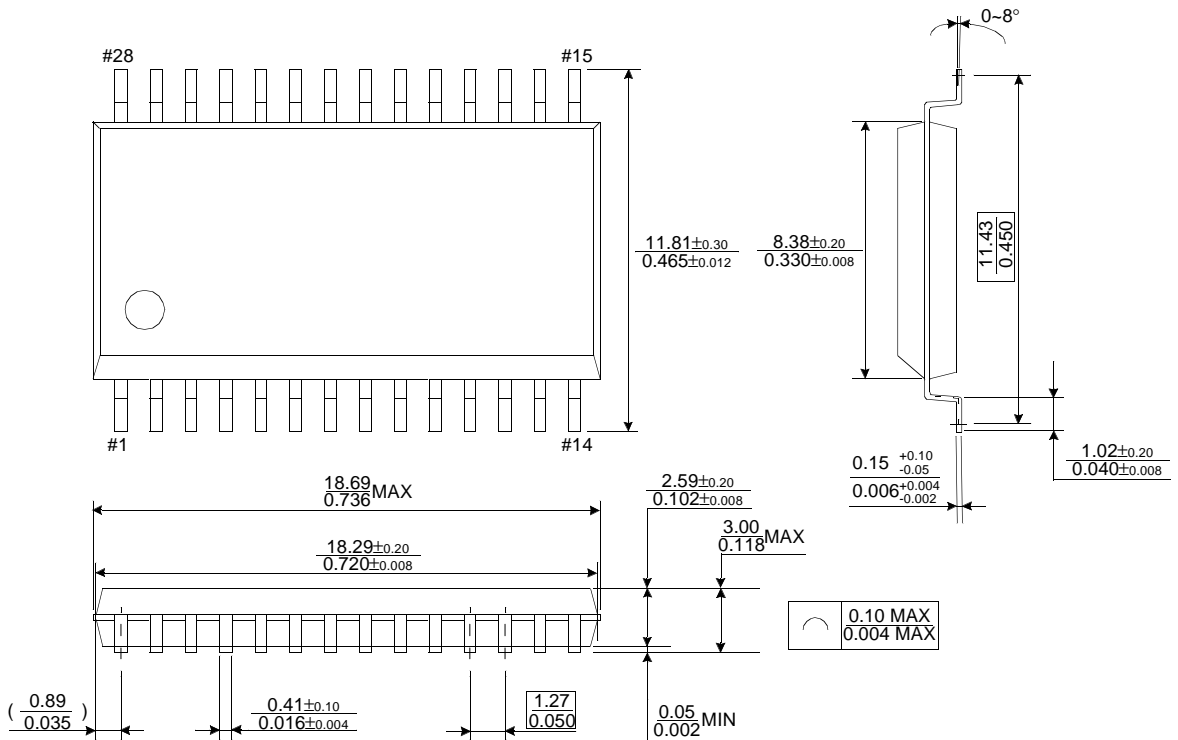
## PACKAGE DIMENSIONS

Units : millimeters(inches)

### 28 PIN DUAL INLINE PACKAGE(600mil)



### 28 PIN PLASTIC SMALL OUTLINE PACKAGE(450mil)

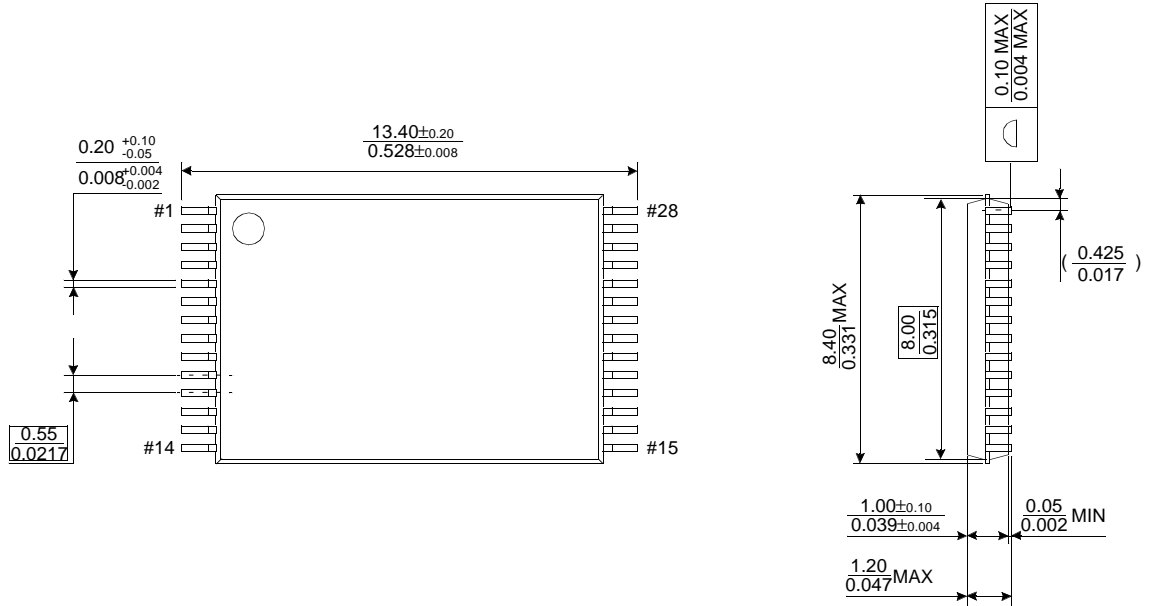




**PACKAGE DIMENSIONS**

Units : millimeters(inches )

**28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)**



**28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)**

