

Document Title

256Kx4 Bit (with OE) High-Speed CMOS Static RAM(5.0V Operating).

Revision History

| <u>Rev.No.</u> | <u>History</u> | <u>Draft Data</u> | <u>Remark</u> | | | | | | | | |
|-----------------------|--|--------------------------|----------------------|---------|-----------------|------|------|------|------|--|--|
| Rev. 0.0 | Initial release with Preliminary. | June. 8. 2001 | Preliminary | | | | | | | | |
| Rev. 0.1 | Current modify | September. 9. 2001 | Preliminary | | | | | | | | |
| Rev. 0.2 | 1. Delete 15ns speed bin. 2. Change Icc for Industrial mode. | December. 18. 2001 | Preliminary | | | | | | | | |
| | <table border="1"> <thead> <tr> <th>Item</th> <th>Previous</th> <th>Current</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Icc(Industrial)</td> <td>10ns</td> <td>85mA</td> </tr> <tr> <td>12ns</td> <td>75mA</td> </tr> </tbody> </table> | Item | Previous | Current | Icc(Industrial) | 10ns | 85mA | 12ns | 75mA | | |
| Item | Previous | Current | | | | | | | | | |
| Icc(Industrial) | 10ns | 85mA | | | | | | | | | |
| | 12ns | 75mA | | | | | | | | | |
| Rev. 1.0 | 1. Final <u>datasheet</u> release. 2. Delete UB, LB related AC characteristics and timing diagram. | June. 19. 2002 | Final | | | | | | | | |
| Rev. 2.0 | 1. Delete 12ns speed bin. | July. 8. 2002 | Final | | | | | | | | |
| Rev. 3.0 | 1. Add the Lead Free Package type. | July. 26, 2004 | Final | | | | | | | | |

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

K6R1004C1D

CMOS SRAM

1Mb Async. Fast SRAM Ordering Information

| Org. | Part Number | VDD(V) | Speed (ns) | PKG | Temp. & Power |
|---------|---------------------------------|--------|--------------|---|--|
| 256K x4 | K6R1004C1D-J(K)C(I) 10 | 5 | 10 | J : 32-SOJ | C : Commercial Temperature ,Normal Power Range I : Industrial Temperature ,Normal Power Range |
| | K6R1004V1D-J(K)C(I) 08/10 | 3.3 | 8/10 | K : 32-SOJ(LF) | |
| 128K x8 | K6R1008C1D-J(K,T,U)C(I) 10 | 5 | 10 | J : 32-SOJ | |
| | K6R1008V1D-J(K,T,U)C(I) 08/10 | 3.3 | 8/10 | K : 32-SOJ(LF) T : 32-TSOP2 U : 32-TSOP2(LF) | |
| 64K x16 | K6R1016C1D-J(K,T,U,E)C(I) 10 | 5 | 10 | J : 44-SOJ | |
| | K6R1016V1D-J(K,T,U,E)C(I) 08/10 | 3.3 | 8/10 | K : 44-SOJ(LF) T : 44-TSOP2 U : 44-TSOP2(LF) E : 48-TBGA | |

256K x 4 Bit (with OE) High-Speed CMOS Static RAM

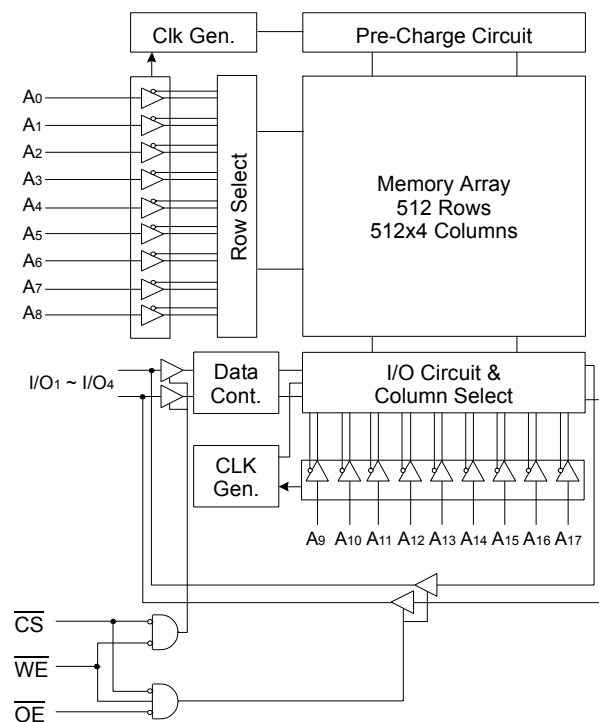
FEATURES

- Fast Access Time 10ns(Max.)
- Power Dissipation
 - Standby (TTL) : 20mA(Max.)
 - (CMOS) : 5mA(Max.)
 - Operating K6R1004C1D-10: 65mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration :
 - K6R1004C1C-J : 32-SOJ-400
 - K6R1004C1C-K : 32-SOJ-400(Lead-Free)
- Operating in Commercial and Industrial Temperature range.

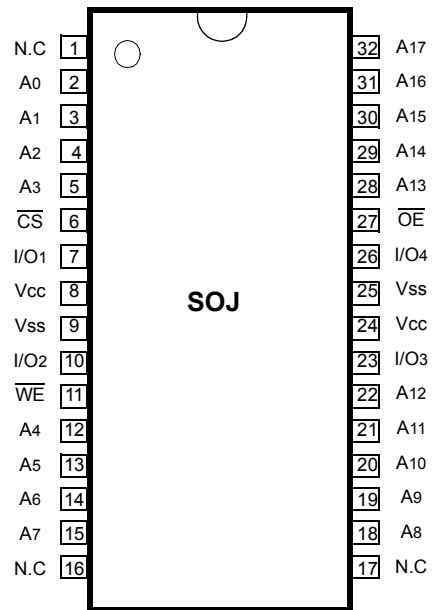
GENERAL DESCRIPTION

The K6R1004C1D is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The K6R1004C1D uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAM-SUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R1004C1D is packaged in a 400 mil 32-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



PIN FUNCTION

| Pin Name | Pin Function |
|-----------------|---------------------|
| A0 - A17 | Address Inputs |
| \overline{WE} | Write Enable |
| \overline{CS} | Chip Select |
| \overline{OE} | Output Enable |
| I/O1 ~ I/O4 | Data Inputs/Outputs |
| Vcc | Power(+5.0V) |
| Vss | Ground |
| N.C | No Connection |

ABSOLUTE MAXIMUM RATINGS*

| Parameter | Symbol | Rating | Unit | |
|---|------------------------------------|-------------------------------|-----------|----|
| Voltage on Any Pin Relative to V _{SS} | V _{IN} , V _{OUT} | -0.5 to V _{CC} +0.5V | V | |
| Voltage on V _{CC} Supply Relative to V _{SS} | V _{CC} | -0.5 to 7.0 | V | |
| Power Dissipation | P _d | 1 | W | |
| Storage Temperature | T _{STG} | -65 to 150 | °C | |
| Operating Temperature | Commercial | T _A | 0 to 70 | °C |
| | Industrial | T _A | -40 to 85 | °C |

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|-------|-----|------------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.2 | - | V _{CC} +0.5** | V |
| Input Low Voltage | V _{IL} | -0.5* | - | 0.8 | V |

* V_{IL}(Min) = -2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Max | Unit | | |
|---------------------------|------------------|--|------|------|------|----|----|
| Input Leakage Current | I _{LI} | V _{IN} =V _{SS} to V _{CC} | -2 | 2 | μA | | |
| Output Leakage Current | I _{LO} | $\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =V _{SS} to V _{CC} | -2 | 2 | μA | | |
| Operating Current | I _{CC} | Min. Cycle, 100% Duty | Com. | 10ns | - | 65 | mA |
| | | | Ind. | 10ns | - | 75 | |
| Standby Current | I _{SB} | Min. Cycle, $\overline{CS}=V_{IH}$ | - | 20 | mA | | |
| | I _{SB1} | f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V | - | 5 | | | |
| Output Low Voltage Level | V _{OL} | I _{OL} =8mA | - | 0.4 | V | | |
| Output High Voltage Level | V _{OH} | I _{OH} =-4mA | 2.4 | - | V | | |

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

| Item | Symbol | Test Conditions | TYP | Max | Unit |
|--------------------------|------------------|----------------------|-----|-----|------|
| Input/Output Capacitance | C _{I/O} | V _{I/O} =0V | - | 8 | pF |
| Input Capacitance | C _{IN} | V _{IN} =0V | - | 6 | pF |

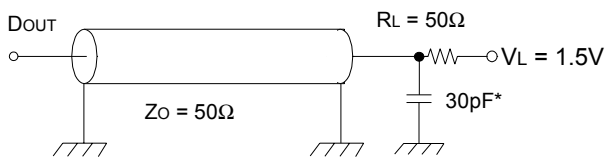
* Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS (TA=0 to 70°C, VCC=5.0V±10%, unless otherwise noted.)

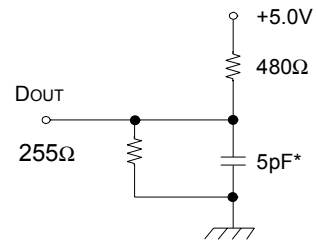
TEST CONDITIONS

| Parameter | Value |
|--|-----------|
| Input Pulse Levels | 0V to 3V |
| Input Rise and Fall Times | 3ns |
| Input and Output timing Reference Levels | 1.5V |
| Output Loads | See below |

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

| Parameter | Symbol | K6R1004C1D-10 | | Unit |
|-----------------------------------|--------|---------------|-----|------|
| | | Min | Max | |
| Read Cycle Time | tRC | 10 | - | ns |
| Address Access Time | tAA | - | 10 | ns |
| Chip Select to Output | tCO | - | 10 | ns |
| Output Enable to Valid Output | tOE | - | 5 | ns |
| Chip Enable to Low-Z Output | tLZ | 3 | - | ns |
| Output Enable to Low-Z Output | tOLZ | 0 | - | ns |
| Chip Disable to High-Z Output | tHZ | 0 | 5 | ns |
| Output Disable to High-Z Output | tOHZ | 0 | 5 | ns |
| Output Hold from Address Change | tOH | 3 | - | ns |
| Chip Selection to Power Up Time | tPU | 0 | - | ns |
| Chip Selection to Power Down Time | tPD | - | 10 | ns |

* The above parameters are also guaranteed at industrial temperature range.

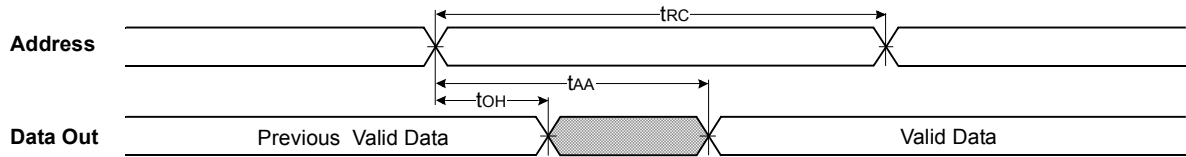
WRITE CYCLE*

| Parameter | Symbol | K6R1004C1D-10 | | Unit |
|--|------------------|---------------|-----|------|
| | | Min | Max | |
| Write Cycle Time | t _{WC} | 10 | - | ns |
| Chip Select to End of Write | t _{CW} | 7 | - | ns |
| Address Set-up Time | t _{AS} | 0 | - | ns |
| Address Valid to End of Write | t _{AW} | 7 | - | ns |
| Write Pulse Width(\overline{OE} High) | t _{WP} | 7 | - | ns |
| Write Pulse Width(\overline{OE} Low) | t _{WP1} | 10 | - | ns |
| Write Recovery Time | t _{WR} | 0 | - | ns |
| Write to Output High-Z | t _{WHZ} | 0 | 5 | ns |
| Data to Write Time Overlap | t _{DW} | 5 | - | ns |
| Data Hold from Write Time | t _{DH} | 0 | - | ns |
| End of Write to Output Low-Z | t _{OW} | 3 | - | ns |

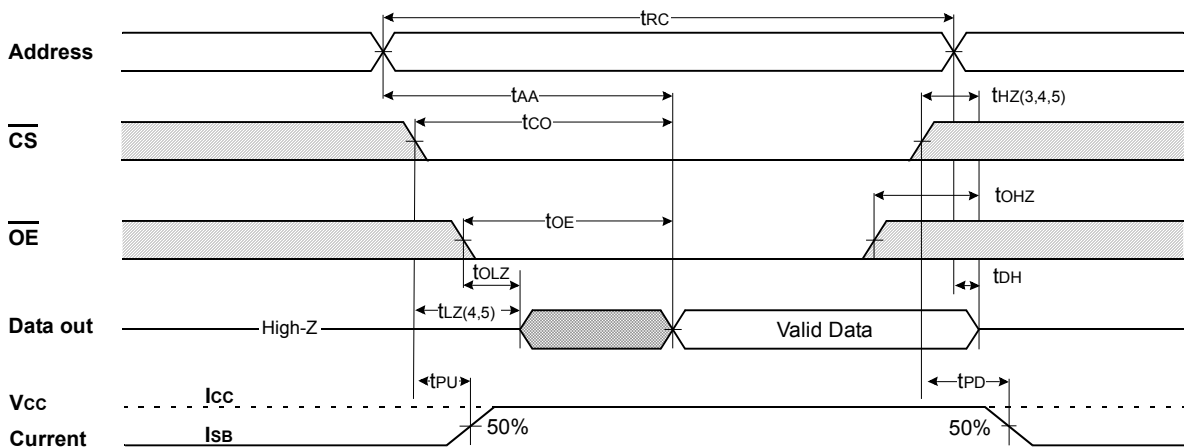
* The above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



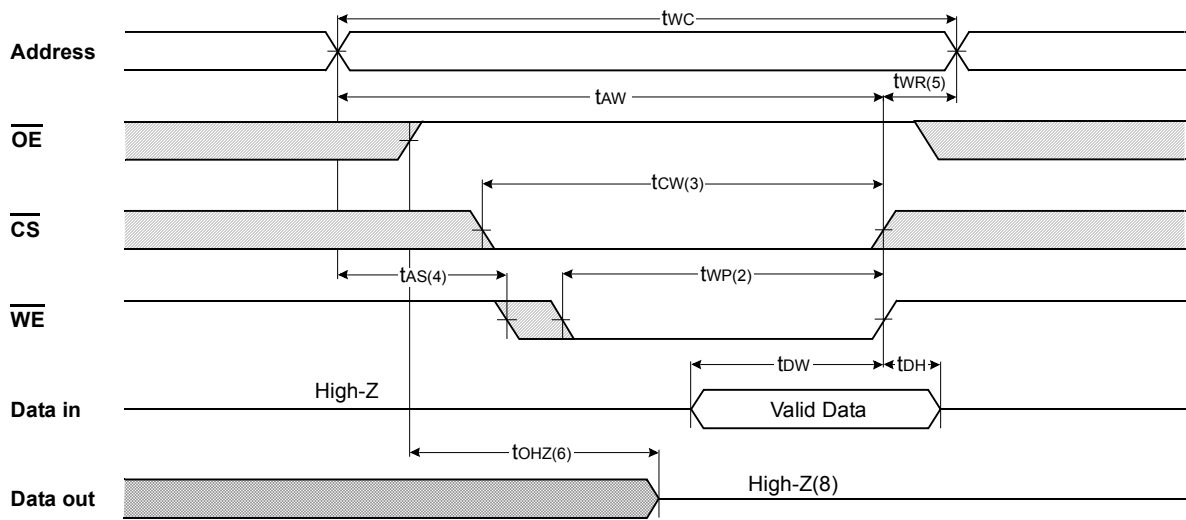
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



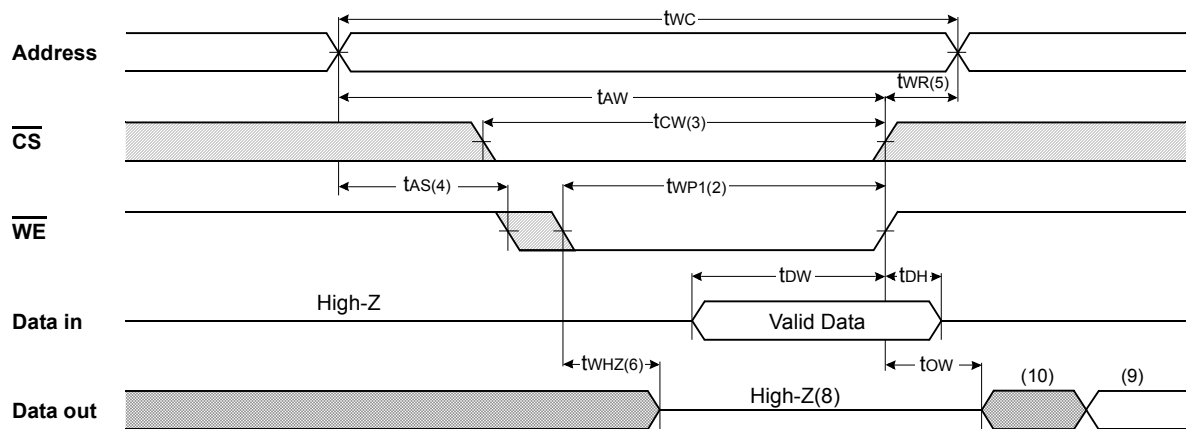
NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{Lz}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

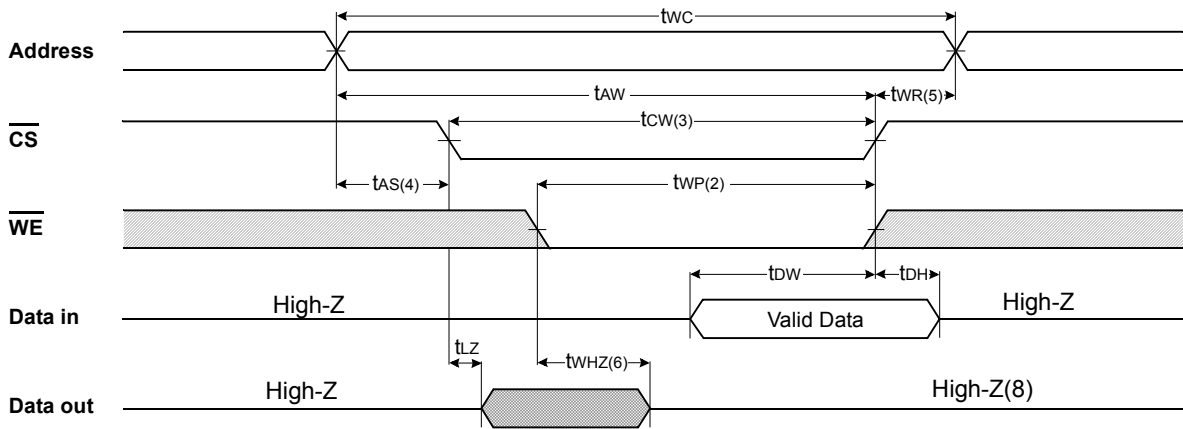
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{OE} = Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} =Low Fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{CS} =Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CS} and \overline{WE} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of \overline{CS} going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

| \overline{CS} | \overline{WE} | \overline{OE} | Mode | I/O Pin | Supply Current |
|-----------------|-----------------|-----------------|----------------|---------|----------------|
| H | X | X* | Not Select | High-Z | ISB, ISB1 |
| L | H | H | Output Disable | High-Z | ICC |
| L | H | L | Read | DOUT | ICC |
| L | L | X | Write | DIN | ICC |

* X means Don't Care.

PACKAGE DIMENSIONS

Units: millimeters/Inches

32-SOJ-400

