

Document Title

256Kx4 Bit (with OE) High Speed Static RAM(3.3V Operating), Revolutionary Pin out.

Revision History

<u>RevNo.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
Rev. 0.0	Initial release with Design Target.	Apr. 1st, 1997	Design Target
Rev.1.0	Release to Preliminary Data Sheet. 1.1. Replace Design Target to Preliminary.	Jun. 1st, 1997	Preliminary
Rev.2.0	Release to Final Data Sheet. 2.1. Delete Preliminary. 2.2. Delete L-version. 2.3. Delete Data Retention Characteristics and Waveform. 2.4. Delete Industrial Temperature Range Part. 2.5. Delete TSOP2 Package. 2.6. Add Capacitive load of the test environment in A.C test load. 2.7. Change D.C characteristics.	Feb. 25th, 1998	Final
	Items	Previous spec. (8/10/12ns part)	Changed spec. (8/10/12ns part)
	Icc	150/140/130mA	150/145/140mA
	Isb	30mA	50mA

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

**256K x 4 Bit (with OE) High-Speed CMOS Static RAM (3.3V Operating)**

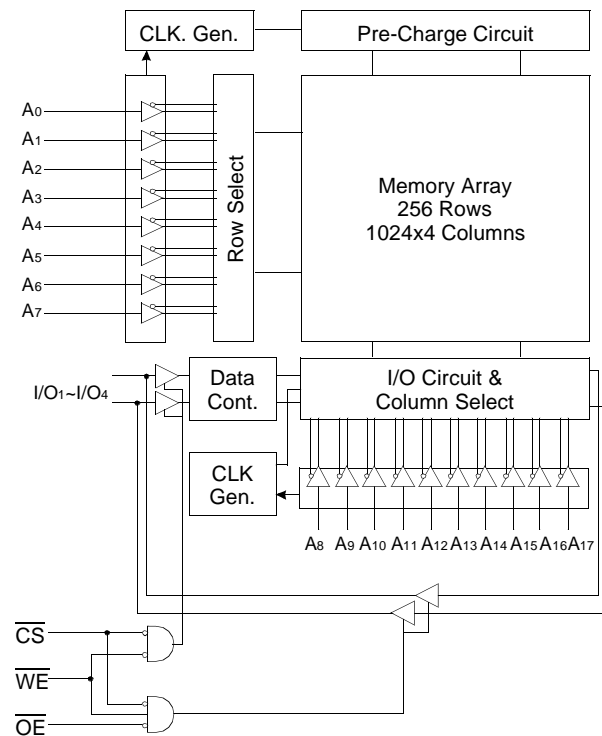
**FEATURES**

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 5mA(Max.)
  - Operating K6R1004V1B-8 : 150mA(Max.)
  - K6R1004V1B-10 : 145mA(Max.)
  - K6R1004V1B-12 : 140mA(Max.)
- Single 3.3±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - K6R1004V1B-J : 32-SOJ-400

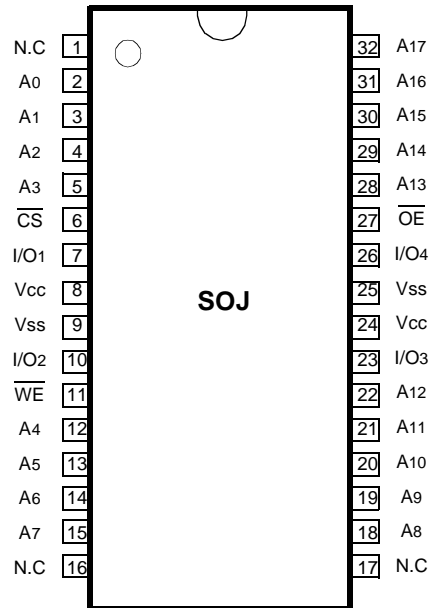
**GENERAL DESCRIPTION**

The K6R1004V1B is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The K6R1004V1B uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R1004V1B is packaged in a 400 mil 32-pin plastic SOJ.

**FUNCTIONAL BLOCK DIAGRAM**



**PIN CONFIGURATION (Top View)**



**PIN FUNCTION**

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

## ABSOLUTE MAXIMUM RATINGS\*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 4.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	0 to 70	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress ating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> + 0.3**	V
Input Low Voltage	V <sub>IL</sub>	-0.3*	-	0.8	V

\* V<sub>IL</sub>(Min)=-2.0V a.c(Pulse Width ≤ 6ns) for I ≤ 20mA.

\*\* V<sub>IH</sub>(Max)=V<sub>CC</sub> + 2.0V a.c (Pulse Width ≤ 6ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS(T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-2	2	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-2	2	μA	
Operating Current	I <sub>CC</sub>	Min. Cycle, 100% Duty $\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	8ns	-	150	mA
			10ns	-	145	
			12ns	-	140	
Standby Current	I <sub>SB</sub>	Min. Cycle, $\overline{CS}=V_{IH}$	-	50	mA	
	I <sub>SB1</sub>	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$ , V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	-	5		
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> =8mA	-	0.4	V	
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> =-4mA	2.4	-	V	

CAPACITANCE\*(T<sub>A</sub>=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF

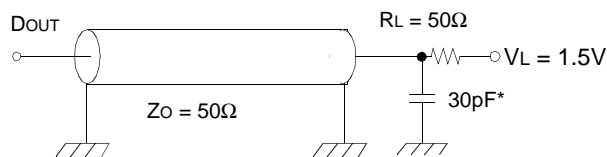
\* Capacitance is sampled and not 100% tested.

## AC CHARACTERISTICS (TA=0 to 70°C, VCC=3.3±0.3V, unless otherwise noted.)

### TEST CONDITIONS

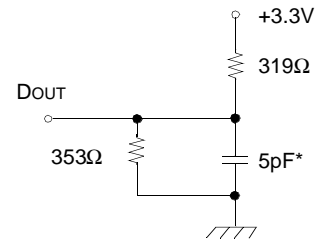
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



\* Capacitive Load consists of all components of the test environment.

\* Including Scope and Jig Capacitance

### READ CYCLE

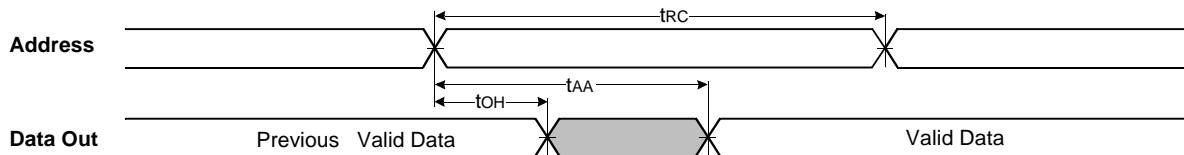
Parameter	Symbol	K6R1004V1B-8		K6R1004V1B-10		K6R1004V1B-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	ns
Address Access Time	tAA	-	8	-	10	-	12	ns
Chip Select to Output	tCO	-	8	-	10	-	12	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	ns
Chip Selection to Power Down Time	tPD	-	8	-	10	-	12	ns

WRITE CYCLE

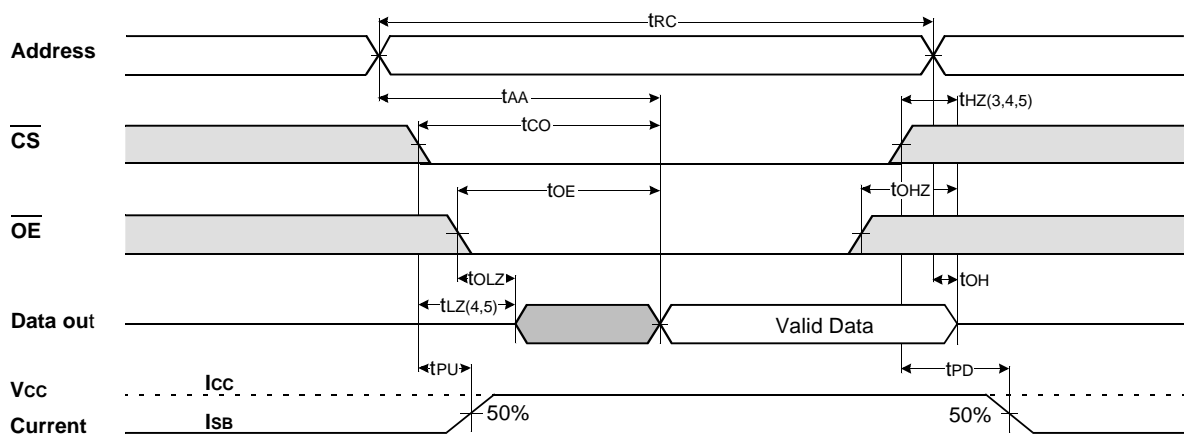
Parameter	Symbol	K6R1004V1B-8		K6R1004V1B-10		K6R1004V1B-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	8	-	10	-	12	-	ns
Chip Select to End of Write	t <sub>CW</sub>	6	-	7	-	8	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Address Valid to End of Write	t <sub>AW</sub>	6	-	7	-	8	-	ns
Write Pulse Width( $\overline{OE}$ High)	t <sub>WP</sub>	6	-	7	-	8	-	ns
Write Pulse Width( $\overline{OE}$ Low)	t <sub>WP1</sub>	8	-	10	-	12	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Write to Output High-Z	t <sub>WHZ</sub>	0	4	0	5	0	6	ns
Data to Write Time Overlap	t <sub>DW</sub>	4	-	5	-	6	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
End Write to Output Low-Z	t <sub>OW</sub>	3	-	3	-	3	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



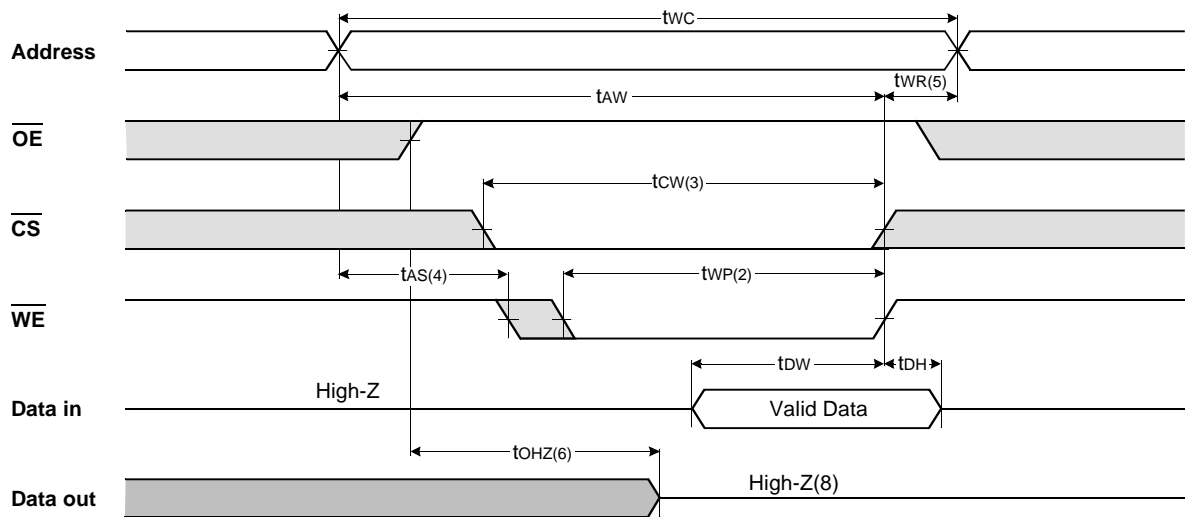
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



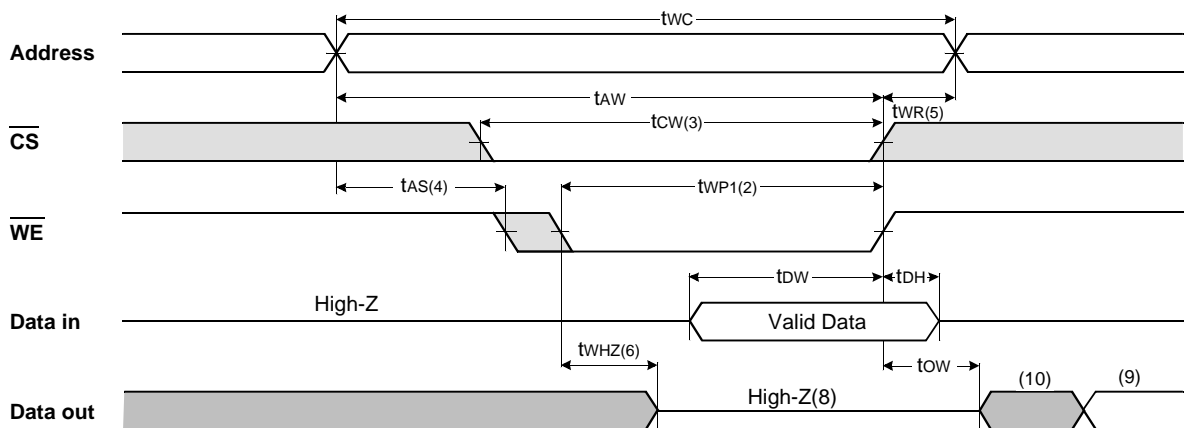
NOTES(READ CYCLE)

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
5. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS}=V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

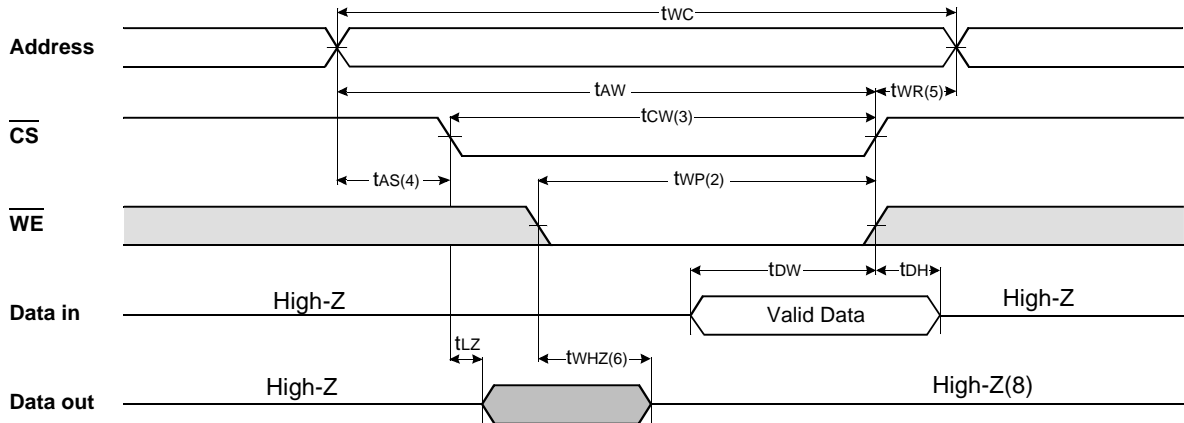
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}=\text{Clock}$ )



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}=\text{Low Fixed}$ )



TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}$ =Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low CS and WE. A write begins at the latest transition CS going low and WE going low ; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
3. tCW is measured from the later of CS going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	DOUT	Icc
L	L	X	Write	DIN	Icc

\* X means Don't Care.

PACKAGE DIMENSIONS

Units: millimeters/Inches

32-SOJ-400

