

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## DESCRIPTION

The M5M29KE131BTP is a Stacked micro Multi Chip Package that contents 2 Dies of 64M-bit Flash memory in a 52-pin TSOP(II) for lead free use.

128M-bit Flash memory is a 16,777,216 bytes / 8,388,608 words, single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR IV (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

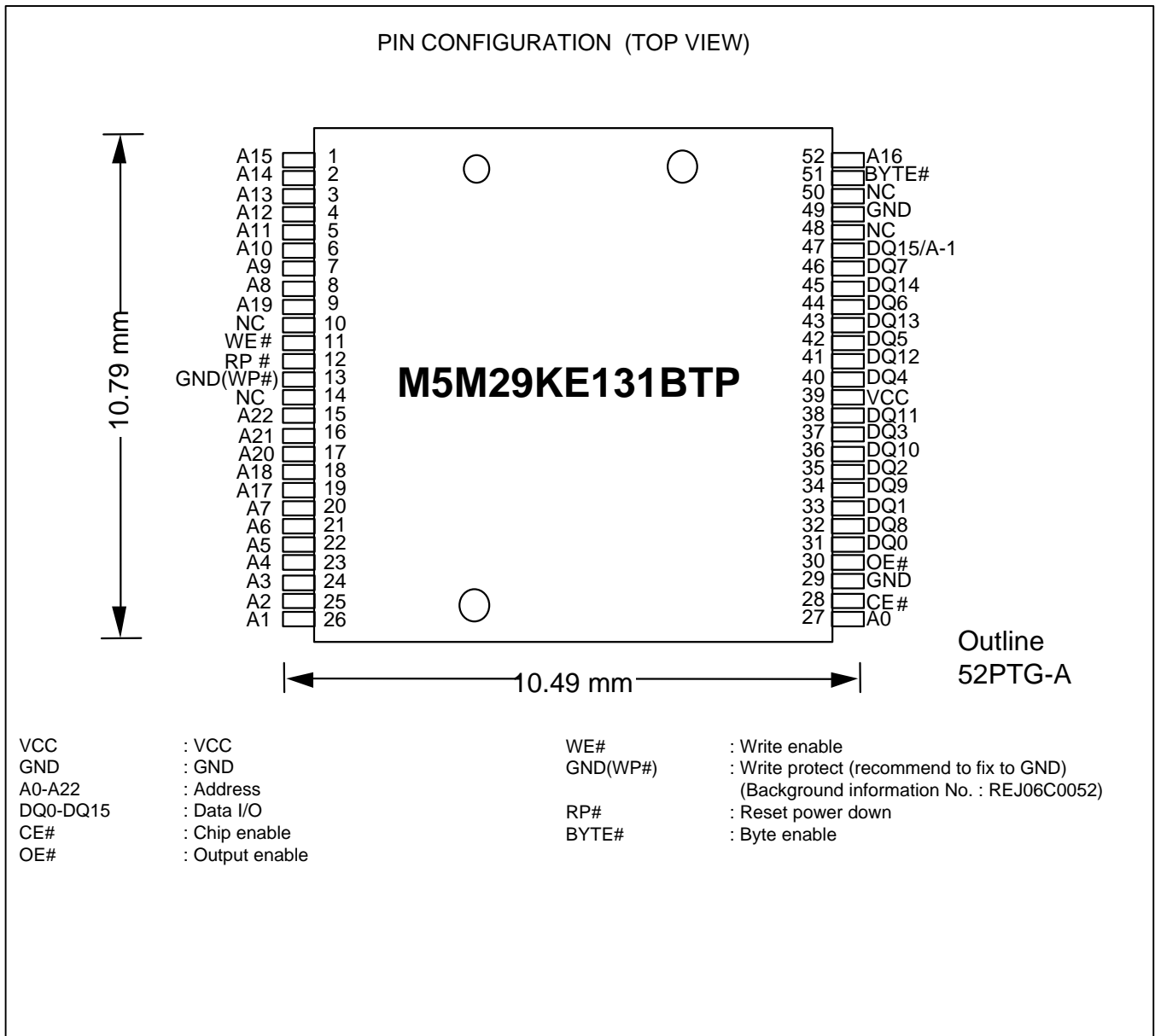
The M5M29KE131BTP is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

## FEATURES

Access time	Random	70ns (Max.)
	Page	25ns(Max.)
Supply voltage		VCC= 3.0 ~ 3.6V
Ambient temperature		Ta=-40 ~ 85 °C
Package	52pin TSOP(Type-II), Lead pitch 0.4mm	
	Outer-lead finishing : Sn-Cu	

## APPLICATION

Digital Cellar Phone, Telecommunication,  
PDA, Car Navigation System, Video Game Machine

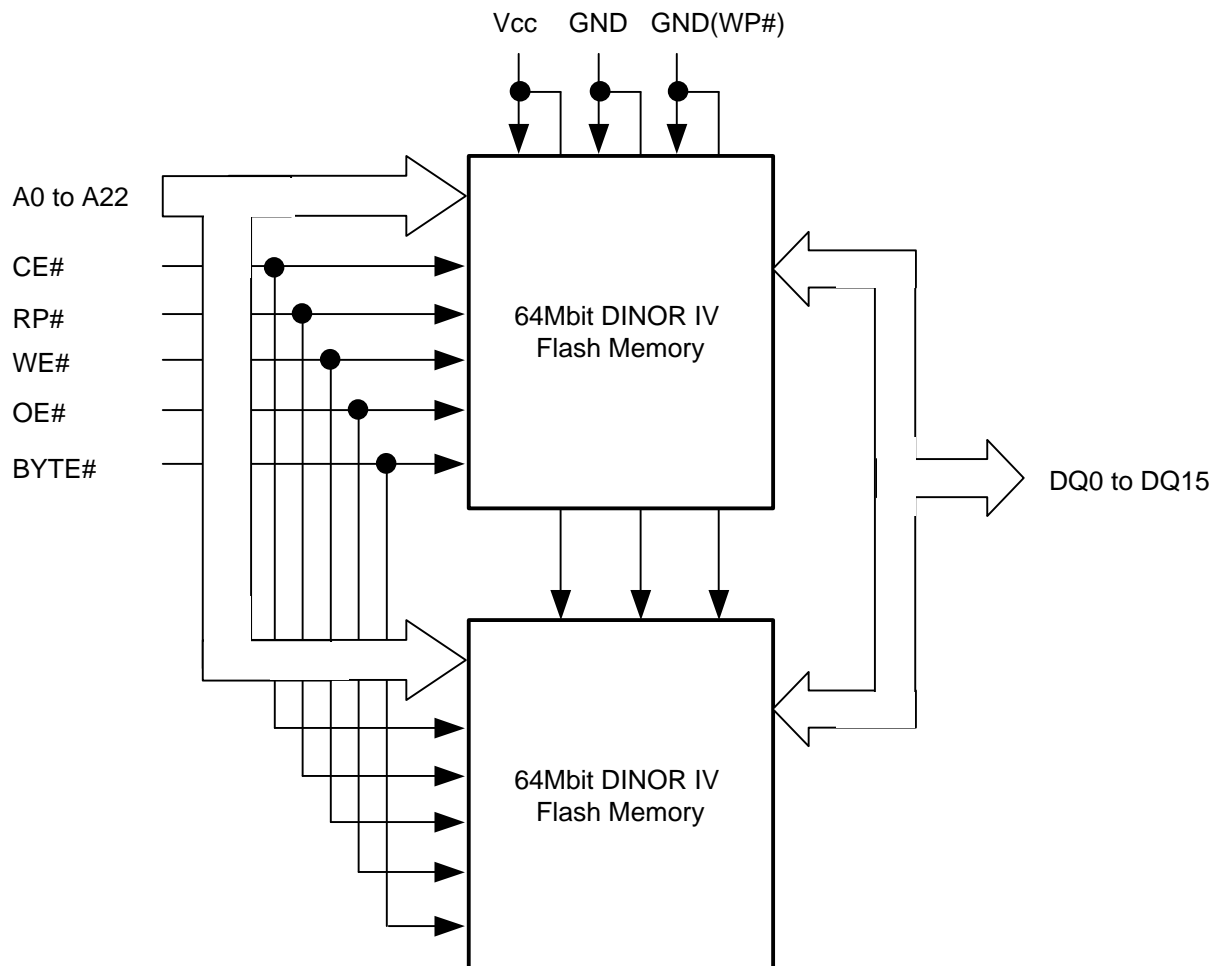


# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## MCP Block Diagram



## Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A22-A0, OE#, WE#, CE#, WP#, RP#, BYTE#	Ta=25°C, f=1MHz, Vin=Vout=0V			24	pF
COUT	Output Capacitance	DQ15-DQ0				24	pF

**M5M29KE131BTP**

**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY**

**Stacked-uMCP (micro Multi Chip Package)**

**Flash Memory Part****Description**

The 128M-bit DINOR IV(Divided bit line NOR IV) Flash Memory is 3.3V-only high speed 134,217,728-bit CMOS boot block Flash Memory. Alternating BGO(Back Ground Operation) feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank in each 64M-bit area which is selected by A22=L or H. This BGO feature is suitable for communication products and cellular phone. The Flash Memory is fabricated by CMOS technology for the peripheral circuits and DINOR IV architecture for the memory cells.

**Features**

- Organization	8,388,608-word x 16-bit 16,777,216-word x 8-bit
- Supply Voltage	VCC = 3.0 ~ 3.6V
- Access time	
Random Access	70ns(Max.)
Random Page Read	25ns(Max.)
- Read	108mW (Max. at 5MHz)
- Page Read	36mW (Max.)
(After Automatic Power Down)	0.66μW(typ.)
- Program/Erase	126mW(Max.)
Standby	0.66μW(typ.)
Deep Power Down mode	0.66μW(typ.)
- Auto Program for Bank(I) – Bank(IV)	
Program Time	
Word Program	30μs/1word(typ.)
Byte Program	30μs/1byte(typ.)
Page Program	4ms(typ.)
Program Unit	
Word Program	1 word
Byte Program	1 byte
Page Program	128 words/256 bytes

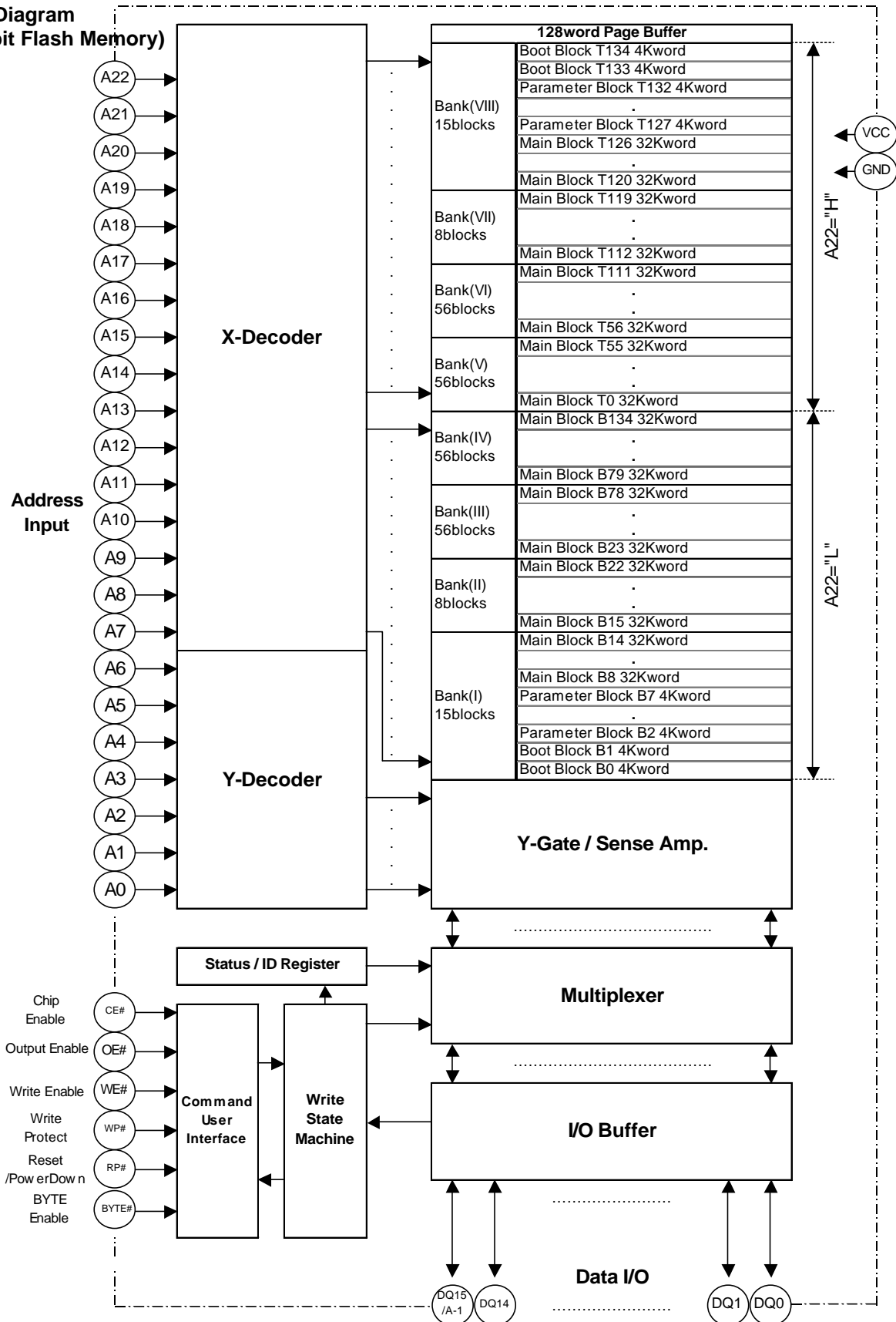
- Auto Erase	
Erase time	150ms(typ.)
Erase unit	
Bank(I) ,Bank(VIII)	
Boot Block	4K-word /8K-byte x 2
Parameter Block	4K-word /8K-byte x 6
Main Block	32K-word /64K-byte x 7
Bank(II) ,Bank(VII)	
Main Block	32K-word /64K-byte 8
Bank(III) ,Bank(VI)	
Main Block	32K-word /64K-byte x 56
Bank(IV) ,Bank(V)	
Main Block	32K-word /64K-byte x 56
- Program/Erase cycles	100Kcycles
- Dual Boot Block Architecture	
There are Bottom and Top boot blocks in both sides.	
Bottom Boot (A22=VIL)	
Top Boot (A22=VIH)	
- The Other Functions	
Software Command Control	
Quick Data Reclaim	
Software Lock Release(while WP# is low)	
Erase Suspend/Resume	
Program Suspend/Resume	
Status Register Read	
Alternating Back Ground Program/Erase Operation	
Among Bank (I)-Bank(IV)	
in Bottom 64Mbit area (A22=VIL),	
Among Bank (V)-Bank(VIII)	
in Top 64Mbit area (A22=VIH)	
Random Page Read	

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

**Block Diagram  
(128Mbit Flash Memory)**



# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Function of Flash Memory

The 128M-bit DINOR IV Flash Memory includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

A Deep Power Down mode is enabled when the RP# pin is at GND, minimizing power consumption.

## Read

The 128M-bit DINOR IV Flash Memory has four read modes, which accesses to the memory array, the Page read, the Device Identifier and the Status Register. The appropriate read commands are required to be written to the CUI. Upon initial device power up or after exit from deep power down, the 128M-bit DINOR IV Flash Memory automatically resets to read array mode. In the read array mode and in the conditions are low level input to OE#, high level input to WE# and RP#, low level input to CE# and address signals to the address inputs (A22 - A0:Word Mode, A22-A-1:Byte Mode) the data of the addressed location to the data input/output (DQ15-DQ0:Word Mode, DQ7-DQ0:Byte Mode) is output.

## Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing WE# to low level and OE# is at high level, while CE# is at low level. Address and data are latched on the earlier rising edge of WE# and CE#. Standard micro processor write timings are used.

## Alternating Background Operation (BGO)

The 128M-bit DINOR IV Flash Memory allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Array Read operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation.

## Output Disable

When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

## Standby

When CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance (High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consumes normal active power until the operation completes.

## Deep Power Down

When RP# is at VIL, the device is in the deep power down mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance (High-Z) state. After return from power down, the CUI is reset to Read Array, and the Status Register is cleared to value 80H.

During block erase or program modes, RP# low will abort either operation. Memory array data of the block being altered become invalid.

## Automatic Power Down (Auto-PD)

The Automatic Power Down minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. During this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

## BBR(Back Bank array Read)

In the 128M-bit DINOR IV Flash Memory, when one memory address is read according to a Read Mode in the case of the same as an access when a Read Mode command is input, another Bank memory data can be read out (Read Array or Page Read) by changing another Bank address.

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Software Command Definitions

The device operations are selected by writing specific software command into the Command User Interface.

### Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep power down, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

### Read Device Identifier Command (90H)

We can normally read device identifier codes when Read Device Identifier Code Command (90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from A0 address 0H and 1H in a bank address, respectively.

### Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of OE# must be toggled every status read.

### Page Read Command (F3H)

The Page Read command (F3H) timing can be used by writing the first command to CUI and CE# falls VIL or changing the address(A22-A2) is necessary to start activating page read mode. This command is fast random 4 words read. During the read it is necessary to fix CE# low and change addresses that are defined by A0 and A1(0h - 3h) at random continuously. The mode is kept until RP# is set to L or this chip is powered down.

The first read of Page Read timing is the same as normal read (ta(CE)). CE# should be fallen "L". The read timing after the first is the same as ta(PAD).

In the page read mode the upper address(A22-A2) or CE# are supposed not to be clocked during read operation. Otherwise the access time is as same as normal read.

### Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicate various failure conditions.

### Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

## Program Commands

### A) Word / Byte Program (40H)

Word/Byte program is executed by a two-command sequence. The Word/Byte program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation.

### B) Page Program for Data Blocks (41H)

Page Program allows fast programming of 128words /256bytes of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle :Word Mode, 257th cycle :Byte Mode, write data must be serially inputted. Address A6-A0:Word Mode, A6-A-1:Byte Mode have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

### C) Single Data Load to Page Buffer (74H)

#### / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address(A6-A0:Word Mode, A6-A-1:Byte Mode) and data. Distinct data up to 128word/256bytes can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programmed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programming the data on the page buffer is cleared automatically.

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Flash to Page Buffer Command (F1H/D0H)

Array data load to the page buffer is performed by writing the Flash to Page Buffer command of F1H followed by the Confirm command of D0H. An address within the page to be loaded is required. Then the array data can be copied into the other pages within the same bank by using the Page Buffer to Flash command.

## Clear Page Buffer Command (55H/D0H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

## Data Protection

The 128M-bit DINOR IV Flash Memory has a master Write Protect pin (WP#). When WP# is at VIH, all blocks can be programmed or erased. When WP# is low, all blocks are in locked mode which prevents any modifications to memory blocks. Software Lock Release function is only command which allows to program or erase.

## Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

## Erase All Unlocked Blocks Command (A7H/D0H)

The command sequence enable us to erase all blocks. The command can be used by writing Setup command A7H(1<sup>st</sup> cycle) and confirm command D0H(2<sup>nd</sup> cycle). The sequence is not valid in case of WP#=VIL.

## Power Supply Voltage

When the power supply voltage is less than VLKO, Low VCC Lock-Out voltage, the device is set to the Read-only mode.

A delay time of 60μs is required before any device operation is initiated. The delay time is measured from the time Flash VCC reaches Flash VCCmin (3.0V).

During power up, RP# = GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

## Memory Organization

The 128M-bit DINOR IV Flash Memory is constructed by 2 boot blocks of 4K words, 6 parameter blocks of 4K words and 7 main blocks of 32K words in Bank(I) and Bank(VIII), by 8 main blocks of 32K words in Bank(II) and Bank(VII), and by 56 main blocks of 32K words in Bank(III), BANK(IV), BANK(V) and Bank(VI).

A block is erased independently of other blocks in the array.

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Block Organization

## 128M-bit DINOR(IV) Flash Memory Map (Bottom 64Mbit / A22=VIL)

x8 (Byte Mode)	x16 (Word Mode)		x8 (Byte Mode)	x16 (Word Mode)		x8 (Byte Mode)	x16 (Word Mode)		x8 (Byte Mode)	x16 (Word Mode)		x8 (Byte Mode)	x16 (Word Mode)	
1A0000H-1AFFFFH	D0000H-D7FFFH	32Kw ord 33	3C0000H-3CFFFFH	1E0000H-1E7FFFH	32Kw ord 67	5E0000H-5EFFFFH	2F0000H-2F7FFFH	32Kw ord 101	7F0000H-7FFFFFH	3F8000H-3FFFFFH	32Kw ord 134			
190000H-19FFFFH	C8000H-CFFFFH	32Kw ord 32	3B0000H-3BFFFFH	1D8000H-1DFFFFH	32Kw ord 66	5D0000H-5DFFFFH	2E8000H-2EFFFFH	32Kw ord 100	7E0000H-7EFFFFH	3F0000H-3F7FFFH	32Kw ord 133			
180000H-18FFFFH	C0000H-C7FFFH	32Kw ord 31	3A0000H-3AFFFFH	1D0000H-1D7FFFH	32Kw ord 65	5C0000H-5CFFFFH	2E0000H-2E7FFFH	32Kw ord 99	7D0000H-7DFFFFH	3E8000H-3EFFFFH	32Kw ord 132			
170000H-17FFFFH	B8000H-BFFFFH	32Kw ord 30	390000H-39FFFFH	1C8000H-1C7FFFH	32Kw ord 64	5B0000H-5BFFFFH	2D8000H-2DFFFFH	32Kw ord 98	7C0000H-7CFFFFH	3E0000H-3E7FFFH	32Kw ord 131			
160000H-16FFFFH	B0000H-B7FFFH	32Kw ord 29	380000H-38FFFFH	1C0000H-1C7FFFH	32Kw ord 63	5A0000H-5AFFFFH	2D0000H-2D7FFFH	32Kw ord 97	7B0000H-7BFFFFH	3D8000H-3DFFFFH	32Kw ord 130			
150000H-15FFFFH	A8000H-A7FFFH	32Kw ord 28	370000H-37FFFFH	1B8000H-1B7FFFH	32Kw ord 62	590000H-59FFFFH	2C8000H-2C7FFFH	32Kw ord 96	7A0000H-7AFFFFH	3D0000H-3D7FFFH	32Kw ord 129			
140000H-14FFFFH	A0000H-A7FFFH	32Kw ord 27	360000H-36FFFFH	1B0000H-1B7FFFH	32Kw ord 61	580000H-58FFFFH	2C0000H-2C7FFFH	32Kw ord 95	790000H-79FFFFH	3C8000H-3CFFFFH	32Kw ord 128			
130000H-13FFFFH	98000H-97FFFH	32Kw ord 26	350000H-35FFFFH	1A8000H-1A7FFFH	32Kw ord 60	570000H-57FFFFH	2B8000H-2B7FFFH	32Kw ord 94	780000H-78FFFFH	3C0000H-3C7FFFH	32Kw ord 127			
120000H-12FFFFH	90000H-97FFFH	32Kw ord 25	340000H-34FFFFH	1A0000H-1A7FFFH	32Kw ord 59	560000H-56FFFFH	2B0000H-2B7FFFH	32Kw ord 93	770000H-77FFFFH	3B8000H-3BFFFFH	32Kw ord 126			
110000H-11FFFFH	88000H-87FFFH	32Kw ord 24	330000H-33FFFFH	198000H-197FFFH	32Kw ord 58	550000H-55FFFFH	2A8000H-2A7FFFH	32Kw ord 92	760000H-76FFFFH	3B0000H-3B7FFFH	32Kw ord 125			
100000H-10FFFFH	80000H-87FFFH	32Kw ord 23	320000H-32FFFFH	190000H-197FFFH	32Kw ord 57	540000H-54FFFFH	2A0000H-2A7FFFH	32Kw ord 91	750000H-75FFFFH	3A8000H-3A7FFFH	32Kw ord 124			
F0000H-FFFFH	78000H-77FFFH	32Kw ord 22	310000H-31FFFFH	188000H-187FFFH	32Kw ord 56	530000H-53FFFFH	298000H-297FFFH	32Kw ord 90	740000H-74FFFFH	3A0000H-3A7FFFH	32Kw ord 123			
E0000H-EFFFFH	70000H-77FFFH	32Kw ord 21	300000H-30FFFFH	180000H-187FFFH	32Kw ord 55	520000H-52FFFFH	290000H-297FFFH	32Kw ord 89	730000H-73FFFFH	398000H-397FFFH	32Kw ord 122			
D0000H-DFFFFH	68000H-67FFFH	32Kw ord 20	2F0000H-2FFFFFH	178000H-177FFFH	32Kw ord 54	510000H-51FFFFH	288000H-287FFFH	32Kw ord 88	720000H-72FFFFH	390000H-397FFFH	32Kw ord 121			
C0000H-CFFFFH	60000H-67FFFH	32Kw ord 19	2E0000H-2EFFFFH	170000H-177FFFH	32Kw ord 53	500000H-50FFFFH	280000H-287FFFH	32Kw ord 87	710000H-71FFFFH	388000H-387FFFH	32Kw ord 120			
B0000H-BFFFFH	58000H-57FFFH	32Kw ord 18	2D0000H-2DFFFFH	168000H-167FFFH	32Kw ord 52	4F0000H-4FFFFFH	278000H-277FFFH	32Kw ord 86	70000H-70FFFFH	380000H-387FFFH	32Kw ord 119			
A0000H-AFFFFH	50000H-57FFFH	32Kw ord 17	2C0000H-2CFFFFH	160000H-167FFFH	32Kw ord 51	4E0000H-4EFFFFH	270000H-277FFFH	32Kw ord 85	6F0000H-6FFFFFH	378000H-377FFFH	32Kw ord 118			
90000H-9FFFFH	48000H-47FFFH	32Kw ord 16	2B0000H-2BFFFFH	158000H-157FFFH	32Kw ord 50	4D0000H-4DFFFFH	268000H-267FFFH	32Kw ord 84	6E0000H-6EFFFFH	370000H-377FFFH	32Kw ord 117			
80000H-8FFFFH	40000H-47FFFH	32Kw ord 15	2A0000H-2AFFFFH	150000H-157FFFH	32Kw ord 49	4C0000H-4CFFFFH	260000H-267FFFH	32Kw ord 83	6D0000H-6DFFFFH	368000H-367FFFH	32Kw ord 116			
70000H-7FFFFH	38000H-37FFFH	32Kw ord 14	290000H-29FFFFH	148000H-147FFFH	32Kw ord 48	4B0000H-4BFFFFH	258000H-257FFFH	32Kw ord 82	6C0000H-6CFFFFH	360000H-367FFFH	32Kw ord 115			
60000H-6FFFFH	30000H-37FFFH	32Kw ord 13	280000H-28FFFFH	140000H-147FFFH	32Kw ord 47	4A0000H-4AFFFFH	250000H-257FFFH	32Kw ord 81	6B0000H-6BFFFFH	358000H-357FFFH	32Kw ord 114			
50000H-5FFFFH	28000H-27FFFH	32Kw ord 12	270000H-27FFFFH	138000H-137FFFH	32Kw ord 46	490000H-49FFFFH	248000H-247FFFH	32Kw ord 80	6A0000H-6AFFFFH	350000H-357FFFH	32Kw ord 113			
40000H-4FFFFH	20000H-27FFFH	32Kw ord 11	260000H-26FFFFH	130000H-137FFFH	32Kw ord 45	480000H-48FFFFH	240000H-247FFFH	32Kw ord 79	690000H-69FFFFH	348000H-347FFFH	32Kw ord 112			
30000H-3FFFFH	18000H-17FFFH	32Kw ord 10	250000H-25FFFFH	128000H-127FFFH	32Kw ord 44	470000H-47FFFFH	238000H-237FFFH	32Kw ord 78	680000H-68FFFFH	340000H-347FFFH	32Kw ord 111			
20000H-2FFFFH	10000H-17FFFH	32Kw ord 9	240000H-24FFFFH	120000H-127FFFH	32Kw ord 43	460000H-46FFFFH	230000H-237FFFH	32Kw ord 77	670000H-67FFFFH	338000H-337FFFH	32Kw ord 110			
10000H-1FFFFH	08000H-07FFFH	32Kw ord 8	230000H-23FFFFH	118000H-117FFFH	32Kw ord 42	450000H-45FFFFH	228000H-227FFFH	32Kw ord 76	660000H-66FFFFH	330000H-337FFFH	32Kw ord 109			
0E000H-0FFFFH	07000H-07FFFH	4Kw ord 7	220000H-22FFFFH	110000H-117FFFH	32Kw ord 41	440000H-44FFFFH	220000H-227FFFH	32Kw ord 75	650000H-65FFFFH	328000H-327FFFH	32Kw ord 108			
0C000H-0DFFFH	06000H-06FFFH	4Kw ord 6	210000H-21FFFFH	108000H-107FFFH	32Kw ord 40	430000H-43FFFFH	218000H-217FFFH	32Kw ord 74	640000H-64FFFFH	320000H-327FFFH	32Kw ord 107			
0A000H-0BFFFH	05000H-05FFFH	4Kw ord 5	200000H-20FFFFH	100000H-107FFFH	32Kw ord 39	420000H-42FFFFH	210000H-217FFFH	32Kw ord 73	630000H-63FFFFH	318000H-317FFFH	32Kw ord 106			
08000H-09FFFH	04000H-04FFFH	4Kw ord 4	1F0000H-1FFFFH	F8000H-FFFFH	32Kw ord 38	410000H-41FFFFH	208000H-207FFFH	32Kw ord 72	620000H-62FFFFH	310000H-317FFFH	32Kw ord 105			
06000H-07FFFH	03000H-03FFFH	4Kw ord 3	1E0000H-1EFFFFH	F0000H-F7FFFH	32Kw ord 37	40000H-40FFFFH	20000H-207FFFH	32Kw ord 71	610000H-61FFFFH	308000H-307FFFH	32Kw ord 104			
04000H-05FFFH	02000H-02FFFH	4Kw ord 2	1D0000H-1DFFFFH	E8000H-E7FFFH	32Kw ord 36	3F0000H-3FFFFH	1F8000H-1FFFFH	32Kw ord 70	60000H-60FFFFH	30000H-307FFFH	32Kw ord 103			
02000H-03FFFH	01000H-01FFFH	4Kw ord 1	1C0000H-1CFFFFH	E0000H-E7FFFH	32Kw ord 35	3E0000H-3EFFFFH	1F0000H-1F7FFFH	32Kw ord 69	5F0000H-5FFFFH	2F8000H-2FFFFH	32Kw ord 102			
00000H-01FFFH	00000H-00FFFH	4Kw ord 0	1B0000H-1BFFFFH	D8000H-D7FFFH	32Kw ord 34	3D0000H-3DFFFFH	1E8000H-1EFFFFH	32Kw ord 68						





**M5M29KE131BTP**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

**Bus Operation****BYTE#=VIH**

Mode		Pins	CE#	OE#	WE#	RP#	DQ0-15
Read	Array		VIL	VIL	VIH	VIH	Data Output
	Status Register		VIL	VIL	VIH	VIH	Status Register Data
	Identifier Code		VIL	VIL	VIH	VIH	Identifier Code
	Page		VIL	VIL	VIH	VIH	Data Output
Output Disable			VIL	VIH	VIH	VIH	High-Z
Write	Program		VIL	VIH	VIL	VIH	Command/Data in
	Erase		VIL	VIH	VIL	VIH	Command
	Others		VIL	VIH	VIL	VIH	Command
Stand by			VIH	X <sup>1)</sup>	X <sup>1)</sup>	VIH	High-Z
Deep Power Down			X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	VIL	High-Z

**BYTE#=VIL**

Mode		Pins	CE#	OE#	WE#	RP#	DQ0-7
Read	Array		VIL	VIL	VIH	VIH	Data Output
	Status Register		VIL	VIL	VIH	VIH	Status Register Data
	Identifier Code		VIL	VIL	VIH	VIH	Identifier Code
	Page		VIL	VIL	VIH	VIH	Data Output
Output Disable			VIL	VIH	VIH	VIH	High-Z
Write	Program		VIL	VIH	VIL	VIH	Command/Data in
	Erase		VIL	VIH	VIL	VIH	Command
	Others		VIL	VIH	VIL	VIH	Command
Stand by			VIH	X <sup>1)</sup>	X <sup>1)</sup>	VIH	High-Z
Deep Power Down			X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	VIL	High-Z

1) X can be VIH or VIL for control pins.

**M5M29KE131BTP**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

**Software Command Definition****Command List (WP# =VIH or VIL)**

Command	1st Bus Cycle			2nd Bus Cycle			3rd-5th Bus Cycle			
	Mode	Address	Data <sup>1)</sup> (DQ0-15)(DQ0-7)	Mode	Address A22-A18 A0		Data <sup>1)</sup> (DQ0-15)(DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15)(DQ0-7)
Read Array	Write	A22 <sup>7)</sup> A0-A21=X <sup>8)</sup>	FFH							
Page Read	Write	A22 <sup>7)</sup> A0-A21=X <sup>8)</sup>	F3H	Read	SA <sup>5)</sup>		RD0	Read	SA+i <sup>6)</sup>	RD <i>i</i>
Device Identifier	Write	A22=VIL A0-A21=X <sup>8)</sup>	90H	Read	A22=VIL Bank <sup>2)</sup>	IA <sup>3)</sup>	ID			
Read Status Register	Write	Bank <sup>2)</sup>	70H	Read	Bank <sup>2)</sup>		SRD <sup>4)</sup>			
Clear Status Register	Write	A22 <sup>7)</sup> A0-A21=X <sup>8)</sup>	50H							
Suspend	Write	Bank <sup>2)</sup>	B0H							
Resume	Write	Bank <sup>2)</sup>	D0H							

1) In the case of Word mode(BYTE#=VIH), upper byte data (DQ15-DQ8) is ignored.

2) Bank=Bank address (Bank(I)-Bank(VIII): A22-18)

3) IA=ID code address: A0=VIL (Manufacturer's code): A0=VIH (Device code), ID=ID code

4) SRD=Status Register Data

5) SA=A21-A2:1<sup>st</sup> Page Address, A1,A0:voluntary address / RD0=1<sup>st</sup> Page read data6) SA+i: Page address(is equal to 1<sup>st</sup> Page Address of A21-A2), A1,A0: voluntary address / RD*i*: 2<sup>nd</sup> Page read data

7) In case of Bottom 64M-bit area, A22 must be set to VIL.

In case of Top 64M-bit area, A22 must be set to VIH.

8) X can be VIH or VIL.

**Command List (WP# =VIH)**

Command	1st Bus Cycle			2nd Bus Cycle			3rd-129th Bus Cycles 3rd-257th Bus Cycles(Byte mode)		
	Mode	Address	Data <sup>1)</sup> (DQ0-15)(DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15)(DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15)(DQ0-7)
Word Program	Write	Bank <sup>7)</sup>	40H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>			
Page Program	Write	Bank <sup>7)</sup>	41H	Write	WA0 <sup>3)</sup>	WD0 <sup>3)</sup>	Write	WA <i>n</i> <sup>3)</sup>	WD <i>n</i> <sup>3)</sup>
Page Buffer to Flash	Write	Bank <sup>7)</sup>	0EH	Write	WA <sup>4)</sup>	D0H <sup>1)</sup>			
Block Erase/Confirm	Write	Bank <sup>7)</sup>	20H	Write	BA <sup>5)</sup>	D0H <sup>1)</sup>			
Erase All Unlocked Blocks	Write	A22 <sup>8)</sup> A0-A21=X <sup>9)</sup>	A7H	Write	A22 <sup>8)</sup> A0-A21=X <sup>9)</sup>	D0H <sup>1)</sup>			
Clear Page Buffer	Write	A22 <sup>8)</sup> A0-A21=X <sup>9)</sup>	55H	Write	A22 <sup>8)</sup> A0-A21=X <sup>9)</sup>	D0H <sup>1)</sup>			
Single Data Load to Page Buffer	Write	A22 <sup>8)</sup> A0-A21=X <sup>9)</sup>	74H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>			
Flash to Page Buffer	Write	Bank <sup>7)</sup>	F1H	Write	RA <sup>6)</sup>	D0H <sup>1)</sup>			

1) In the case of Word mode(BYTE#=VIH), upper byte data (DQ15-DQ8) is ignored.

2) WA=Write Address, WD=Write Data

3) WA0, WA*n*=Write Address, WD0, WD*n*=Write Data.

Word mode (BYTE#=VIH) : Write address and write data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128 words (128-word x 16-bit), and also A22-A7 (block address, page address) must be valid.

Byte mode (BYTE#=VIL) : Write address and write data must be provided sequentially from 00H to FFH for A6-A-1. Page size is 256 Bytes (256-byte x 8-bit), and also A22-A7 (block address, page address) must be valid.

4) WA=Write Address: A22-A7 (block address, page address) must be valid.

5) BA=Block Address : A22-A12[Bank(I),Bank(VIII)], A22-A15 [Bank(II) ~ Bank(VII)]

6) RA=Read Address: A22-A7 (block address, page address) must be valid.

7) Bank=Bank address (Bank(I)-Bank(VIII): A22-18)

8) In case of Bottom 64M-bit area, A22 must be set to VIL. In case of Top 64M-bit area, A22 must be set to VIH.

9) X can be VIH or VIL.

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Software Command Definition Command List (WP# =VIL)

Software lock release operation needs following consecutive 7bus cycles. Moreover, additional 127(255) bus cycles are needed for page program operation.

Setup Command for Software Lock Release	1st Bus Cycle			2nd Bus Cycle			3rd Bus Cycle		
	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)
Word Program	Write	Bank <sup>8)</sup>	60H	Write	Bank <sup>8)</sup>	Block <sup>6)</sup>	Write	Bank <sup>8)</sup>	ACH
Page Program	Write	Bank <sup>8)</sup>	60H	Write	Bank <sup>8)</sup>	Block <sup>6)</sup>	Write	Bank <sup>8)</sup>	ACH
Page Buffer to Flash	Write	Bank <sup>8)</sup>	60H	Write	Bank <sup>8)</sup>	Block <sup>6)</sup>	Write	Bank <sup>8)</sup>	ACH
Block Erase/Confirm	Write	Bank <sup>8)</sup>	60H	Write	Bank <sup>8)</sup>	Block <sup>6)</sup>	Write	Bank <sup>8)</sup>	ACH
Clear Page Buffer	Write	Bank <sup>8)</sup>	60H	Write	Bank <sup>8)</sup>	Block <sup>6)</sup>	Write	Bank <sup>8)</sup>	ACH
Single Data Load to Page Buffer	Write	Bank <sup>8)</sup>	60H	Write	Bank <sup>8)</sup>	Block <sup>6)</sup>	Write	Bank <sup>8)</sup>	ACH
Flash to Page Buffer	Write	Bank <sup>8)</sup>	60H	Write	Bank <sup>8)</sup>	Block <sup>6)</sup>	Write	Bank <sup>8)</sup>	ACH

Setup Command for Software Lock Release	4th Bus Cycle			5th Bus Cycle		
	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)
Word Program	Write	Bank <sup>8)</sup>	Block# <sup>6)</sup>	Write	Bank <sup>8)</sup>	7BH
Page Program	Write	Bank <sup>8)</sup>	Block# <sup>6)</sup>	Write	Bank <sup>8)</sup>	7BH
Page Buffer to Flash	Write	Bank <sup>8)</sup>	Block# <sup>6)</sup>	Write	Bank <sup>8)</sup>	7BH
Block Erase/Confirm	Write	Bank <sup>8)</sup>	Block# <sup>6)</sup>	Write	Bank <sup>8)</sup>	7BH
Clear Page Buffer	Write	Bank <sup>8)</sup>	Block# <sup>6)</sup>	Write	Bank <sup>8)</sup>	7BH
Single Data Load to Page Buffer	Write	Bank <sup>8)</sup>	Block# <sup>6)</sup>	Write	Bank <sup>8)</sup>	7BH
Flash to Page Buffer	Write	Bank <sup>8)</sup>	Block# <sup>6)</sup>	Write	Bank <sup>8)</sup>	7BH

Setup Command for Program or Erase Operations	6th Bus Cycle			7th Bus Cycle			8th-134th Bus Cycles 8th-262th Bus Cycles(Byte mode)		
	Mode	Address	Data <sup>1)</sup> (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)	Mode	Address	Data (DQ0-15/DQ0-7)
Word Program	Write	Bank <sup>8)</sup>	40H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>			
Page Program	Write	Bank <sup>8)</sup>	41H	Write	WA0 <sup>3)</sup>	WD0 <sup>3)</sup>	Write	WAn <sup>3)</sup>	WDn <sup>3)</sup>
Page Buffer to Flash	Write	Bank <sup>8)</sup>	0EH	Write	WA <sup>4)</sup>	D0H <sup>1)</sup>			
Block Erase/Confirm	Write	Bank <sup>8)</sup>	20H	Write	BA <sup>5)</sup>	D0H <sup>1)</sup>			
Clear Page Buffer	Write	A22 <sup>9)</sup> A0-A21=X <sup>10)</sup>	55H	Write	A22 <sup>9)</sup> A0-A21=X <sup>10)</sup>	D0H <sup>1)</sup>			
Single Data Load to Page Buffer	Write	A22 <sup>9)</sup> A0-A21=X <sup>10)</sup>	74H	Write	WA <sup>2)</sup>	WD <sup>2)</sup>			
Flash to Page Buffer	Write	Bank <sup>8)</sup>	F1H	Write	RA <sup>7)</sup>	D0H <sup>1)</sup>			

1) In the case of word mode(BYTE#=VIH) upper byte data (DQ15-DQ8) is ignored.

2) WA=Write Address, WD=Write Data

3) WA0, WAn=Write Address, WD0, WDn=Write Data. Write address and write data must be provided sequentially from 00H to 7FH for A6-A0(word mode) and from 00H to FFH for A6-A-1(byte mode), respectively.

Page size is 128 words (128-word x 16-bit/ word mode) or Page size is 256 bytes (256-word x 8-bit/ byte mode), and also A22-A7 (block address, page address) must be valid.

4) WA=Write Address: A22-A7 (block address, page address) must be valid.

5) BA=Block Address : A21-A12[Bank(I),Bank(VIII)], A21-A15 [Bank(II) ~ Bank(VII)]

6) Block=Block Address: A21-A15, Block#=A21#-A15#

Address	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Block	fixed 0	A21	A20	A19	A18	A17	A16	A15
Block#	fixed 0	A21#	A20#	A19#	A18#	A17#	A16#	A15#

7) RA=Read Address: A22-A7 (block address, page address) must be valid.

8) Bank=Bank address (Bank(I)-Bank(VIII): A22-18)

**9) In case of Bottom 64M-bit area, A22 must be set to VIL.**

**In case of Top 64M-bit area, A22 must be set to VIH.**

10) X can be VIH or VIL.

**M5M29KE131BTP**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

**Block Locking**

RP#	WP#	Write Protection Provided					Notes
		Bank (I),(VIII)		Bank (II),(VII)	Bank (III),(VI)	Bank (IV),(V)	
		Boot	Parameter/Main	Main	Main	Main	
VIL	X	Locked	Locked	Locked	Locked	Locked	Deep Power Down Mode
VIH	VIL	Locked	Locked	Locked	Locked	Locked	All Blocks Locked(Valid to operate Software Lock Release)
	VIH	Unlocked	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

WP# pin must not be switched during performing Read / Write operations or WSM busy (WSMS=0).

**Status Register**

Symbol (I/O Pin)	Status	Definition	
		"1"	"0"
S.R. 7 (DQ7)	Write State Machine Status	Ready	Busy
S.R. 6 (DQ6)	Suspend Status	Suspended	Operation in Progress/Completed
S.R. 5 (DQ5)	Erase Status	Error	Successful
S.R. 4 (DQ4)	Program Status	Error	Successful
S.R. 3 (DQ3)	Block Status after Erase	Error	Successful
S.R. 2 (DQ2)	Reserved	-	-
S.R. 1 (DQ1)	Reserved	-	-
S.R. 0 (DQ0)	Reserved	-	-

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Device ID Code

Pins	A22	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex. Data
Code											
Manufacturer Code	VIL	VIL	"0"	"0"	"0"	"1"	"1"	"1"	"0"	"0"	1CH
Device Code	VIL	VIH	"1"	"0"	"1"	"1"	"1"	"0"	"0"	"1"	B9H

The output of upper byte data (DQ15-DQ8) is "0H". A22 must be set "VIL".

## Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Units
VCC	VCC Voltage	With Respect to GND	-0.2	4.6	V
VI1	All Input or Output Voltage <sup>1)</sup>		-0.6	4.6	V
Ta	Ambient Temperature		-40	85	°C
Tbs	Temperature under Bias		-50	95	°C
Tstg	Storage Temperature		-65	125	°C
Iout	Output Short Circuit Current			100	mA

1)Minimum DC voltage is -0.6V on input / output pins. During transitions, the level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is VCC+0.5V which, during transitions, may overshoot to VCC+1.5V for periods <20ns.

## DC electrical characteristics (Ta= -40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits		
			Min.	Typ. <sup>1)</sup>	Max.
ILI	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	-2		2
ILO	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$	-20		20
ISB2	VCC Stand by Current	VCC= 3.6V, VIN= GND/VCC, CE#= RP#= WP#= VCC±0.3V		0.2	12
ISB3	VCC Deep Power Down Current	VCC= 3.6V, VIN= VIL/VIH, RP#= VIL		10	50
ISB4		VCC= 3.6V, VIN= GND or VCC, RP#= GND± 0.3V		0.2	12
ICC1	VCC Read Current for Word	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# =VIL, Iout = 0mA	5MHz	20	30
			1MHz	4	8
ICC1P	VCC Page Read Current for Word	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# = VIL, Iout = 0mA		5	10
ICC2	VCC Write Current for Word	Vcc = 3.6V, VIN = VIL/VIH, RP# = OE# = VIH, CE# = WE# = VIL			15
ICC3	VCC Program Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = WP# = VIH			35
ICC4	VCC Erase Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = WP# = VIH			35
ICC5	VCC Suspend Current	VCC = 3.6V, VIN = VIL/VIH, CE#= RP# = WP# = VIH			400
VIL	Input Low Voltage		-0.5		0.4
VIH	Input High Voltage		2.4		VCC+0.5
VOL	Output Low Voltage	IOL = 4.0mA			0.45
VOH1	Output High Voltage	IOH = -2.0mA		0.85xVCC	
VOH2		IOH = -100uA		VCC-0.4	
VLKO	Low VCC Lock Out Voltage <sup>2)</sup>		1.5		2.2

All currents are in RMS unless otherwise noted.

1) Typical values at Flash VCC=3.3V, Ta=25 °C.

2) To protect against initiation of write cycle during Flash VCC power up / down, a write cycle is locked out for Flash VCC less than VLKO. If Flash VCC is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Flash VCC is less than VLKO, the alteration of memory contents may occur.

**M5M29KE131BTP**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

**AC electrical characteristics** (Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)**Read Only Mode**

Symbol		Parameter	Limits			Units
			Flash VCC=3.0-3.6V			
			Min.	Typ.	Max.	
tRC	tAVAV	Read Cycle Time	70			ns
ta(AD)	tAVQV	Address Access Time			70	ns
ta(CE)	tELQV	Chip Enable Access Time			70	ns
ta(OE)	tGLQV	Output Enable Access Time			30	ns
ta(PAD)	tPAVQV	Page Read Access Time			25	ns
tCEPH		CE# "H" Pulse width	30			ns
tCLZ	tELQX	Chip Enable to Output in Low-Z	0			ns
tDF(CE)	tEHQZ	Chip Enable High to Output in High-Z			25	ns
tOLZ	tGLQX	Output Enable to Output in Low-Z	0			ns
tDF(OE)	tGHQZ	Output Enable to High to Output in High-Z			25	ns
tPHZ	tPLQZ	RP# Low to Output High-Z			150	ns
ta(BYTE)	tFL/HQV	BYTE# access time			70	ns
tBHZ	tFLQZ	BYTE# low to output high-Z			25	ns
tOH	tOH	Output Hold from CE#, OE# and Addresses	0			ns
tBCD	tELFL/H	CE# low to BYTE# high or low			5	ns
tBAD	tAVFL/H	Address to BYTE# high or low			5	ns
tOEH	tWHGL	OE# Hold from WE# High	10			ns
tPS	tPHL	RP# Recovery to CE# Low	150			ns

-Timing measurements are made under AC waveforms for read operations.

**M5M29KE131BTP**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

**AC electrical characteristics** (Ta=-40 ~85 °C and Flash VCC=3.0V~3.6V, unless otherwise noted)**Read / Write Mode (WE# control)**

Symbol	Parameter	Limits			Units	
		Flash VCC=3.0-3.6V				
		Min.	Typ.	Max.		
tWC	tAVAV	Write Cycle Time	70		ns	
tAS	tAVWH	Address Setup Time	35		ns	
tAH	tWHAX	Address Hold Time	0		ns	
tDS	tDVWH	Data Setup Time	35		ns	
tDH	tWHDX	Data Hold Time	0		ns	
tOEH	tWHGL	OE# Hold from WE# High	10		ns	
tCS	tELWL	Chip Enable Setup Time	0		ns	
tCH	tWHEH	Chip Enable Hold Time	0		ns	
tWP	tWLWH	Write Pulse Width	35		ns	
tWPH	tWHWL	Write Pulse Width High	30		ns	
tBS	tFL/HWH	Byte enable high or low set-up time	35		ns	
tBH	tWHFL/H	Byte enable high or low hold time	70		ns	
tGHWL	tGHWL	OE# Hold to WE# Low	0		ns	
tBLS	tPHHWH	Block Lock Setup to Write Enable High	70		ns	
tBLH	tQVPH	Block Lock Hold from Valid SRD	0		ns	
tDAP	tWHRH1	Duration of Auto Program Operation(Word Mode)		30	300	μs
tDAP	tWHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	μs
tDAP	tWHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tWHRH2	Duration of Auto Block Erase Operation		150	600	ms
tWHRL	tWHRL	Delay Time During Internal Operation			70	ns
tPS	tPHWL	RP# Recovery to CE# Low	150			ns

-Read timing parameters during command write operations mode are the same as during read only operation mode.

-Typical values at Flash VCC=3.3V and Ta=25 °C.

**Read / Write Mode (CE# control)**

Symbol	Parameter	Limits			Units	
		Flash VCC=3.0-3.6V				
		Min.	Typ.	Max.		
tWC	tAVAV	Write Cycle Time	70		ns	
tAS	tAVEH	Address Setup Time	35		ns	
tAH	tEHAX	Address Hold Time	0		ns	
tDS	tDVEH	Data Setup Time	35		ns	
tDH	tEHDX	Data Hold Time	0		ns	
tOEH	tEHGL	OE# Hold from CE# High	10		ns	
tWS	tWLEL	Write Enable Setup Time	0		ns	
tWH	tEHWH	Write Enable Hold Time	0		ns	
tCEP	tELEH	CE# Pulse Width	35		ns	
tCEPH	tEHEL	CE#"H" Pulse Width	30		ns	
tBS	tFL/HEH	Byte enable high or low set-up time	35		ns	
tBH	tEHFL/H	Byte enable high or low hold time	70		ns	
tGHEL	tGHEL	OE# Hold to CE# Low	0		ns	
tBLS	tPHHEH	Block Lock Setup to Write Enable High	70		ns	
tBLH	tQVPH	Block Lock Hold from Valid SRD	0		ns	
tDAP	tEHRH1	Duration of Auto Program Operation(Word Mode)		30	300	μs
tDAP	tEHRH1	Duration of Auto Program Operation(Byte Mode)		30	300	μs
tDAP	tEHRH1	Duration of Auto Program Operation(Page Mode)		4	80	ms
tDAE	tEHRH2	Duration of Auto Block Erase Operation		150	600	ms
tEHL	tEHL	Delay Time During Internal Operation			70	ns
tPS	tPEHL	RP# Recovery to CE# Low	150			ns

-Timing measurements are made under AC waveforms for read operations.

-Typical values at Flash VCC=3.3V and Ta=25 °C.



**M5M29KE131BTP**134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

**Program / Erase Time**

Parameter	Min.	Typ.	Max.	Units
Block Erase Time		150	600	ms
Main Block Write Time (Byte Mode)		2	8	sec
Main Block Write Time (Word Mode)		1	4	sec
Page Write Time		4	80	ms
Flash to Page Buffer Time		100	150	μs

**Program Suspend / Erase Suspend Time**

Parameter	Min.	Typ.	Max.	Unit
Program Suspend Time			15	μs
Erase Suspend Time			15	μs

**Flash VCC Power Up / Down Timing**

symbol	Parameter	Min.	Typ.	Max.	Unit
tVCS	RP#=VIH Setup Time from Flash VCC min.	2			μs
tVHEL	CE#=VIL Setup Time from Flash VCC min.	60			μs

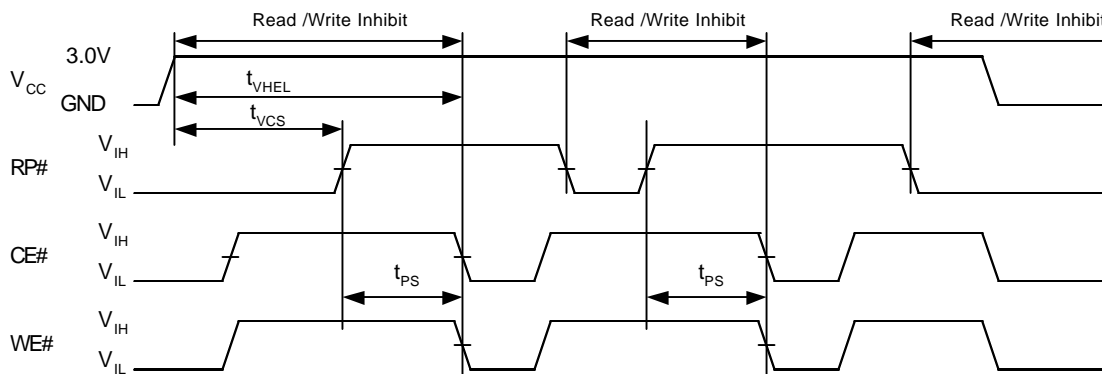
During power up / down, by the noise pulses on control pins, the device has possibility of accidental erase of programming. The device must be protected against initiation of write cycle for memory contents during power up / down. The delay time of min. 60 μsec is always required before read operation or write operation is initiated from the time Flash VCC reaches Flash VCC min. during power up /down. By holding RP#=VIL, the contents of memory is protected during Flash VCC power up / down. During power up, RP# must be held VIL for min. 2μs from the time Flash VCC reaches Flash VCC min.. During power down, RP# must be held VIL until Flash VCC reaches GND. RP# doesn't have latch mode, therefore RP# must be held VIH during read operation or erase / program operation.

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

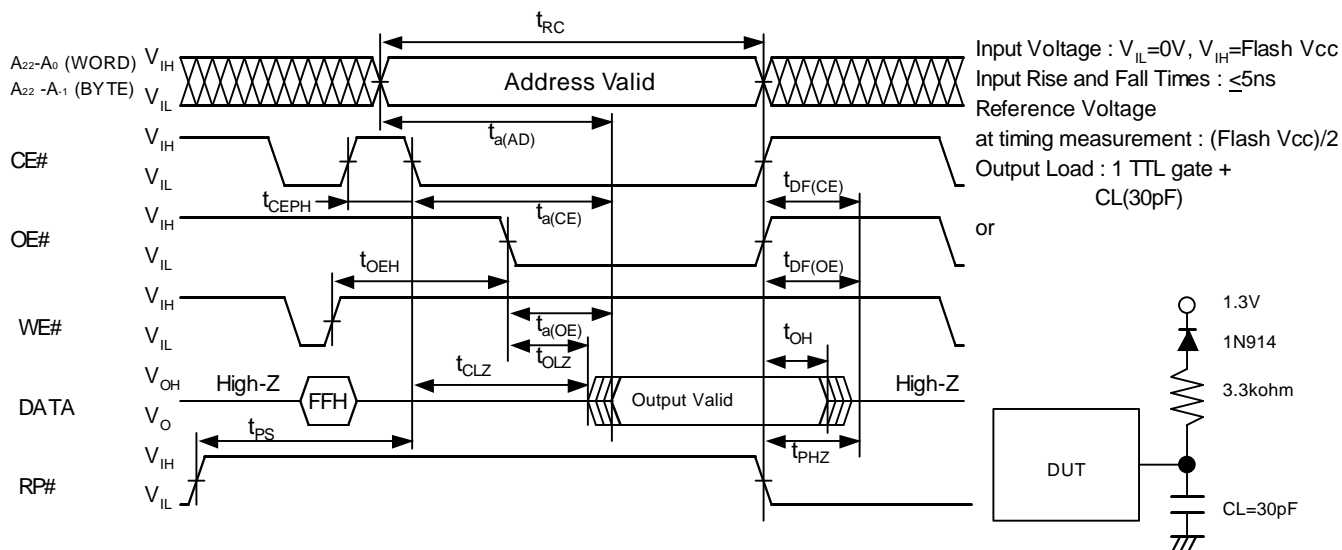
Stacked-uMCP (micro Multi Chip Package)

## Flash VCC Power up / down Timing



## AC Waveforms for Read Operation and Test Conditions

### Test Conditions for AC Characteristics



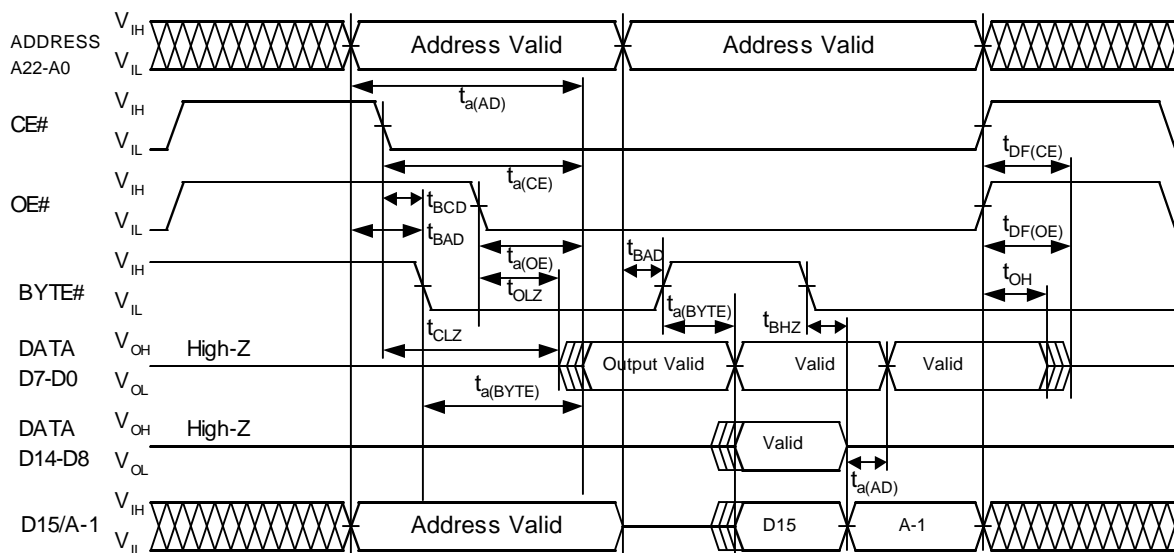
- After inputting Read Array Command FFH, it is necessary to make CE# "H" pulse more than 30ns ( $t_{CEPH}$ ). And after inputting Read Array Command FFH, it is also necessary to keep 30ns to recover before starting read after WE# rises "H" in case of changing a part or all of addresses( A22~A0/A22~A-1) and CE#="L".

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Byte AC Waveforms for Read Operation



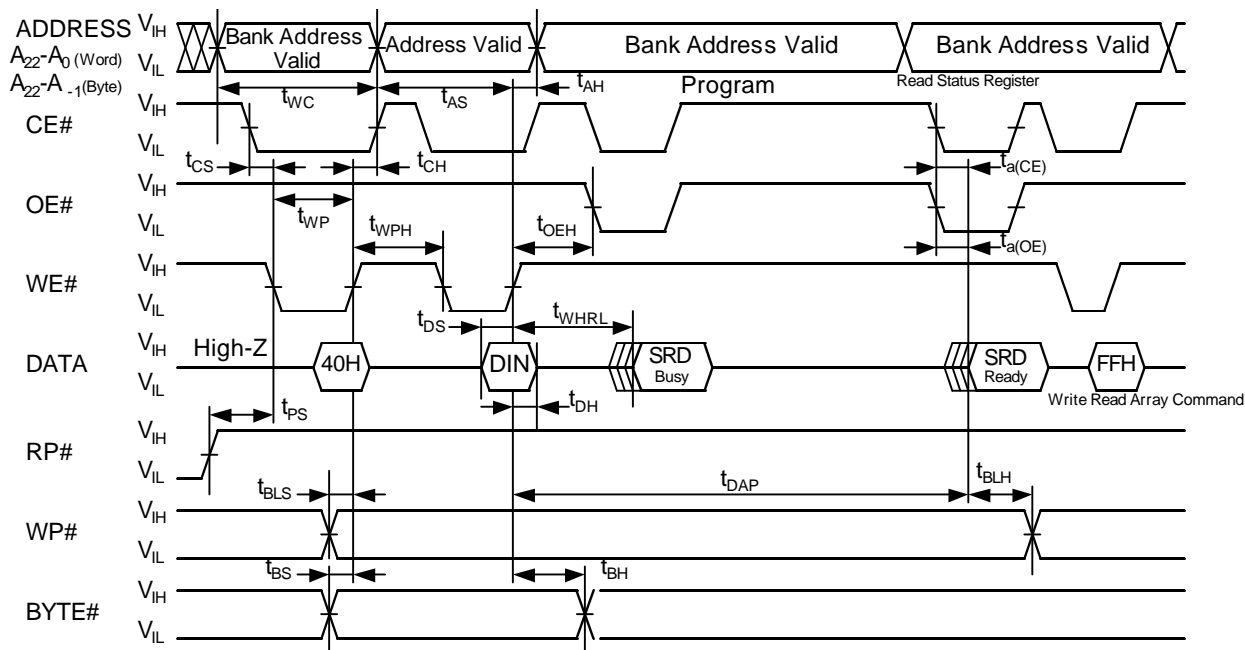
When BYTE# = VIH, CE# = OE# = VIL, D15/A-1 is output status. At this time, input signal must not be applied.

# M5M29KE131BTP

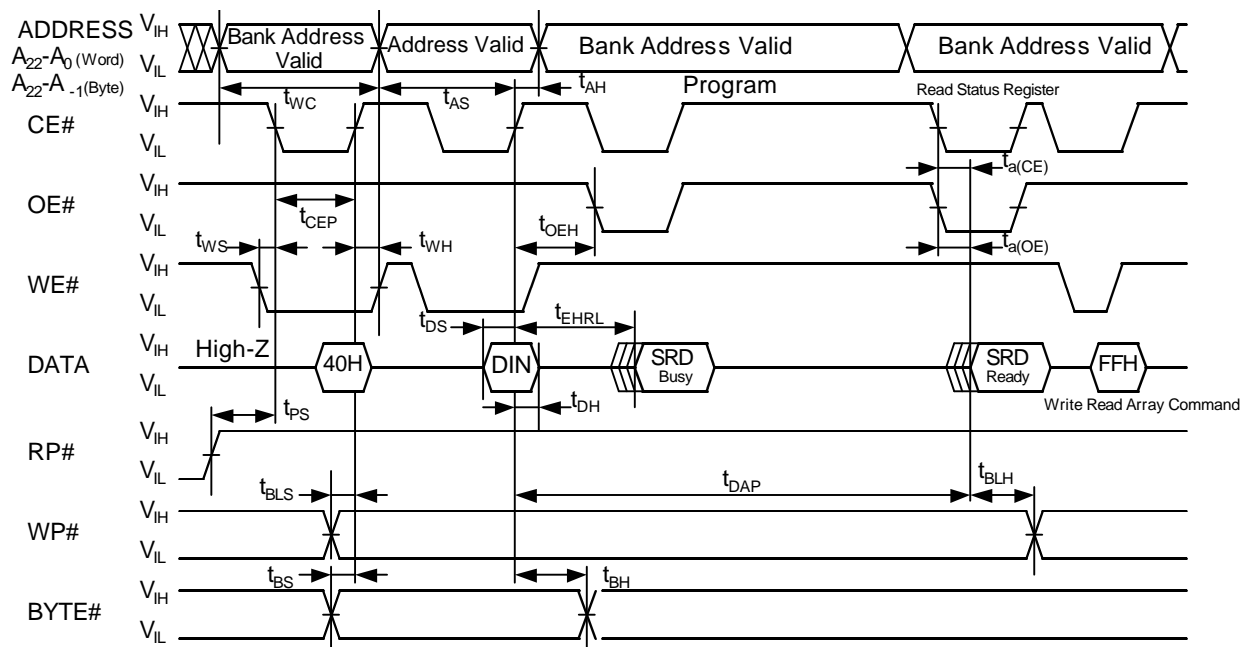
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Word / Byte Program Operation (WE# Control)



## AC Waveforms for Word / Byte Program Operation (CE# Control)

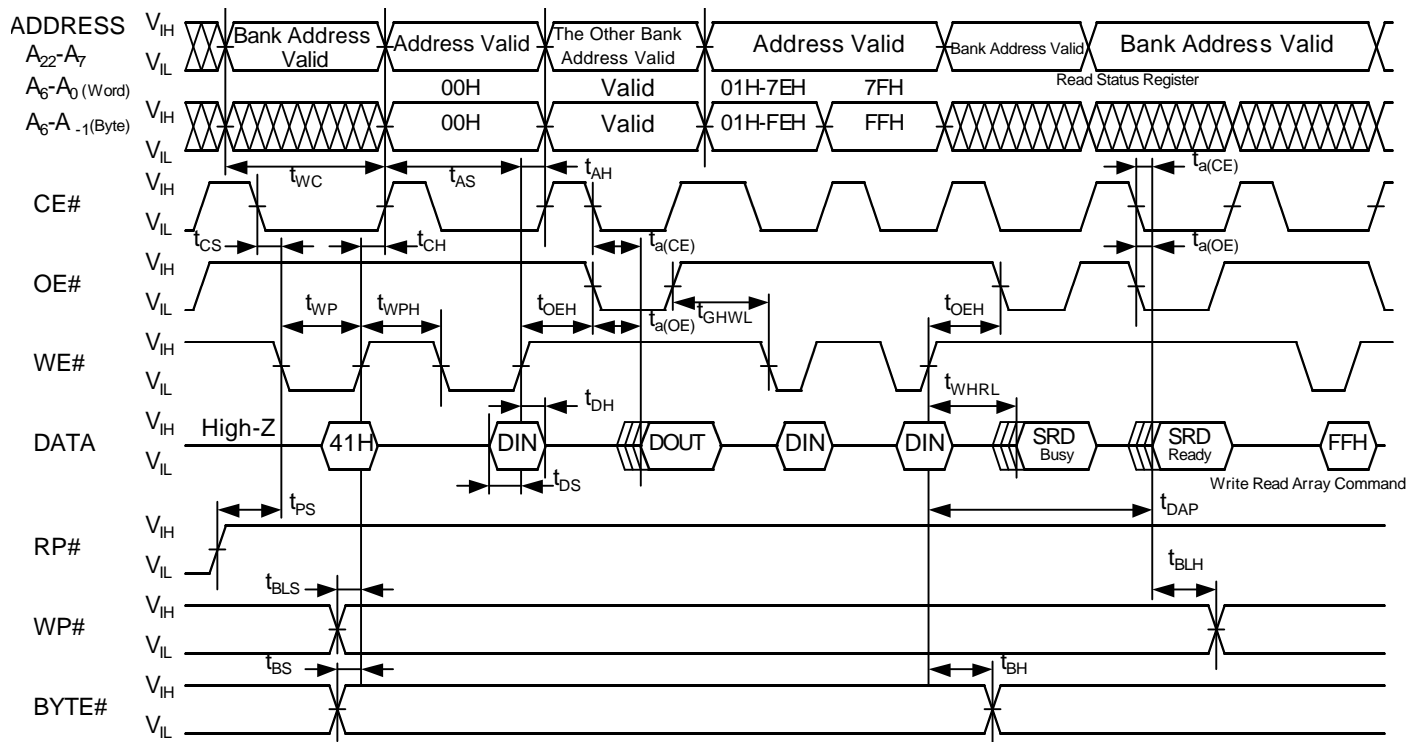


# M5M29KE131BTP

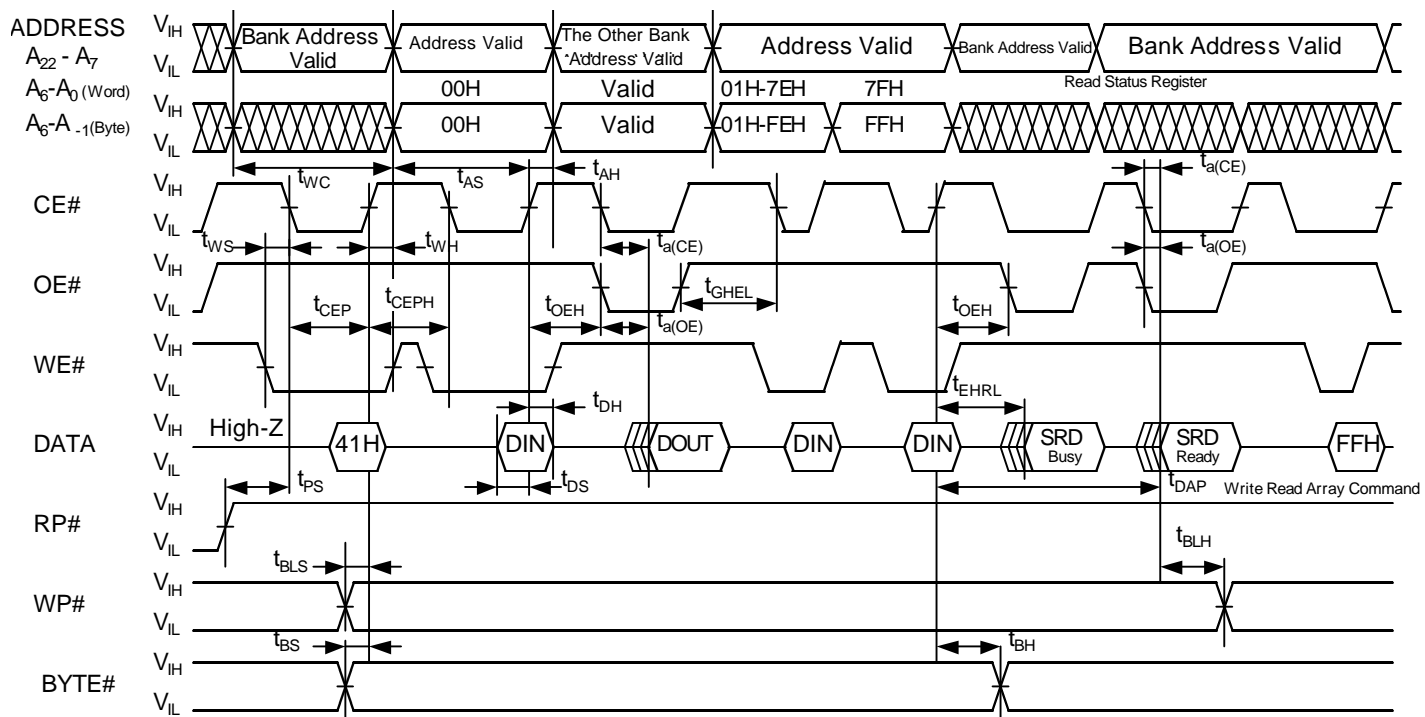
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Page Program Operation (WE# Control)



## AC Waveforms for Page Program Operation (CE# Control)

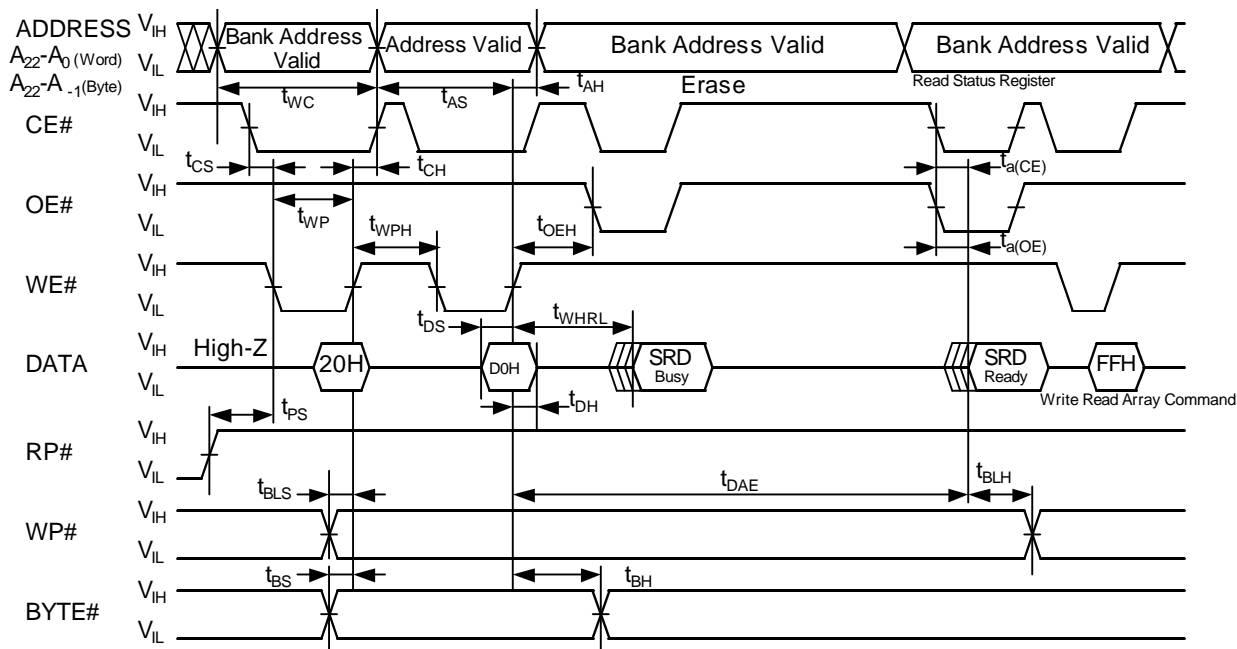


# M5M29KE131BTP

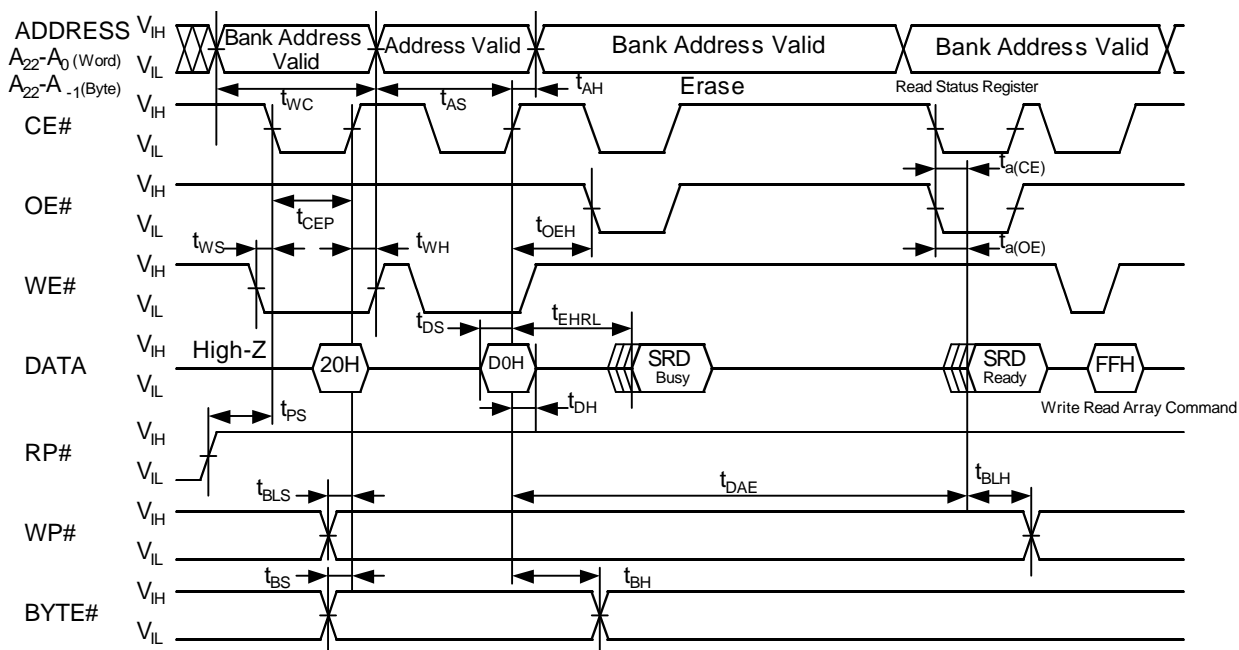
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Erase Operation (WE# Control)



## AC Waveforms for Erase Operation (CE# Control)

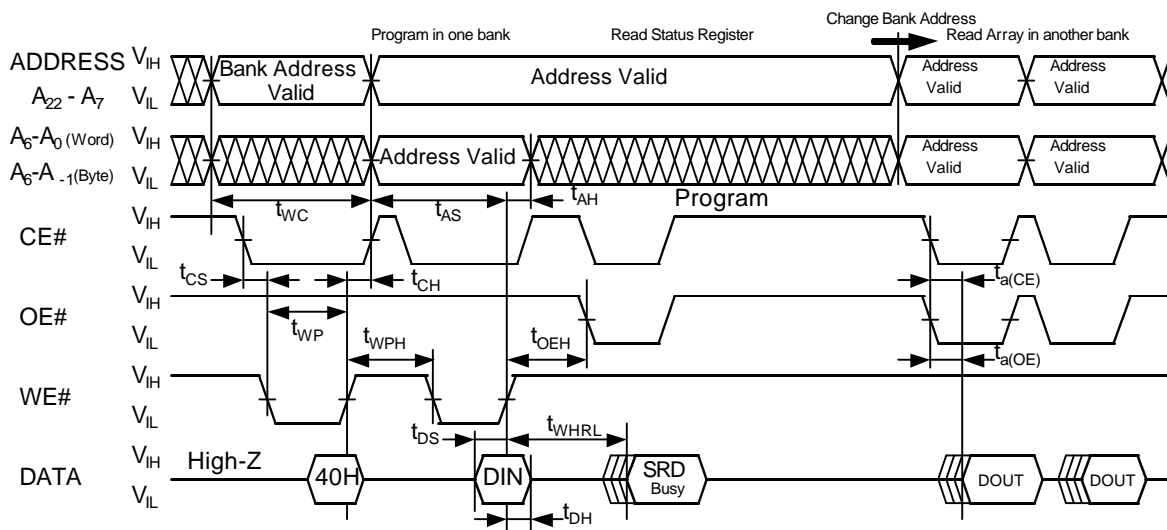


# M5M29KE131BTP

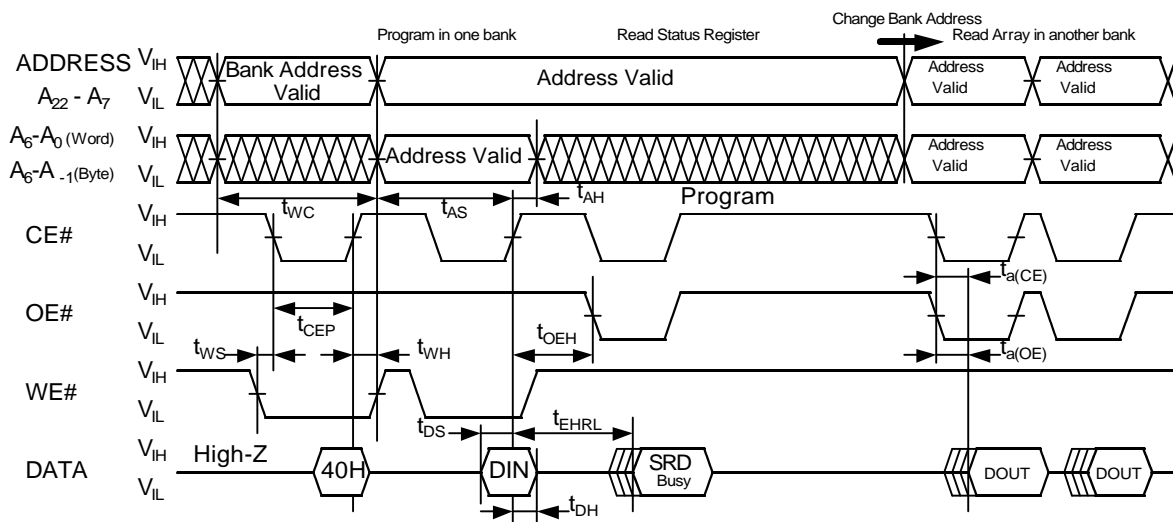
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Word / Byte Program Operation with BGO (WE# Control)



## AC Waveforms for Word / Byte Program Operation with BGO (CE# Control)

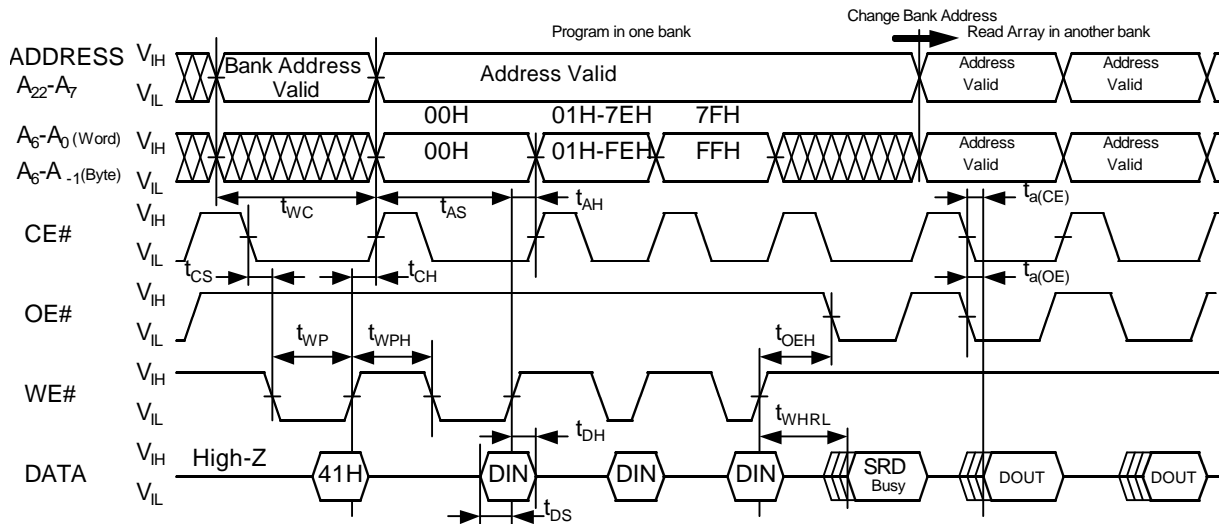


# M5M29KE131BTP

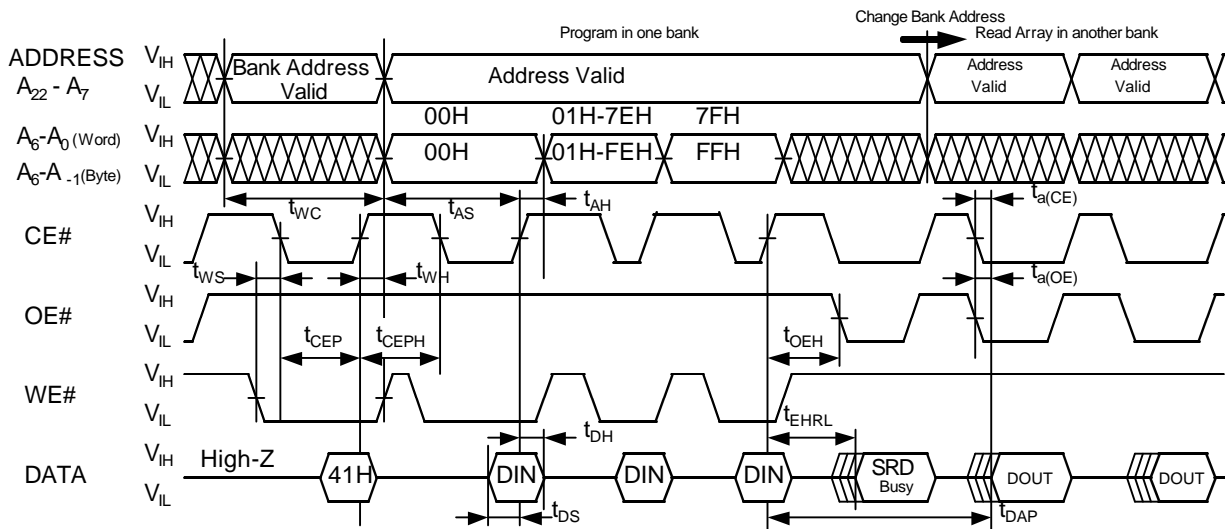
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Page Program Operation with BGO (WE# Control)



## AC Waveforms for Page Program Operation with BGO (CE# Control)



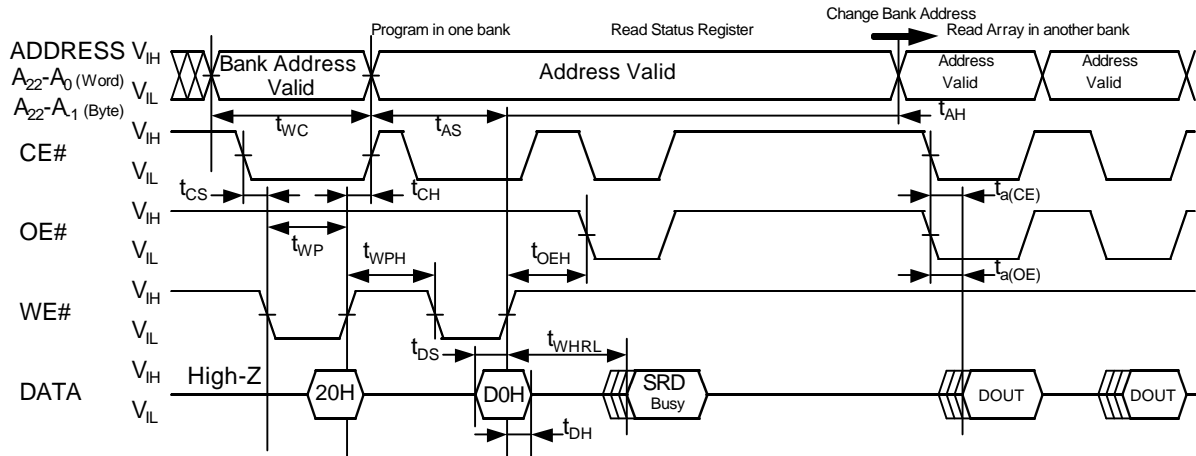


# M5M29KE131BTP

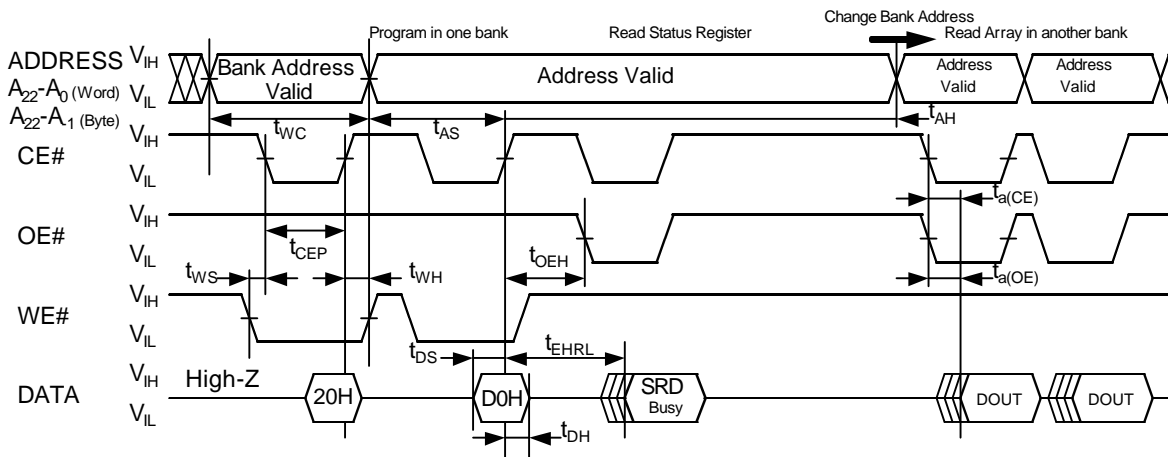
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Erase Operation with BGO (WE# Control)



## AC Waveforms for Erase Operation with BGO (CE# Control)

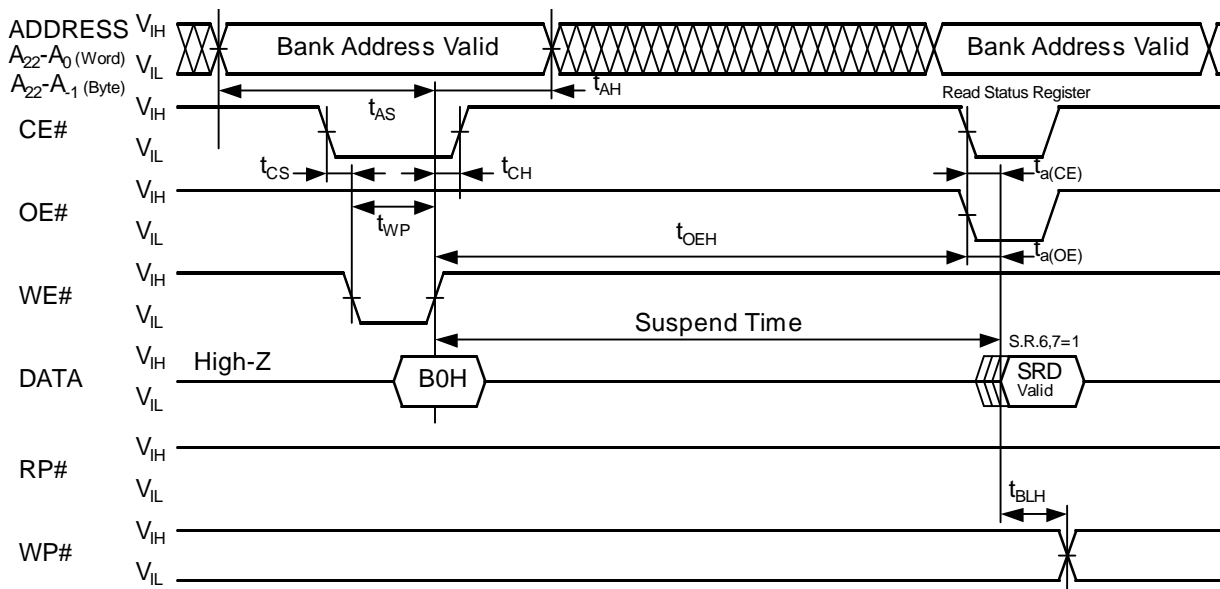


# M5M29KE131BTP

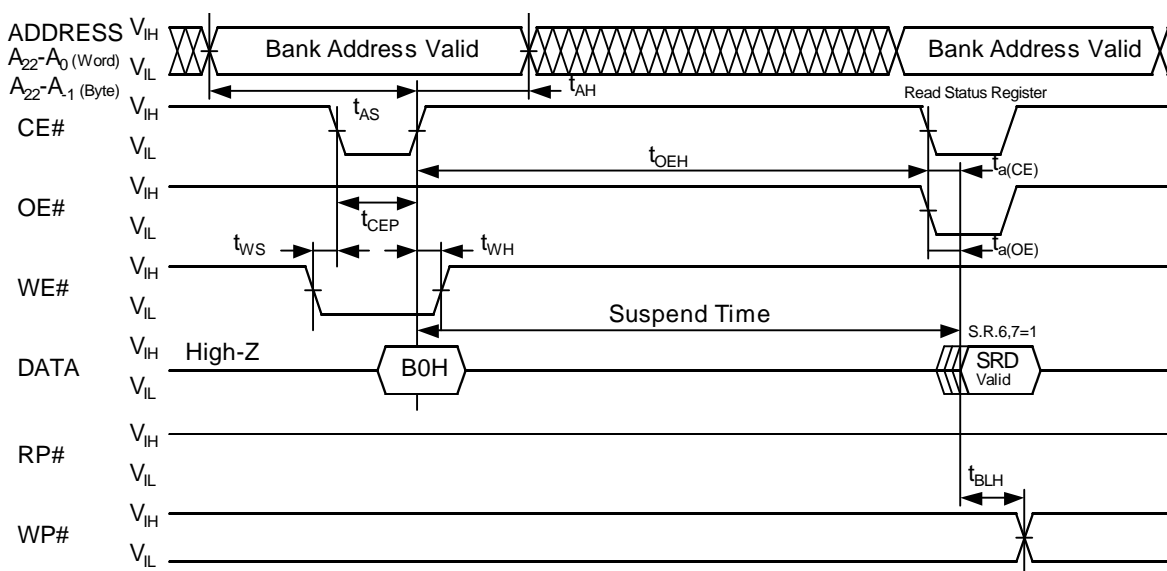
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Suspend Operation (WE# Control)



## AC Waveforms for Suspend Operation (CE# Control)

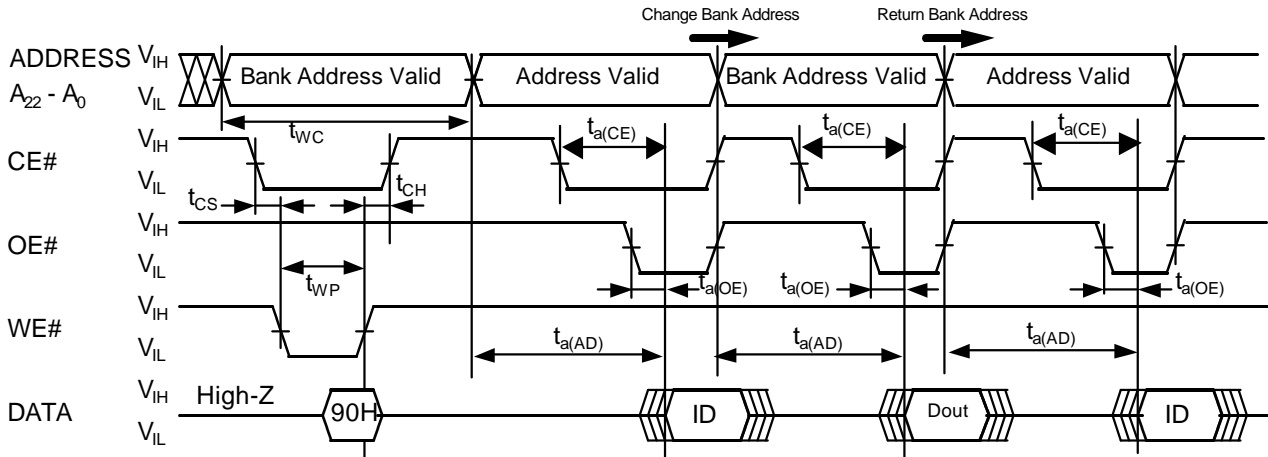


# M5M29KE131BTP

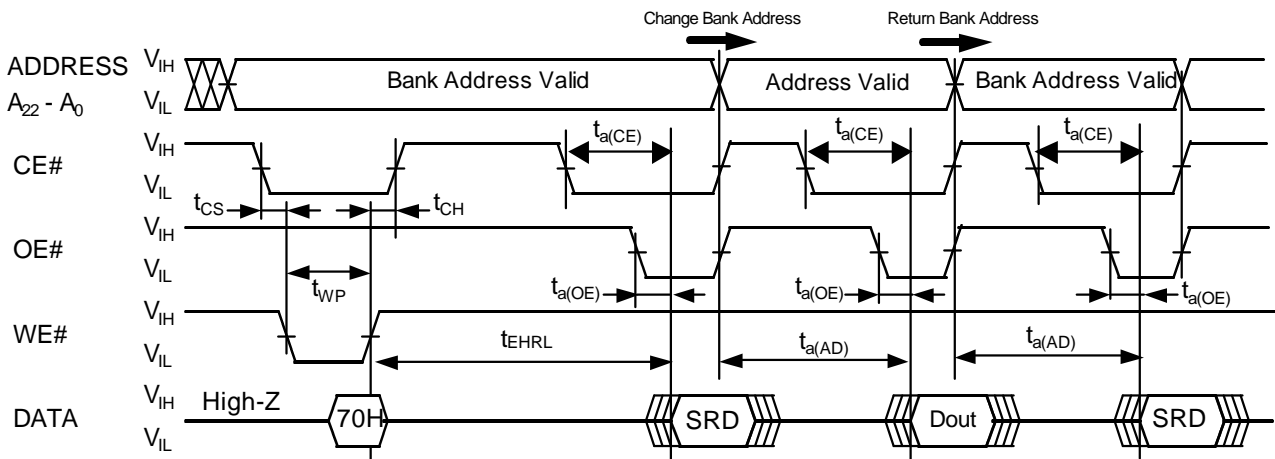
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## AC Waveforms for Device ID Read Operation with BBR(Back Bank Read)



## AC Waveforms for Status Register Read Operation with BBR(Back Bank Read)

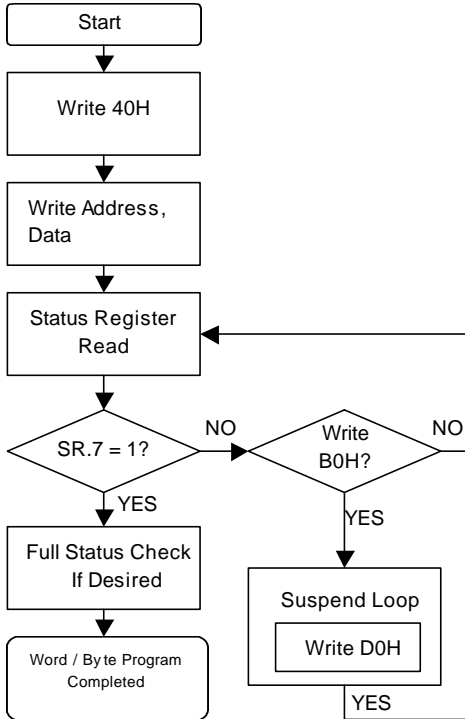


# M5M29KE131BTP

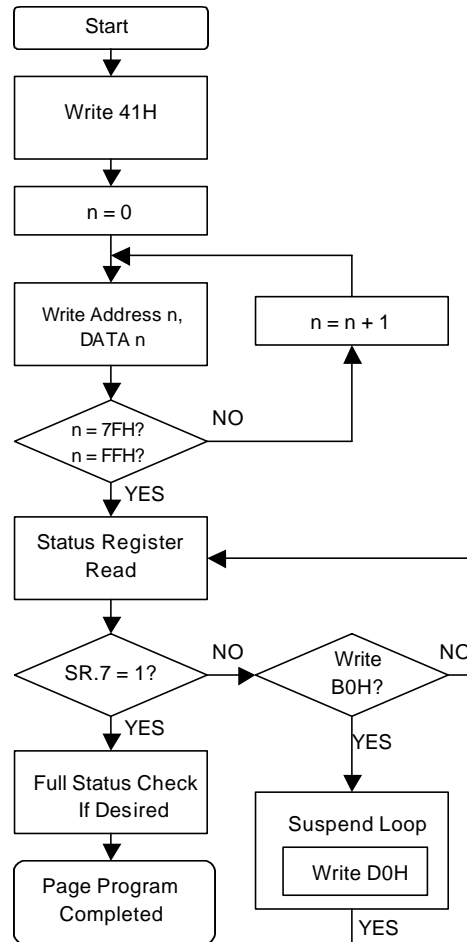
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

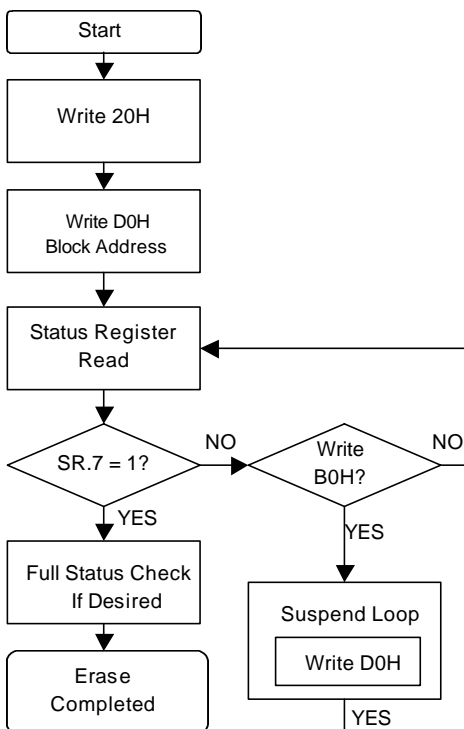
**Word / Byte Program Flow Chart**



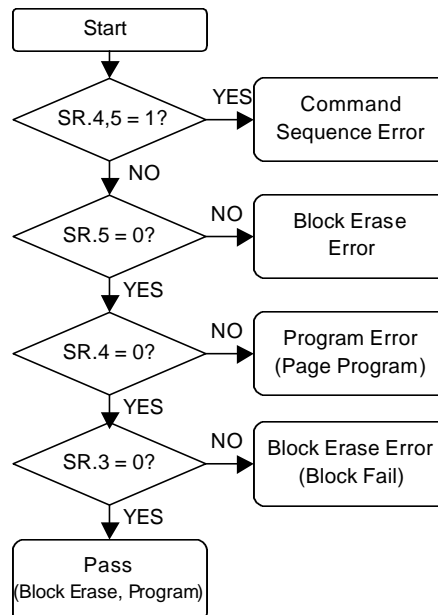
**Page Program Flow Chart**



**Block Erase Flow Chart**



**Status Register Check Flow Chart**

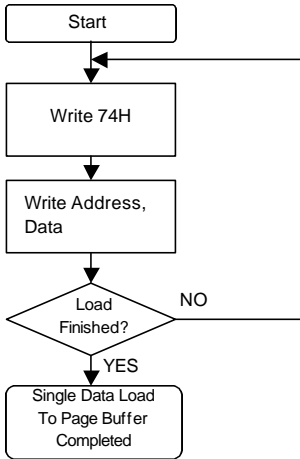


# M5M29KE131BTP

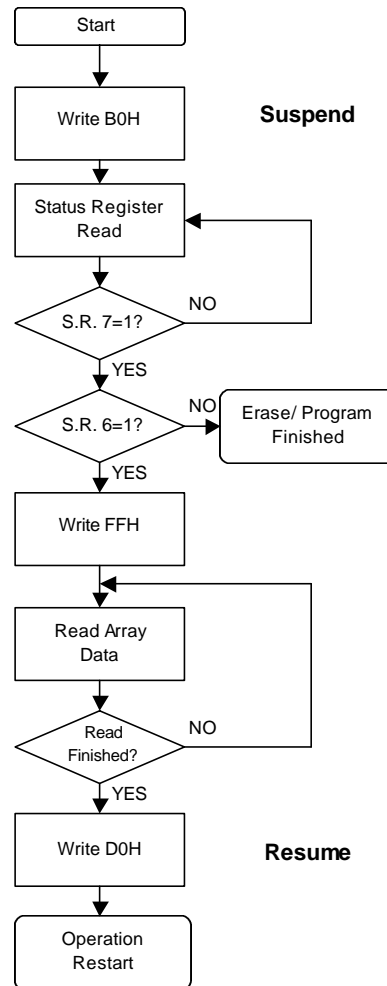
134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

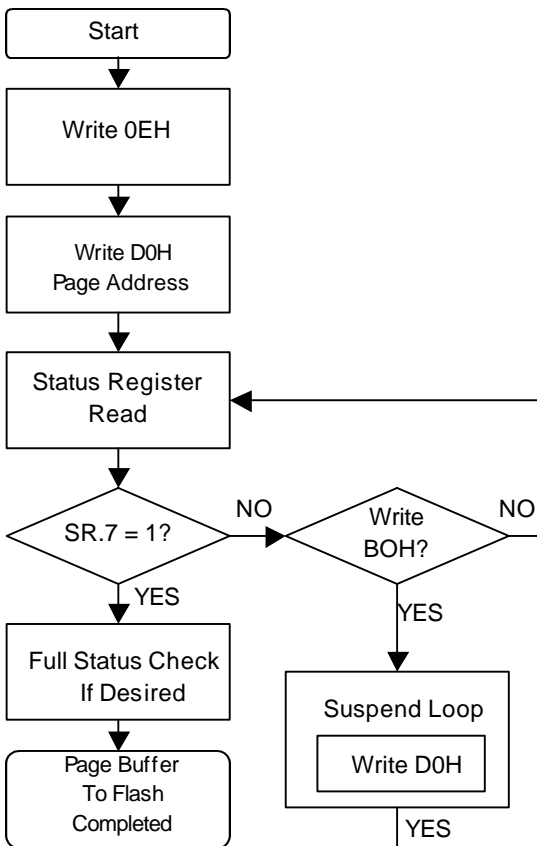
**Single Data Load to Page Buffer Flow Chart**



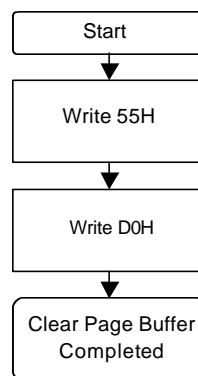
**Suspend / Resume Flow Chart**



**Page Buffer to Flash Flow Chart**



**Clear Page Buffer Flow Chart**

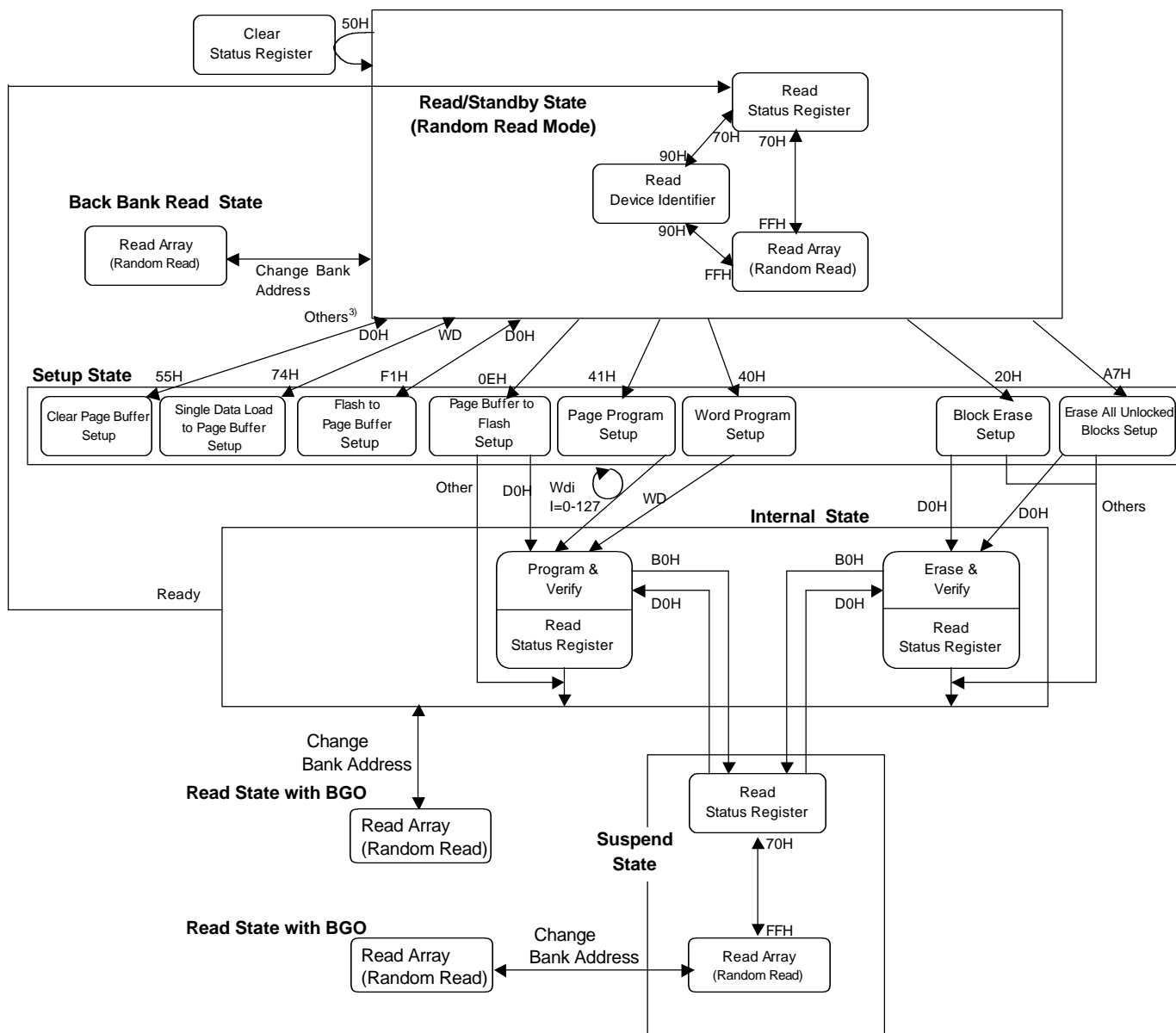


# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Operation Status (WP#=VIH)



1) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.

2) To access any bank during Erase All Unlocked Block results Status Register Read.

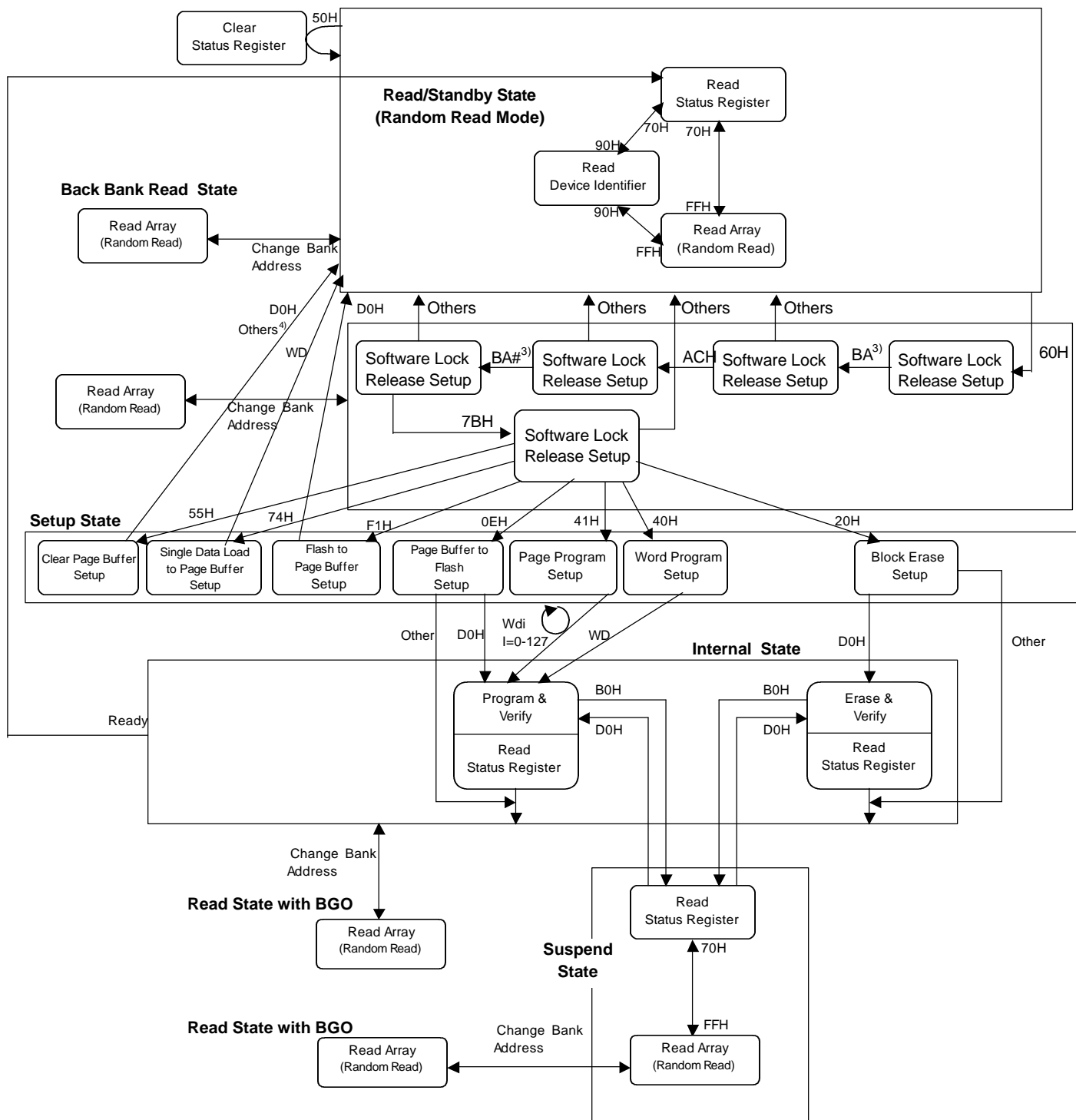
Although Read Status Register Command and Read Array Command can be issued under Suspend State, output data make no sense.

# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Operation Status (WP#=VIL)



1) BA, BA#: Block Address, Block Address# (Shown in Command List(WP#=VIL) in detail).

2) After setting up Clear Page Buffer, D0H enables to clear Page Buffer.

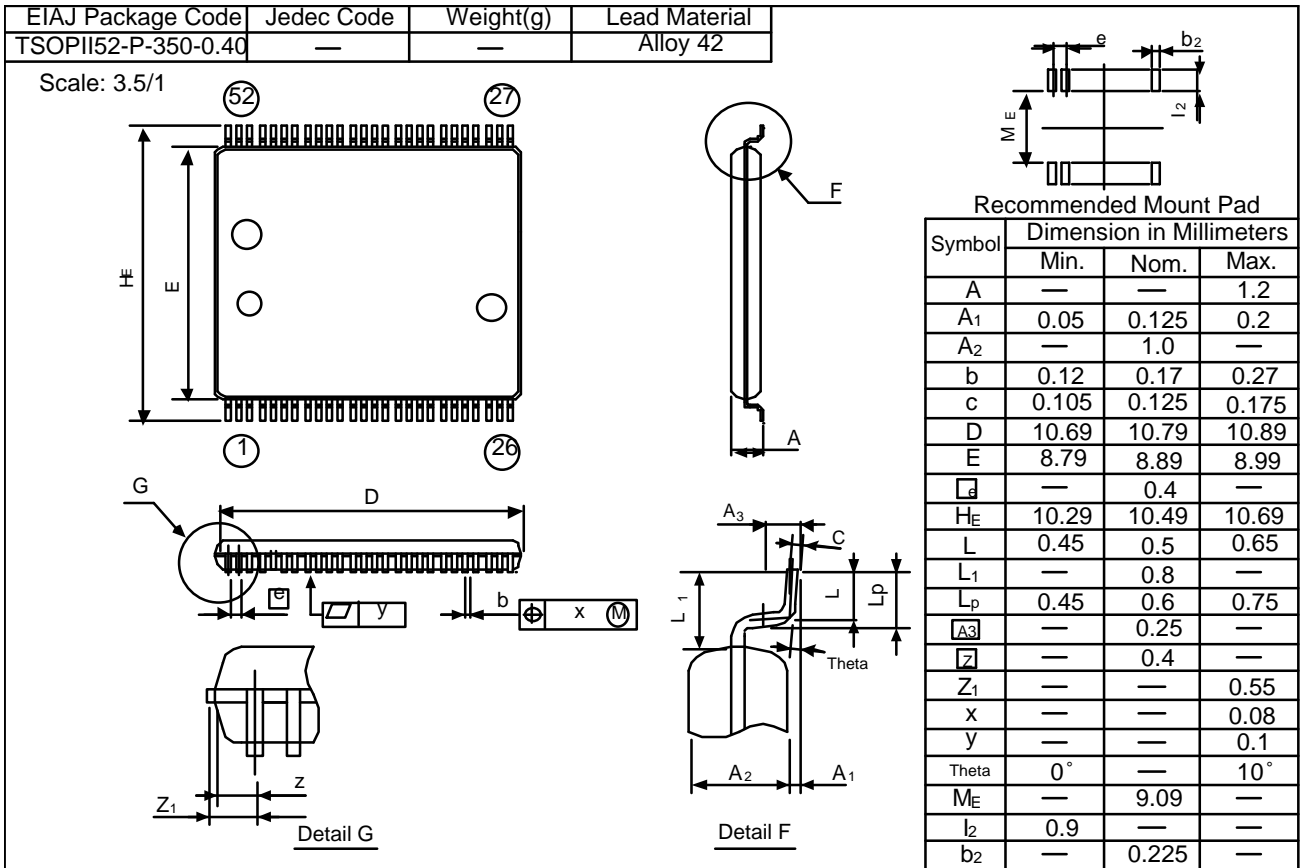
# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Package Dimension

52PTG-A





# M5M29KE131BTP

134,217,728-BIT (16,777,216-WORD BY 8-BIT / 8,388,608-WORD BY 16-BIT)  
CMOS FLASH MEMORY

Stacked-uMCP (micro Multi Chip Package)

## Renesas Technology Corp.

Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

### Keep safety first in your circuit designs!

- Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

### Notes regarding these materials

- These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
- Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
- All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein. The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors. Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
- When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
- Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
- The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
- If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
- Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
- Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.