

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

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# HAT2143H

Silicon N Channel Power MOS FET  
Power Switching

**RENESAS**

ADE-208-1584A (Z)

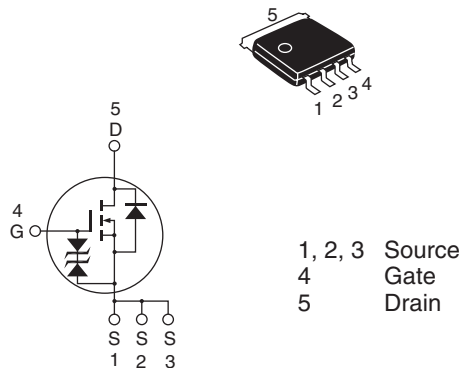
Preliminary  
2nd. Edition  
Aug. 2002

## Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 4.9 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )

## Outline

LFPAK



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	30	V
Gate to source voltage	$V_{GSS}$	± 20	V
Drain current	$I_D$	40	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	160	A
Body-drain diode reverse drain current	$I_{DR}$	40	A
Avalanche current	$I_{AP}$ <sup>Note 3</sup>	16	A
Avalanche energy	$E_{AR}$ <sup>Note 3</sup>	25	mJ
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	20	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	- 55 to + 150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2.  $T_c = 25^\circ C$

3. Value at Tch = 25°C,  $R_g \geq 50 \Omega$

## Electrical Characteristics

(Ta = 25°C)

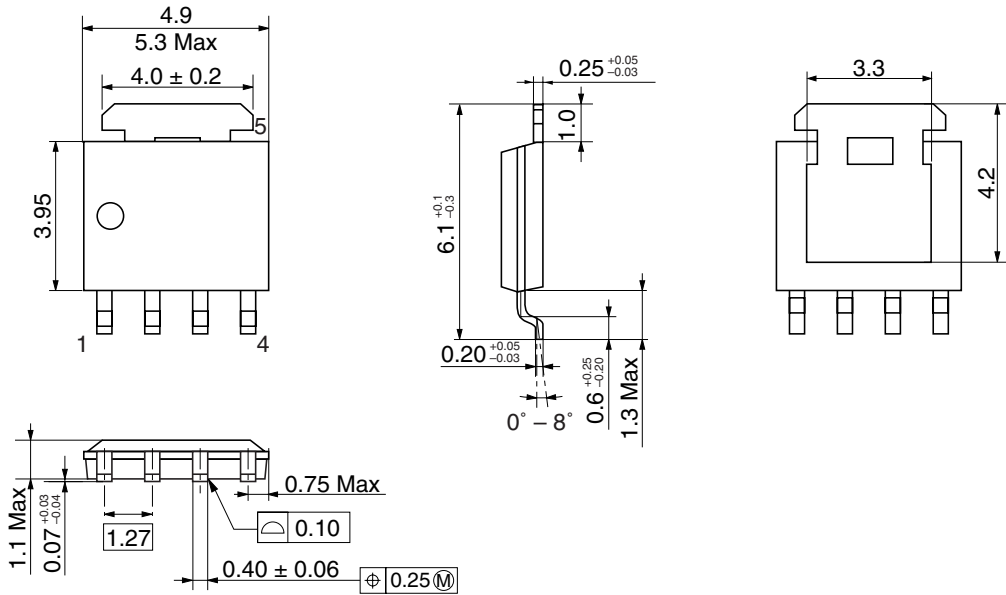
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.9	6.1	$\text{m}\Omega$	$I_D = 20 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	7.9	11.5	$\text{m}\Omega$	$I_D = 20 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	30	50	—	S	$I_D = 20 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	Ciss	—	2450	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	540	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	280	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	40	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Qgs	—	8	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	7	—	nc	$I_D = 40 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$
Rise time	$t_r$	—	56	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	76	—	ns	$R_L = 0.5 \text{ }\Omega$
Fall time	$t_f$	—	15	—	ns	$R_g = 4.7 \text{ }\Omega$
Body–drain diode forward voltage	$V_{DF}$	—	0.85	1.11	V	$I_F = 40 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body–drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = 40 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

# HAT2143H

## Package Dimensions

As of January, 2002  
Unit: mm



Hitachi Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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