

PowerMOS transistor Logic level TOPFET

BUK106-50L/S
BUK106-50LP/SP

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving

- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	50	A
P_{tot}	Total power dissipation	125	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance		
	$V_{IS} = 5\text{ V}$	35	mΩ
	$V_{IS} = 8\text{ V}$	28	mΩ
SYMBOL	PARAMETER	NOM.	UNIT
V_{PSN}	Protection supply voltage		
	BUK106-50L	5	V
	BUK106-50S	10	V

FUNCTIONAL BLOCK DIAGRAM

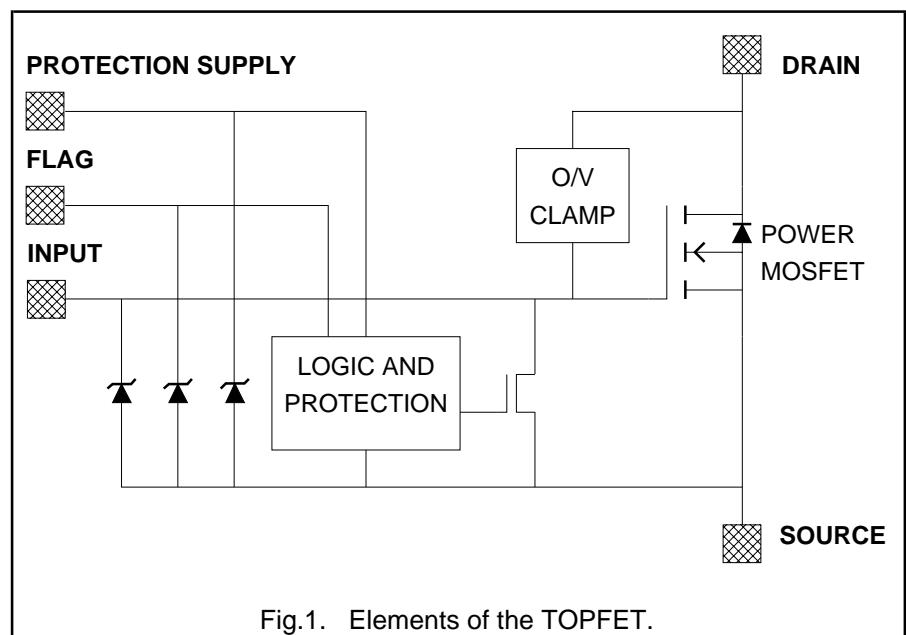
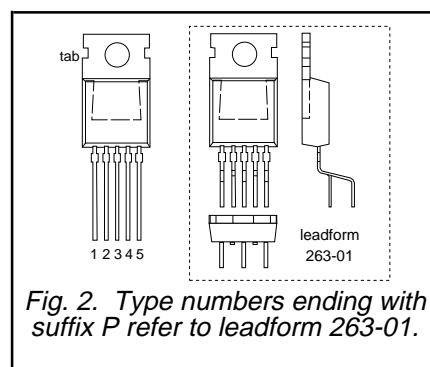


Fig.1. Elements of the TOPFET.

PINNING - SOT263

PIN	DESCRIPTION
1	input
2	flag
3	drain
4	protection supply
5	source
tab	drain

PIN CONFIGURATION



SYMBOL

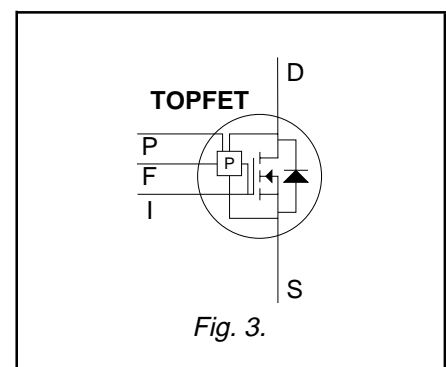


Fig. 3.

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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Voltages Continuous off-state drain source voltage ¹	$V_{IS} = 0\text{ V}$	-	50	V
V_{IS}	Continuous input voltage	-	0	11	V
V_{FS}	Continuous flag voltage	-	0	11	V
V_{PS}	Continuous supply voltage	-	0	11	V
	Currents	$V_{IS} =$	-	8	5
I_D	Continuous drain current	$T_{mb} \leq 25\text{ °C}$	-	50	45
I_D	Continuous drain current	$T_{mb} \leq 100\text{ °C}$	-	31	28
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25\text{ °C}$	-	200	180
P_{tot}	Thermal Total power dissipation	$T_{mb} = 25\text{ °C}$	-	125	W
T_{stg}	Storage temperature	-	-55	150	°C
T_j	Junction temperature ²	continuous	-	150	°C
T_{sold}	Lead temperature	during soldering	-	250	°C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{PSP}	Protection supply voltage ³	$V_{IS} =$ for valid protection	8	5	-
		BUK106-50L	4.4	4	-
		BUK106-50S	5.4	5	-
$V_{DDP(T)}$	Over temperature protection Protected drain source supply voltage	$V_{PS} = V_{PSN}$ $V_{IS} = 10\text{ V}; R_I \geq 2\text{ k}\Omega$ $V_{IS} = 5\text{ V}; R_I \geq 1\text{ k}\Omega$	-	50	V
$V_{DDP(P)}$	Short circuit load protection Protected drain source supply voltage ⁴	$V_{PS} = V_{PSN}; L \leq 10\text{ }\mu\text{H}$ $V_{IS} = 10\text{ V}; R_I \geq 2\text{ k}\Omega$ $V_{IS} = 5\text{ V}; R_I \geq 1\text{ k}\Omega$	-	24	V
P_{DSM}	Instantaneous overload dissipation		-	4	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; $C = 250\text{ pF}; R = 1.5\text{ k}\Omega$	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

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OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100 \Omega^1$	-	50	A
E_{DSM}	Non-repetitive inductive turn-off energy ²	$I_{DM} = 27 \text{ A}; R_{IS} \geq 100 \Omega$	-	1	J
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100 \Omega; T_{mb} \leq 85 \text{ }^\circ\text{C};$ $I_{DM} = 16 \text{ A}; V_{DD} \leq 20 \text{ V};$ $f = 250 \text{ Hz}$	-	80	mJ
I_{DIRM}	Repetitive peak drain to input current ³	$R_{IS} = 0 \Omega; t_p \leq 1 \text{ ms}$	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} = 25 \text{ }^\circ\text{C};$ $V_{IS} = V_{PS} = V_{FS} = 0 \text{ V}$	-	50	A

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance Junction to mounting base	-	-	0.8	1.0	K/W
$R_{th\ j-a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS
 $T_{mb} = 25 \text{ }^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100 \Omega; I_D = 10 \text{ mA}$	50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100 \Omega; I_{DM} = 1 \text{ A}; t_p \leq 300 \mu\text{s};$ $\delta \leq 0.01$	50	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12 \text{ V}; V_{IS} = 0 \text{ V}$	-	0.5	10	μA
I_{DSR}	Drain source leakage current	$V_{DS} = 50 \text{ V}; R_{IS} = 100 \Omega;$	-	1	20	μA
I_{DSR}	Drain source leakage current	$V_{DS} = 40 \text{ V}; R_{IS} = 100 \Omega;$ $T_j = 125 \text{ }^\circ\text{C}$	-	10	100	μA
$R_{DS(ON)}$	Drain-source on-state resistance	$I_{DM} = 25 \text{ A};$ $t_p \leq 300 \mu\text{s}; \delta \leq 0.01$	-	22	28	$\text{m}\Omega$
		$V_{IS} = 8 \text{ V}$ $V_{IS} = 5 \text{ V}$	-	28	35	$\text{m}\Omega$

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

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OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$E_{DS(TO)}$	Short circuit load protection¹ Overload threshold energy Response time	$V_{PS} = V_{PSN}^2$; $T_{mb} = 25\text{ °C}$; $L \leq 10\ \mu\text{H}$ $V_{DD} = 13\text{ V}$; $V_{IS} = 10\text{ V}$ $V_{DD} = 13\text{ V}$; $V_{IS} = 10\text{ V}$	-	550	-	mJ
$t_{d\ sc}$			-	0.4	-	ms
$T_{j(TO)}$	Over temperature protection Threshold junction temperature	$V_{PS} = V_{PSN}$ from $I_D \geq 2.5\text{ A}^3$	150	-	-	°C

TRANSFER CHARACTERISTICS

$T_{mb} = 25\text{ °C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 12\text{ V}$; $I_{DM} = 25\text{ A}$ $t_p \leq 300\ \mu\text{s}$; $\delta \leq 0.01$	17	28	-	S
I_D	Drain current ⁴	$V_{DS} = 13\text{ V}$; $V_{IS} = 5\text{ V}$ $V_{IS} = 10\text{ V}$	-	80 160	- -	A A

PROTECTION SUPPLY CHARACTERISTICS

$T_{mb} = 25\text{ °C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
I_{PS} , I_{PSL}	Protection supply Protection supply current	normal operation or protection latched BUK106-50L BUK106-50S	-	$V_{PS} = 5\text{ V}$	0.2	0.35	mA
V_{PSR}				$V_{PS} = 10\text{ V}$	0.4	1.0	mA
	Protection reset voltage ⁵	$T_j = 150\text{ °C}$	1.5	2.5	3.5	V	
$V_{(CL)PS}$	Protection clamp voltage	$I_p = 1.35\text{ mA}$	1.0	-	-	V	
			11	13	-	V	

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25\text{ °C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	$I_S = 20\text{ A}$; $V_{IS} = V_{PS} = V_{FS} = 0\text{ V}$; $t_p = 300\ \mu\text{s}$	-	0.9	1.2	V
t_{rr}	Reverse recovery time	not applicable ⁶	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM} , which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

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INPUT CHARACTERISTICS

$T_{mb} = 25\text{ °C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(To)}$	Normal operation Input threshold voltage	$V_{DS} = 5\text{ V}; I_D = 1\text{ mA}$ $T_{mb} = 150\text{ °C}$	1.0 0.5	1.5 -	2.0 -	V V
I_{IS}	Input current	$V_{IS} = 10\text{ V}$	-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	$I_I = 1\text{ mA}$	11	13	-	V
R_{ISL}	Overload protection latched Input resistance ¹	$V_{PS} = 5\text{ V}$ $I_I = 5\text{ mA};$ $T_{mb} = 150\text{ °C}$ $V_{PS} = 10\text{ V}$ $I_I = 5\text{ mA};$ $T_{mb} = 150\text{ °C}$	- - -	55 95 35 60	- - - -	Ω Ω Ω Ω
R_{IS}	Application information External input resistances for internal overvoltage clamping ²	(see figure 29) $R_I = \infty\ \Omega;$ $V_{DS} > 30\text{ V}$	100	-	-	Ω
R_I	internal overload protection ³	$R_{IS} = \infty\ \Omega;$ $V_{II} = 5\text{ V}$ $V_{II} = 10\text{ V}$	1 2	- -	- -	k Ω k Ω

SWITCHING CHARACTERISTICS

$T_{mb} = 25\text{ °C}; R_I = 50\ \Omega; R_{IS} = 50\ \Omega$ (see figure 29); resistive load $R_L = 10\ \Omega$. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 15\text{ V}; V_{IS}: 0\text{ V} \Rightarrow 10\text{ V}$	-	10	-	ns
t_r	Rise time		-	35	-	ns
$t_{d\ off}$	Turn-off delay time	$V_{DD} = 15\text{ V}; V_{IS}: 10\text{ V} \Rightarrow 0\text{ V}$	-	280	-	ns
t_f	Fall time		-	120	-	ns

CAPACITANCES

$T_{mb} = 25\text{ °C}; f = 1\text{ MHz}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{ISS}	Input capacitance	$V_{DS} = 25\text{ V}; V_{IS} = 0\text{ V}$	-	1250	1800	pF
C_{OSS}	Output capacitance	$V_{DS} = 25\text{ V}; V_{IS} = 0\text{ V}$	-	650	1000	pF
C_{RSS}	Reverse transfer capacitance	$V_{DS} = 25\text{ V}; V_{IS} = 0\text{ V}$	-	150	250	pF
C_{PSO}	Protection supply pin capacitance	$V_{PS} = 10\text{ V}$	-	30	-	pF
C_{FSO}	Flag pin capacitance	$V_{FS} = 10\text{ V}; V_{PS} = 0\text{ V}$	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.

The external drive circuit should be such that the input voltage does not exceed $V_{IS(To)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I , an external overload protection strategy is possible using the flag pin to 'tell' the control circuit to switch off the input.

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FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor¹. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy² for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

$T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{FS} I_{FSS}	Flag 'low' Flag voltage Flag saturation current	normal operation $I_F = 1.6\text{ mA}$ $V_{FS} = 10\text{ V}$	-	0.15 15	0.4 -	V mA
I_{FS} V_{PSF}	Flag 'high' Flag leakage current Protection supply threshold voltage	overload or fault $V_{FS} = 10\text{ V}$ $V_{FF} = 5\text{ V}$; $R_F = 3\text{ k}\Omega$; BUK106-50L BUK106-50S	-	-	10	μA V V
$V_{(CL)FS}$	Flag clamping voltage	$I_F = 1\text{ mA}$; $V_{PS} = 0\text{ V}$	11	13	-	V
R_F	Application information Suitable external pull-up resistance	$V_{FF} = 5\text{ V}$ $V_{FF} = 10\text{ V}$	1 2	10 20	50 100	k Ω k Ω

ENVELOPE CHARACTERISTICS

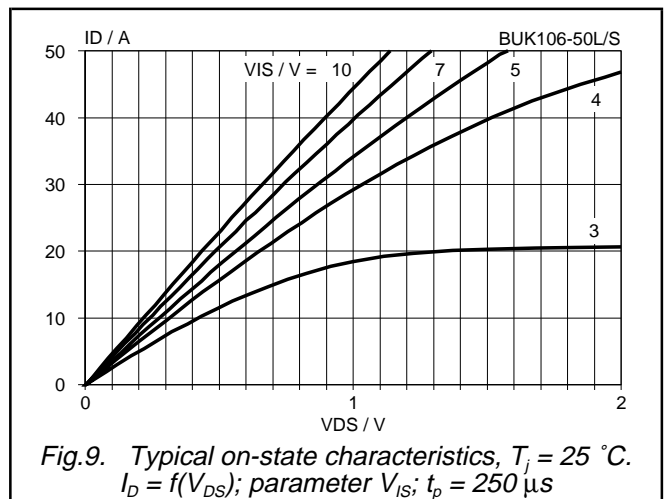
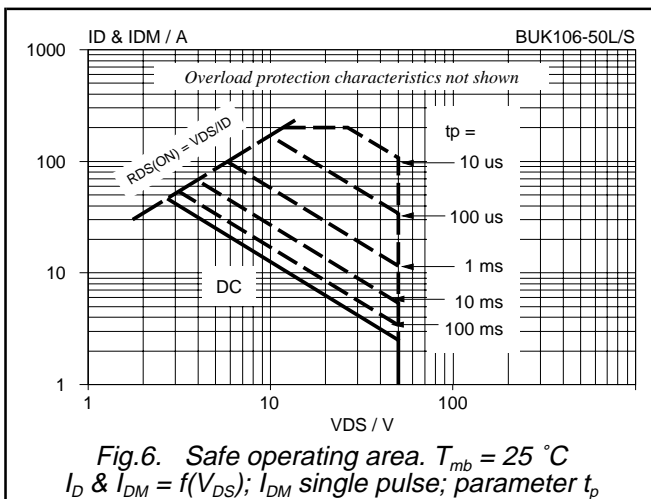
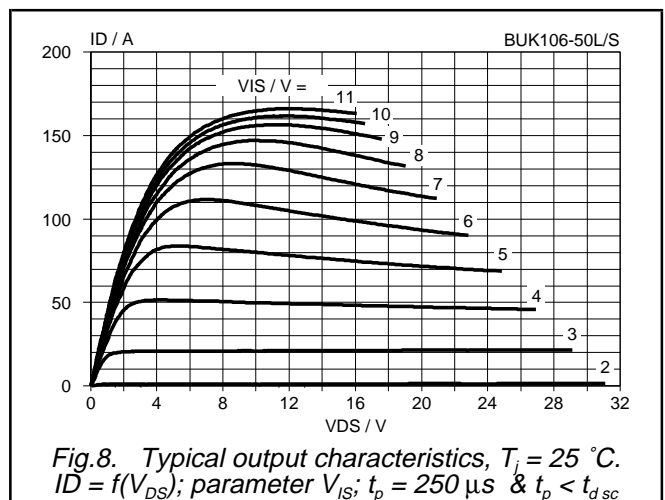
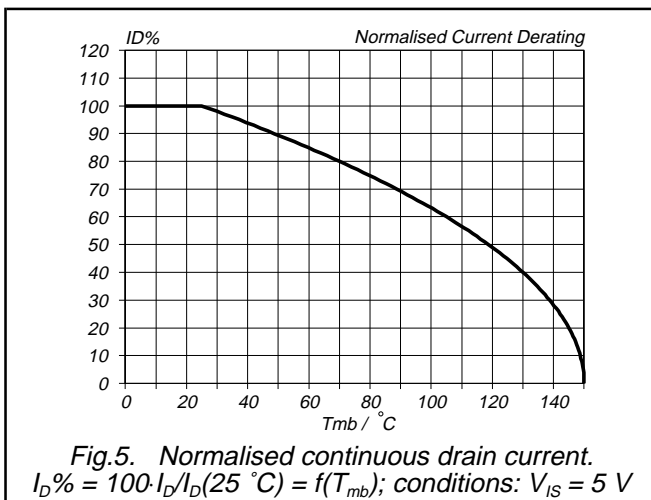
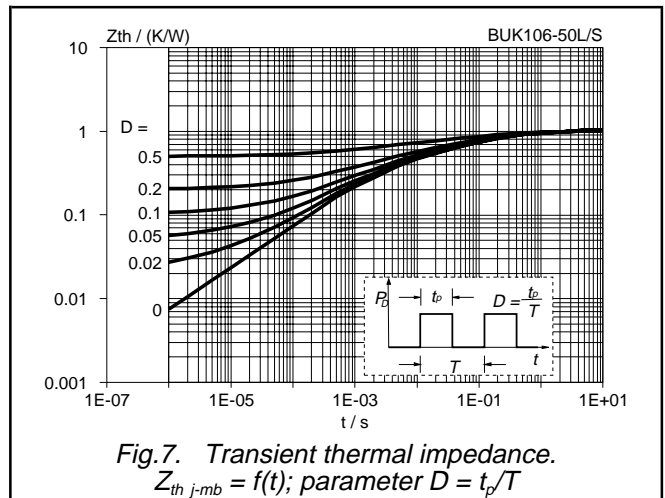
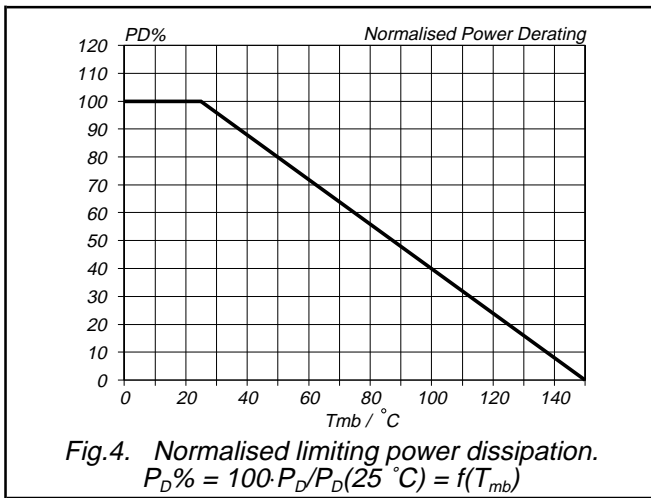
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

¹ Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

² Low pass filtering of the flag signal may be advisable to prevent false tripping.

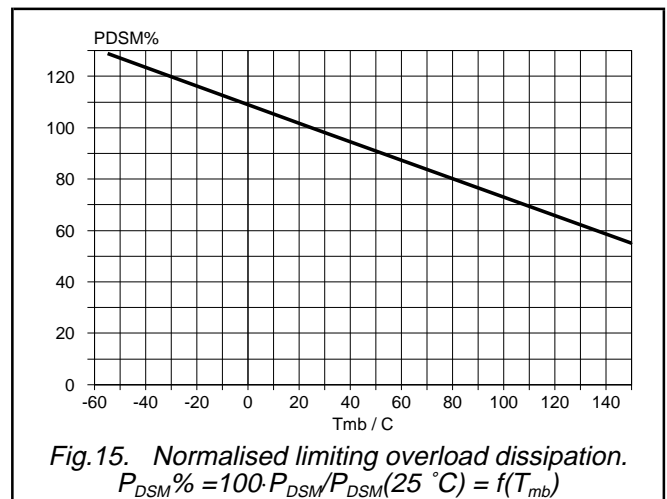
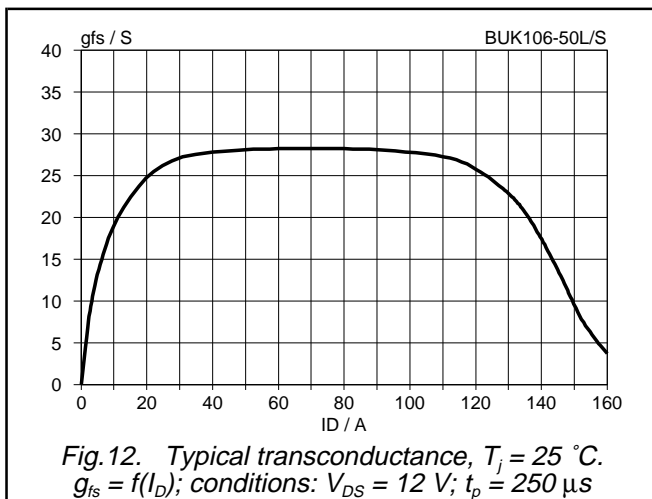
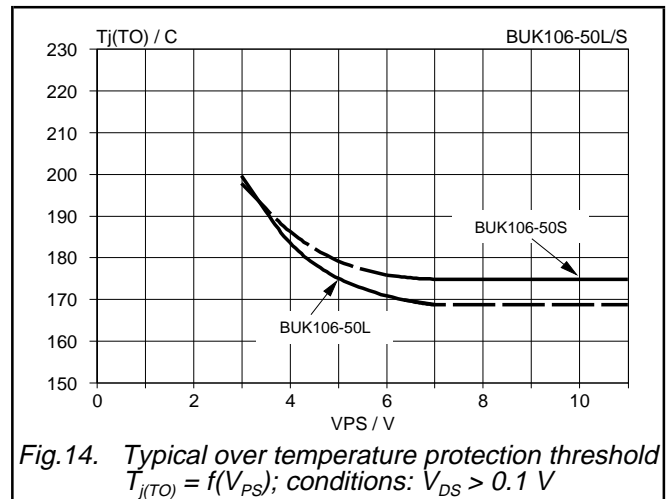
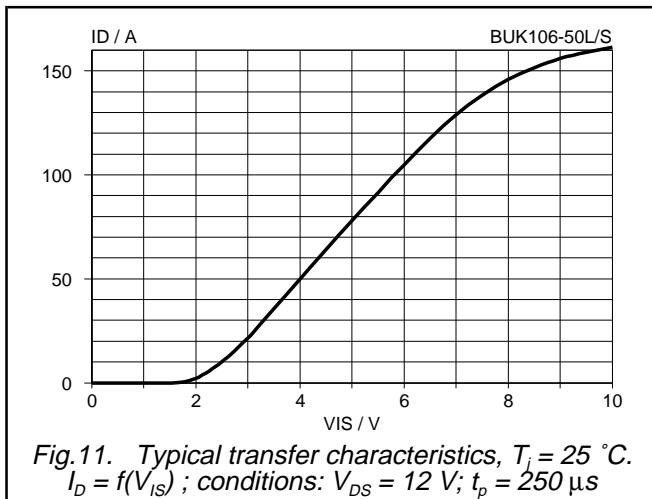
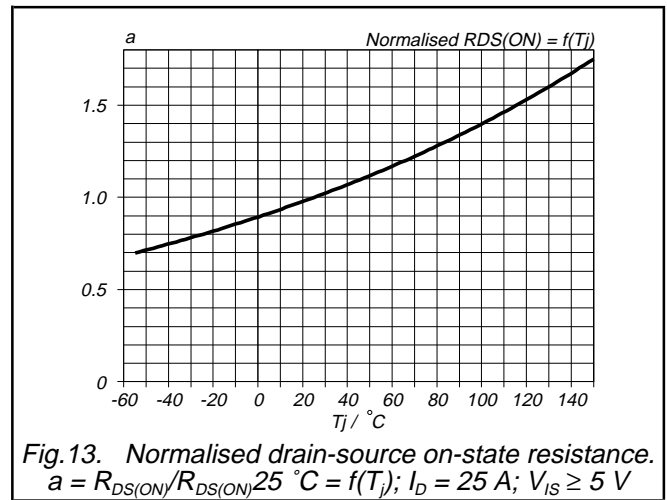
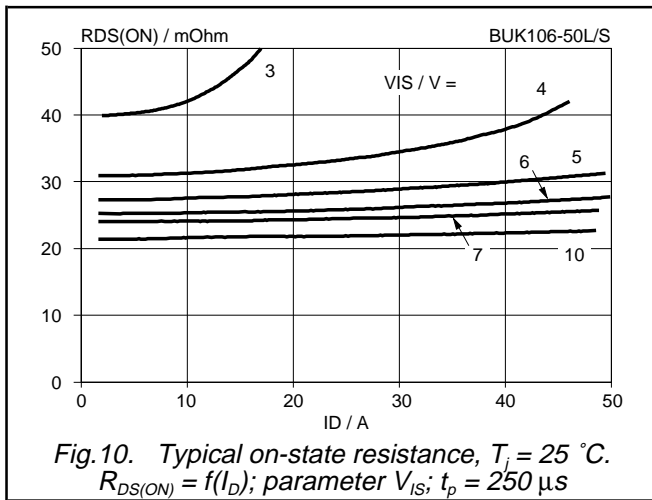
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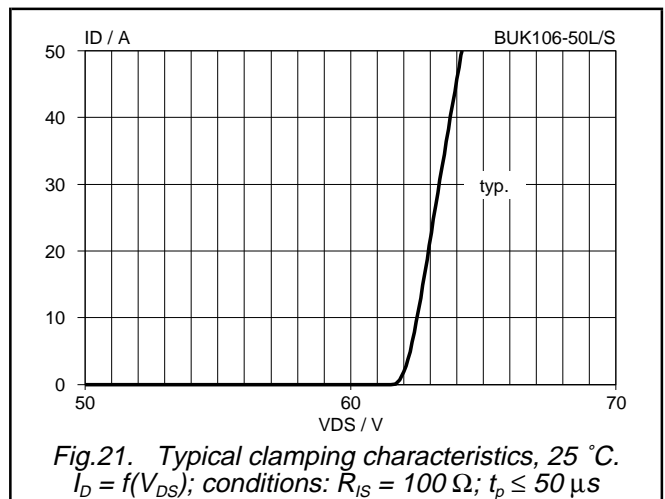
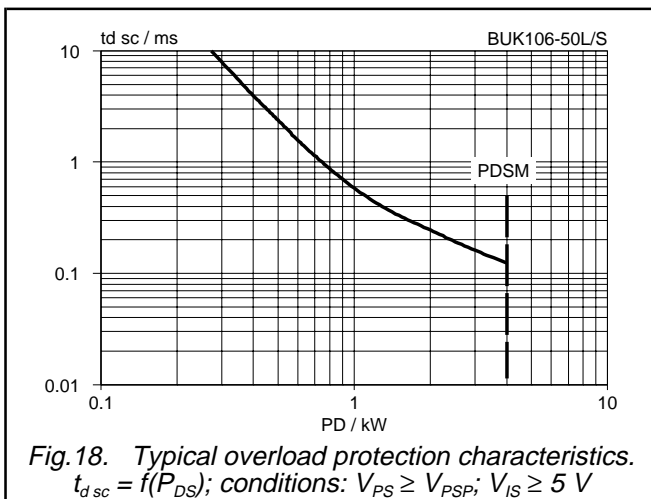
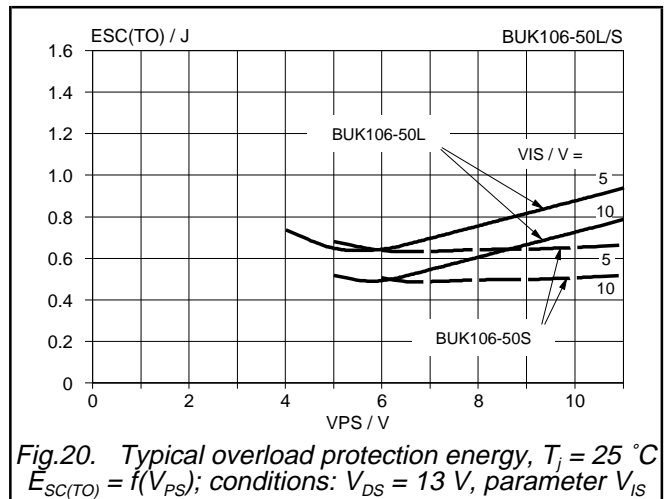
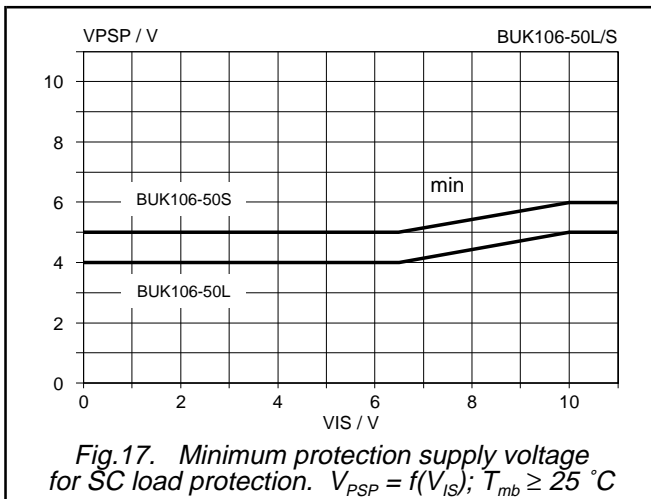
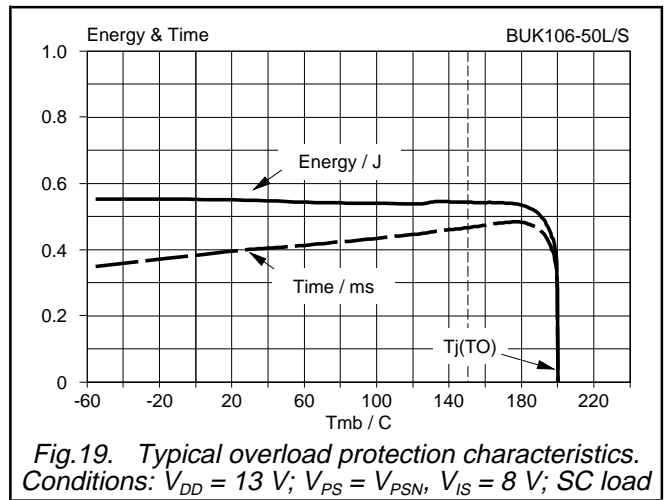
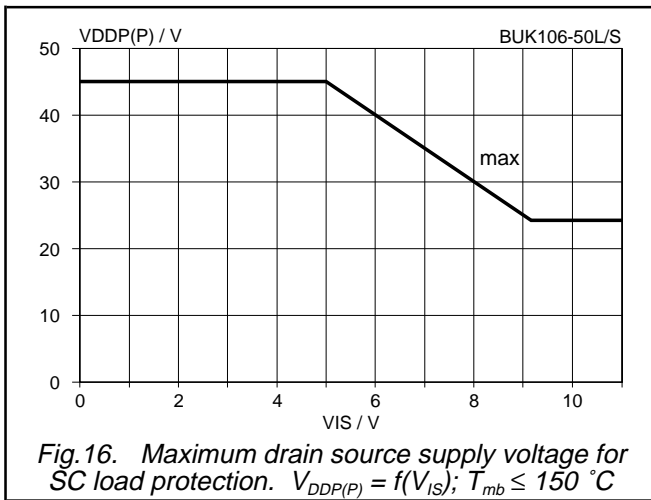
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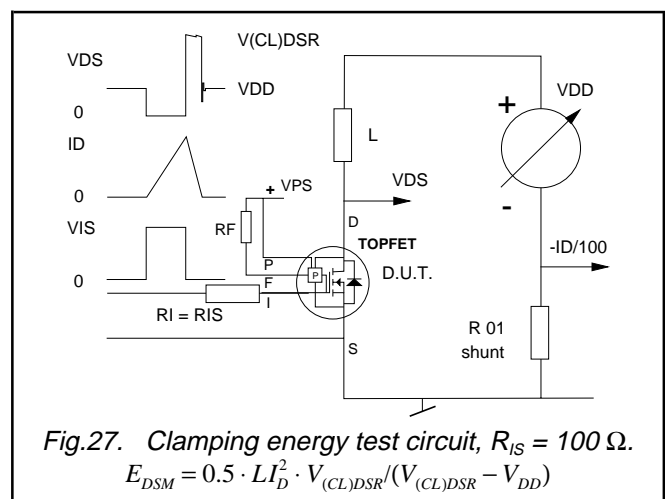
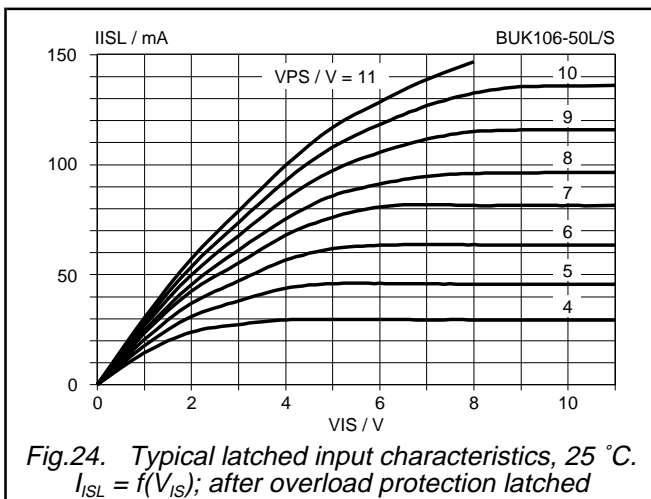
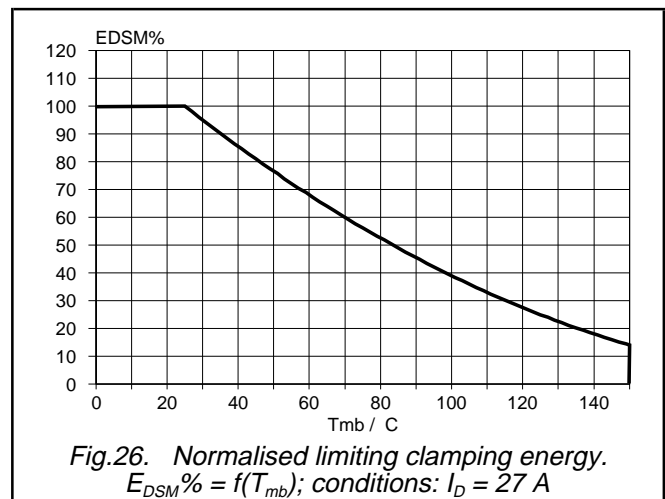
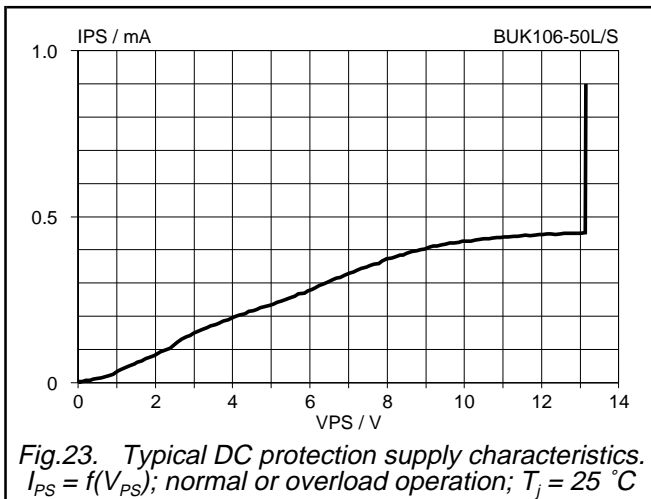
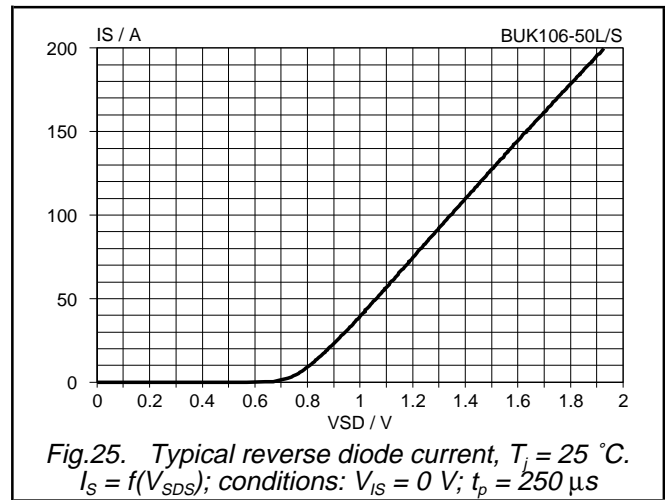
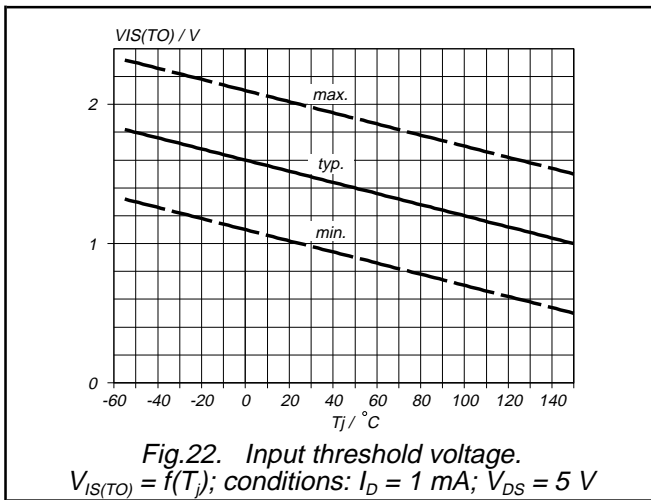
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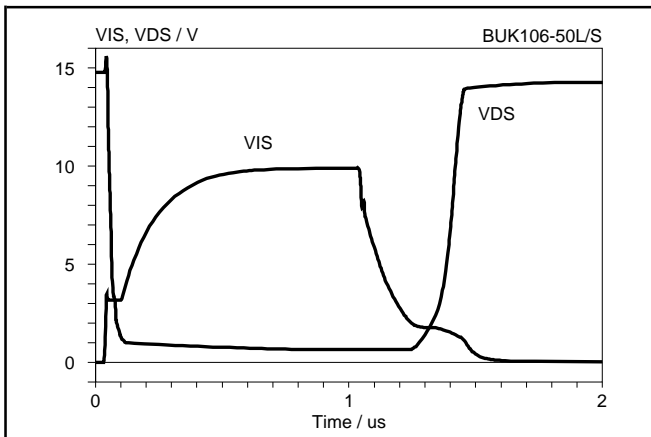


Fig.28. Typical resistive load switching waveforms
 $R_I = R_{IS} = 50 \Omega$; $R_L = 10 \Omega$; $V_{DD} = 15 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$

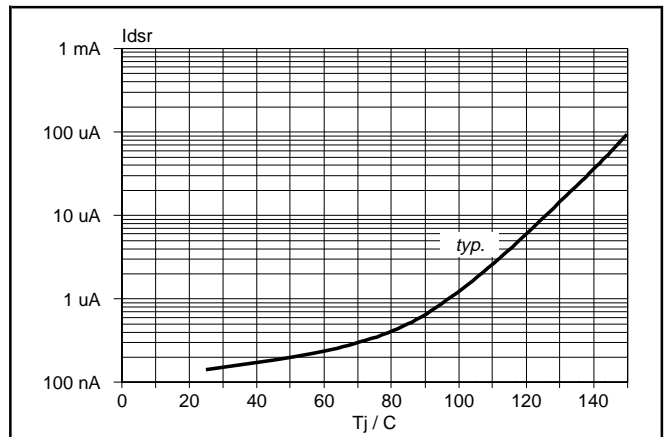


Fig.31. Typical off-state leakage current.
 $I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40 \text{ V}$; $R_{IS} = 100 \Omega$.

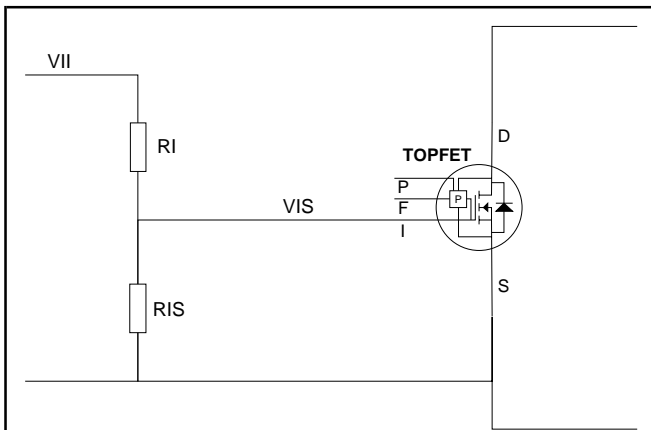


Fig.29. External input resistances R_I and R_{IS} , generator voltage V_{II} and input voltage V_{IS} .

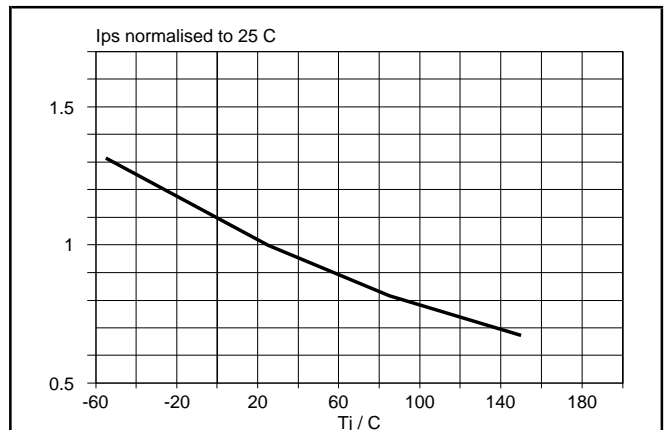


Fig.32. Normalised protection supply current.
 $I_{PS} / I_{PS, 25^\circ\text{C}} = f(T_j)$; $V_{PS} = V_{PSN}$

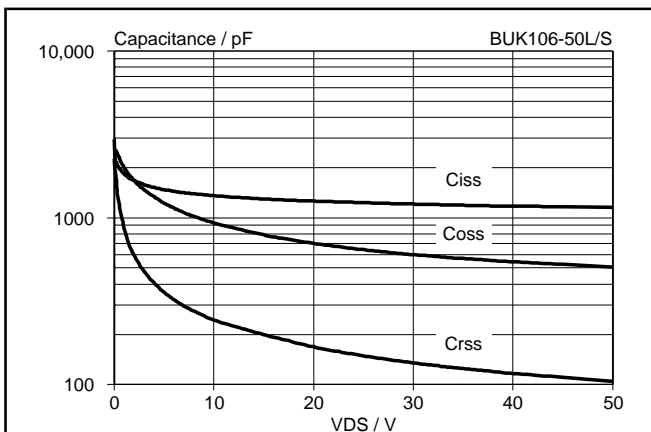
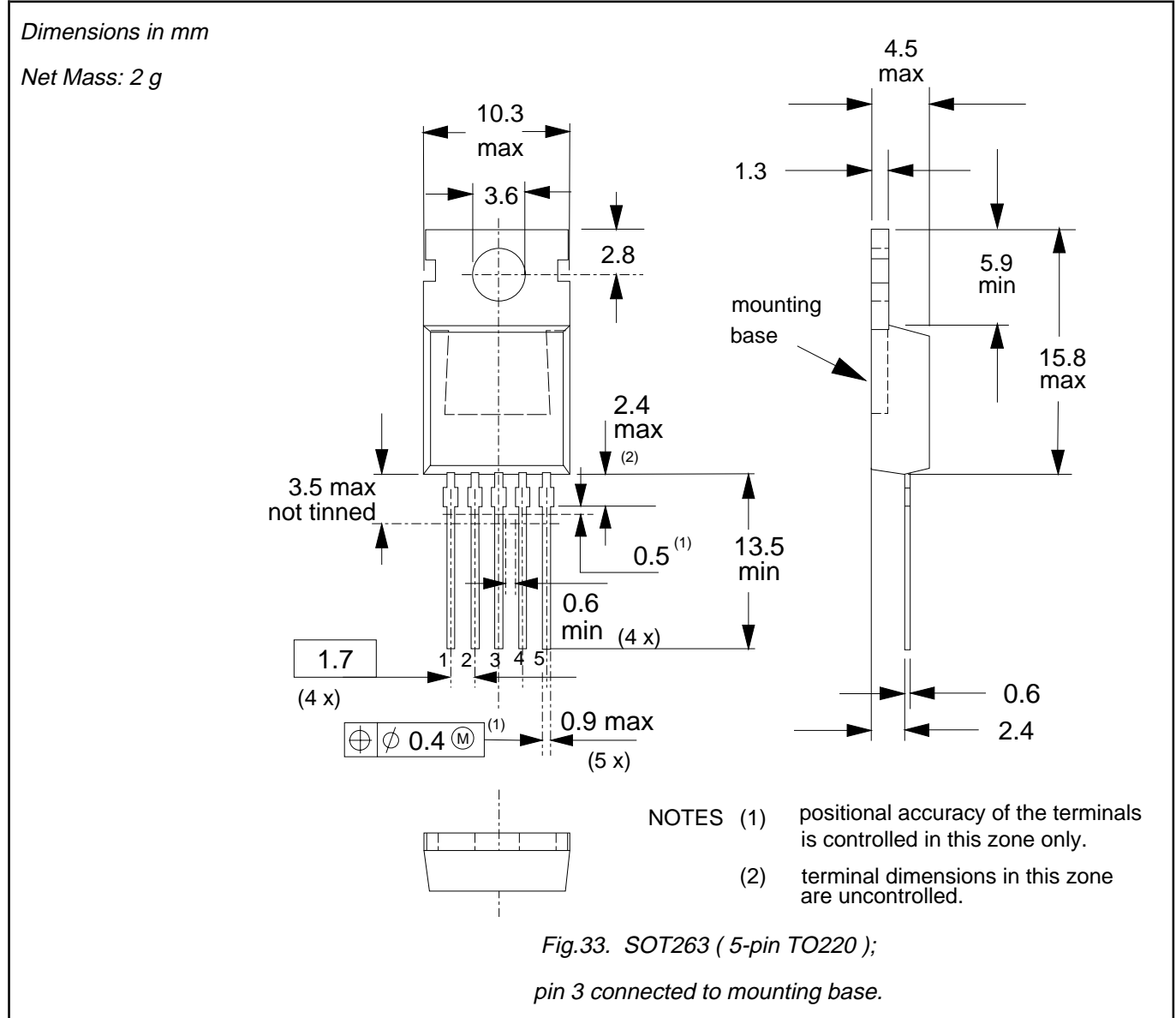


Fig.30. Typical capacitances, C_{ISS} , C_{OSS} , C_{RSS}
 $C = f(V_{DS})$; conditions: $V_{IS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

PowerMOS transistor
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MECHANICAL DATA



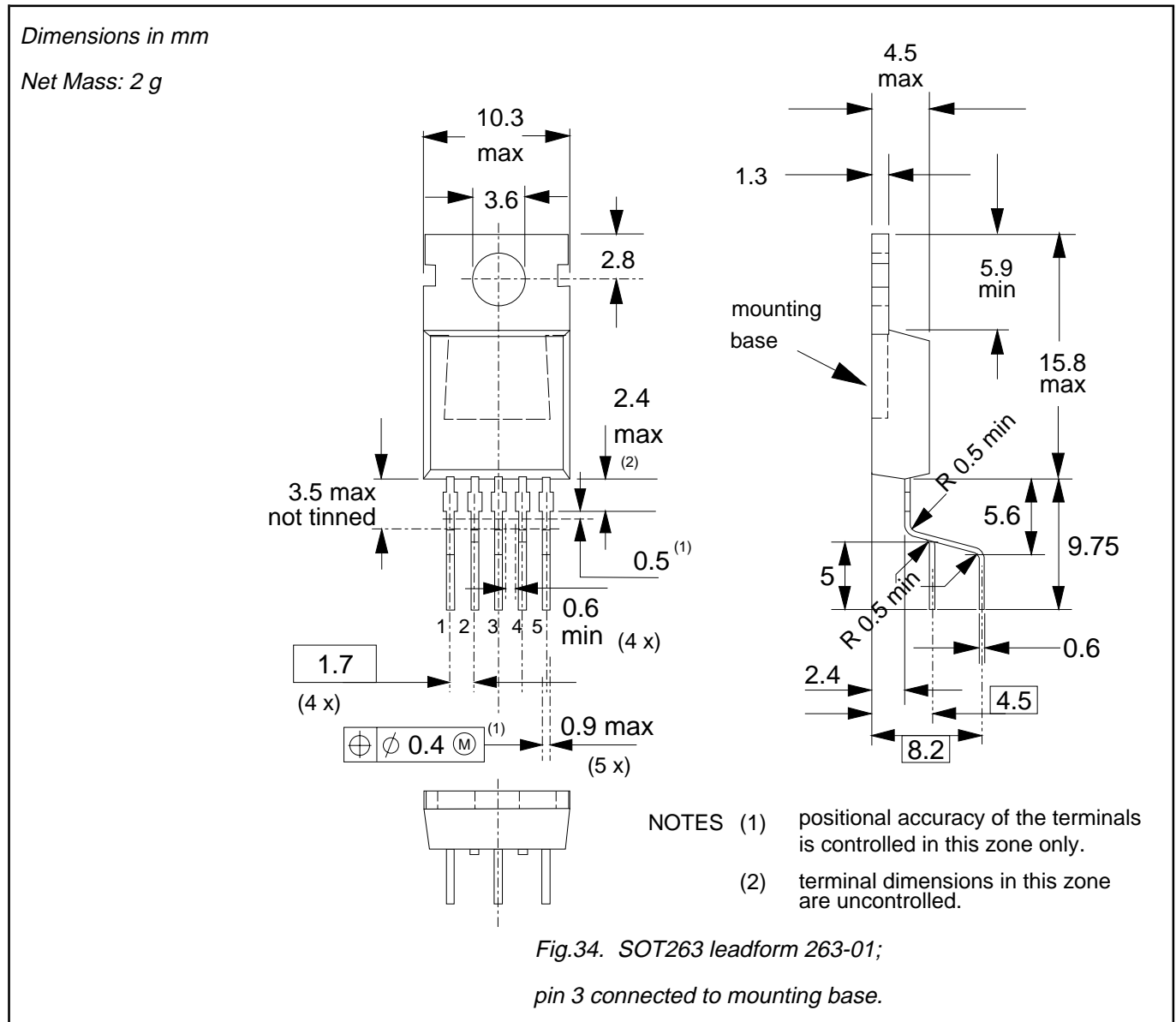
Note

1. Refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

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BUK106-50LP/SP

MECHANICAL DATA



Note

1. Refer to mounting instructions for TO220 envelopes.
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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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