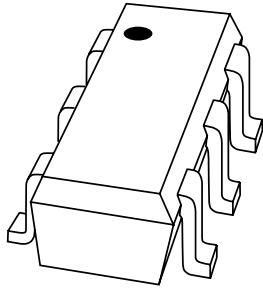


DATA SHEET



BF1102

Dual N-channel dual gate MOS-FET

Preliminary specification

1999 Jul 08

Dual N-channel dual gate MOS-FET

BF1102

FEATURES

- Two low noise gain controlled amplifiers in a single package
- Specially designed for 5 V applications
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

APPLICATIONS

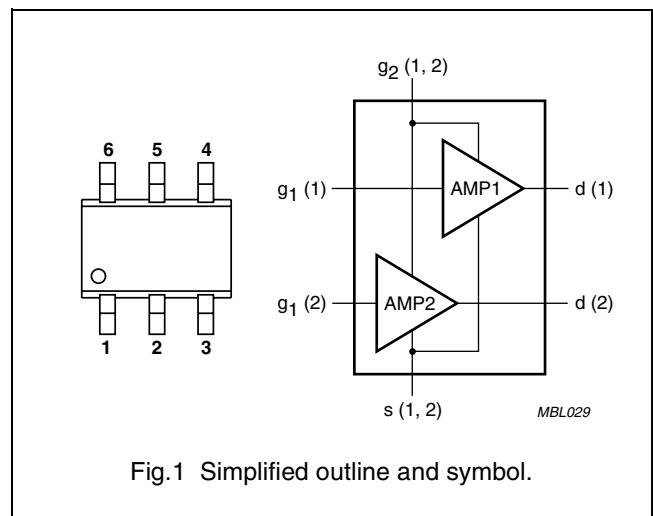
- Gain controlled low noise amplifier for VHF and UHF applications such as television tuners and professional communications equipment.

DESCRIPTION

The BF1102 is a combination of two equal dual gate MOS-FETs with shared source and gate 2 leads. The source and substrate are interconnected. An internal bias circuit enables DC stabilization and a very good cross-modulation performance at 5 V supply voltage. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT363 micro-miniature plastic package.

PINNING - SOT363

PIN	DESCRIPTION
1	gate 1 (1)
2	gate 2 (1,2)
3	drain (1)
4	drain (2)
5	source (1,2)
6	gate 1 (2)



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET unless otherwise specified						
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current (DC)		–	–	40	mA
P_{tot}	total power dissipation	$T_s \leq 102\text{ }^\circ\text{C}$; note 1	–	–	200	mW
$ y_{fs} $	forward transfer admittance	$I_D = 15\text{ mA}$	–	43	–	mS
C_{ig1-s}	input capacitance at gate 1	$I_D = 15\text{ mA}$	–	2.8	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	30	–	fF
F	noise figure	$f = 800\text{ MHz}$	–	–	2.8	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	–	–	dB μ V
T_j	operating junction temperature		–	–	150	$^\circ\text{C}$

Note

1. T_s is the temperature at the soldering point of the source lead.

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

Dual N-channel dual gate MOS-FET

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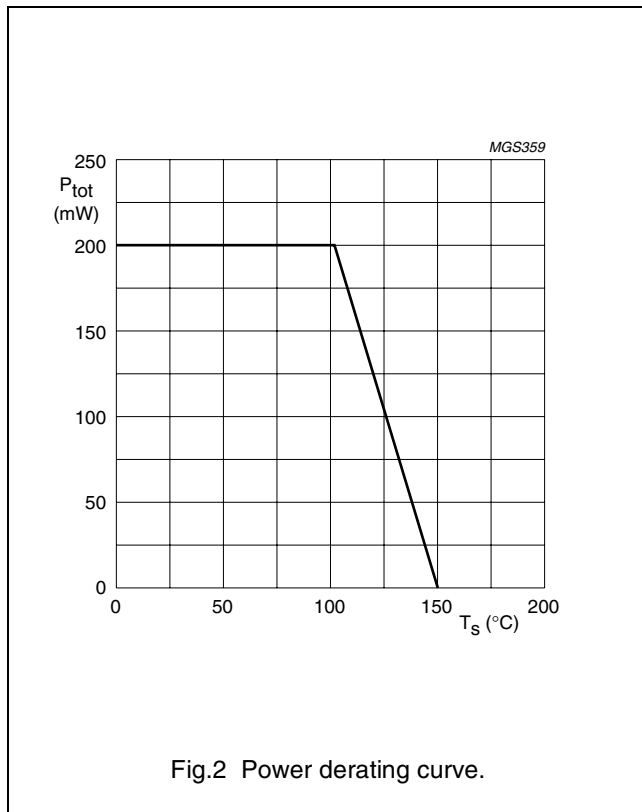
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
V _{DS}	drain-source voltage		–	7	V
I _D	drain current (DC)		–	40	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _s ≤ 102 °C	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point	240	K/W



Dual N-channel dual gate MOS-FET

BF1102

STATIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0; I_D = 10\text{ }\mu\text{A}$	7	–	V
$V_{(BR)G1-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0; I_{G1-S} = 10\text{ mA}$	6	15	V
$V_{(BR)G2-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0; I_{G2-S} = 5\text{ mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate voltage	$V_{G2-S} = V_{DS} = 0; I_{S-G1} = -10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate voltage	$V_{G1-S} = V_{DS} = 0; I_{S-G2} = -10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}; V_{G2-S} = 4\text{ V}; I_D = 20\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}; V_{G1-S} = 4\text{ V}; I_D = 20\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}; V_{DS} = 5\text{ V}; R_G = 120\text{ k}\Omega; \text{note 1}$	12	20	mA
I_{G1-S}	gate cut-off current	$V_{G1-S} = 5\text{ V}; V_{G2-S} = V_{DS} = 0$	–	50	nA
I_{G2-S}	gate cut-off current	$V_{G2-S} = 5\text{ V}; V_{G1-S} = V_{DS} = 0$	–	20	nA

Notes

- R_{G1} connects gate 1 to $V_{GG} = 5\text{ V}$.

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET unless otherwise specified (note 1)						
$ y_{fs} $	forward transfer admittance	$T_j = 25\text{ }^\circ\text{C}$	36	43	50	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	2	2.8	3.6	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	–	7	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	1.6	2.5	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	30	50	fF
F	noise figure	$f = 800\text{ MHz}; Y_S = Y_{S\text{ opt}}$	–	2	2.8	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\text{ MHz}; f_{unw} = 60\text{ MHz}$; (note 2)	85	–	–	dB μ V
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\text{ MHz}; f_{unw} = 60\text{ MHz}$; (note 2)	100	–	–	dB μ V

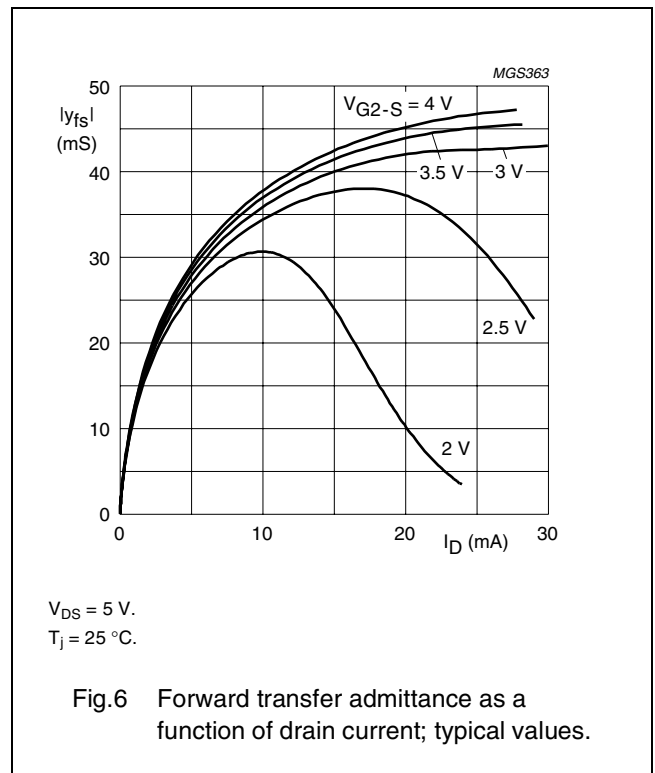
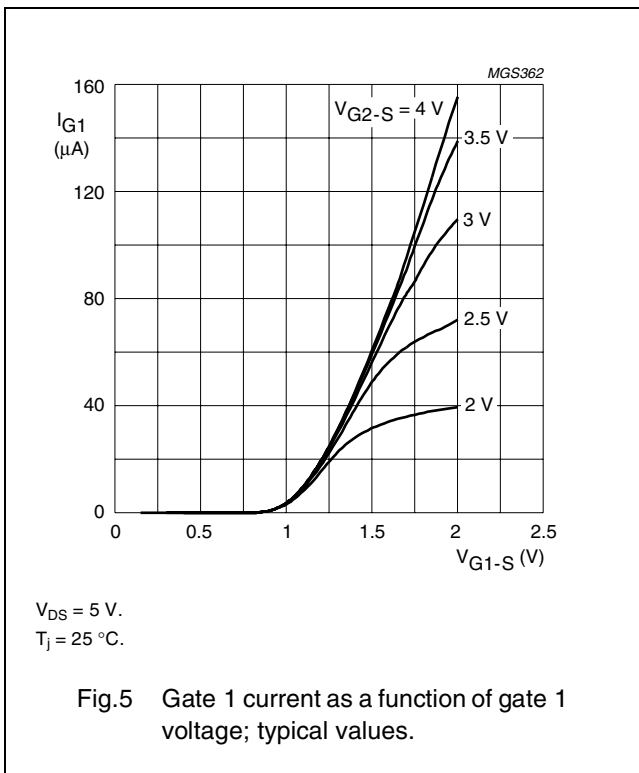
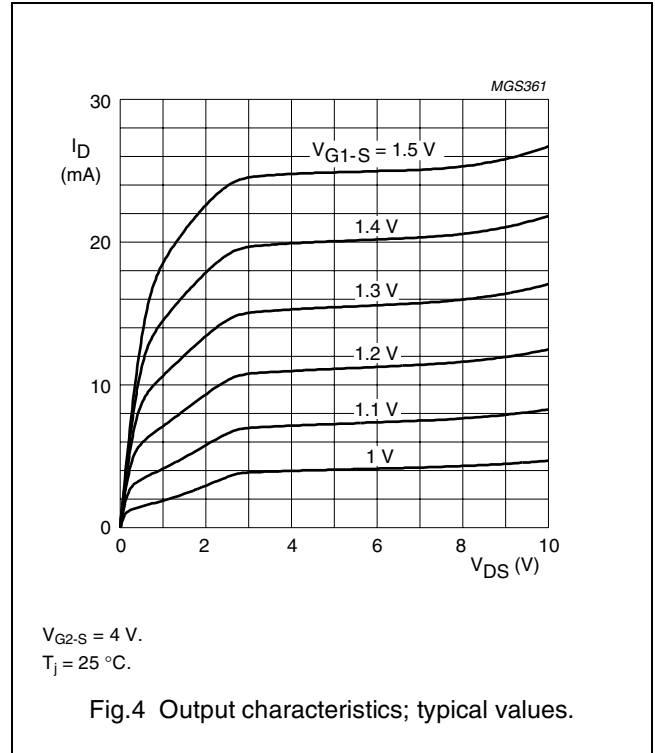
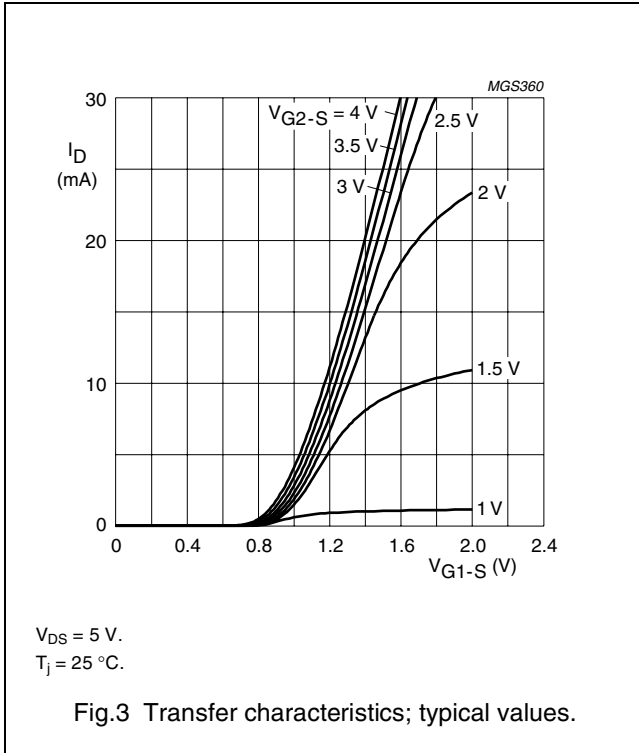
Notes

- Not used MOS-FET: $V_{G1-S} = 0; V_{DS} = 0$.
- Measured in test circuit of Fig.17.

Dual N-channel dual gate MOS-FET

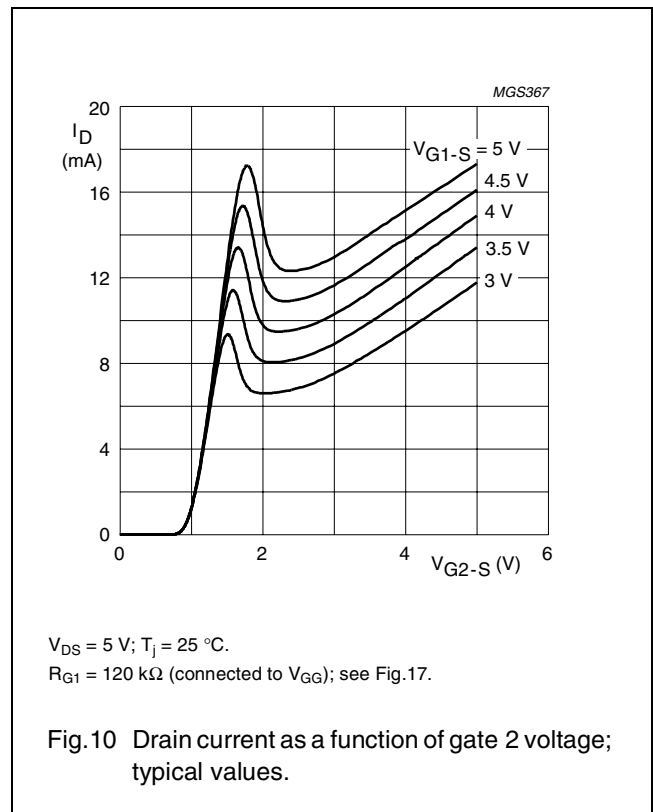
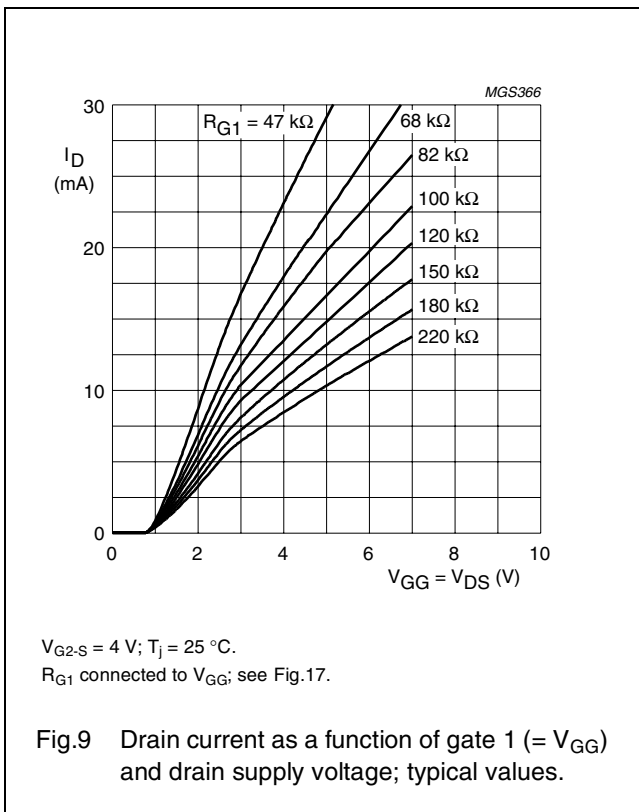
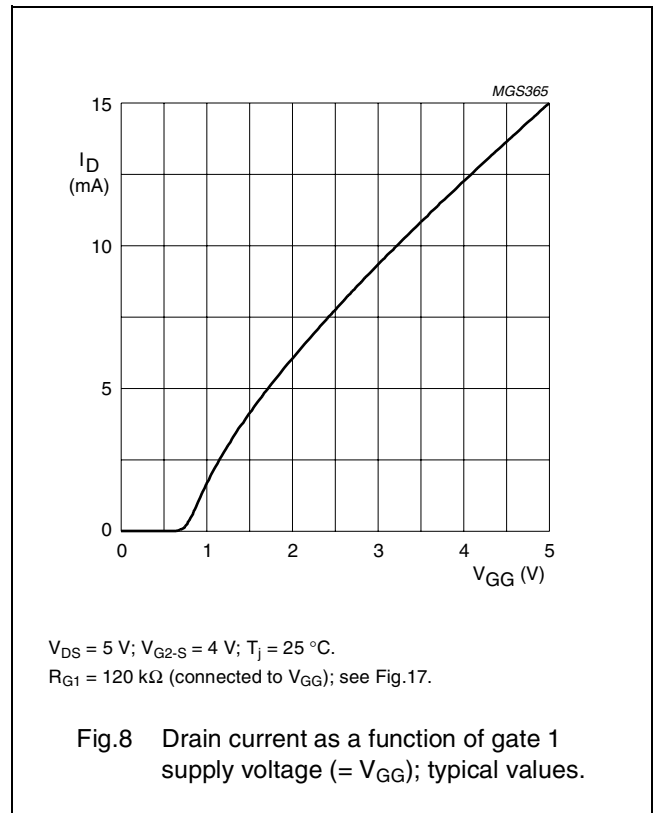
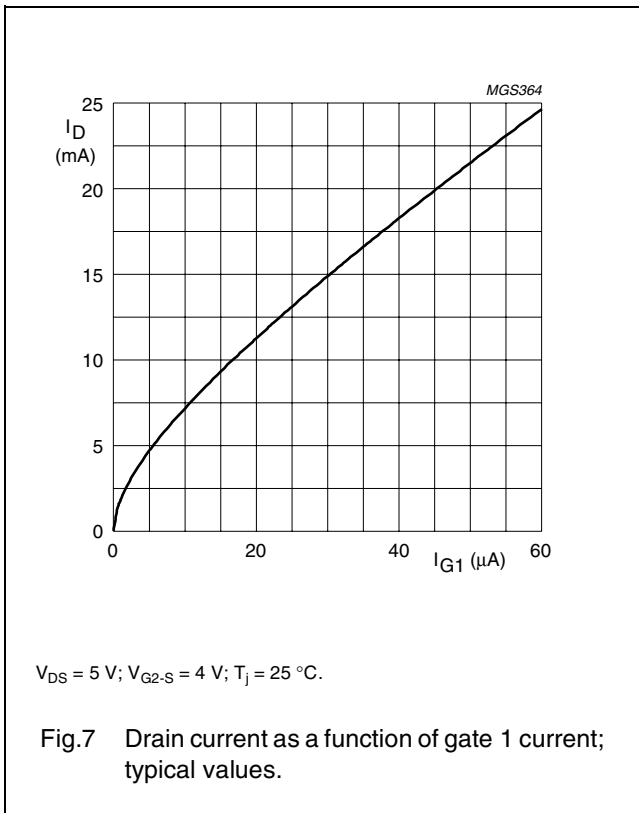
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ALL GRAPHS FOR ONE MOS-FET



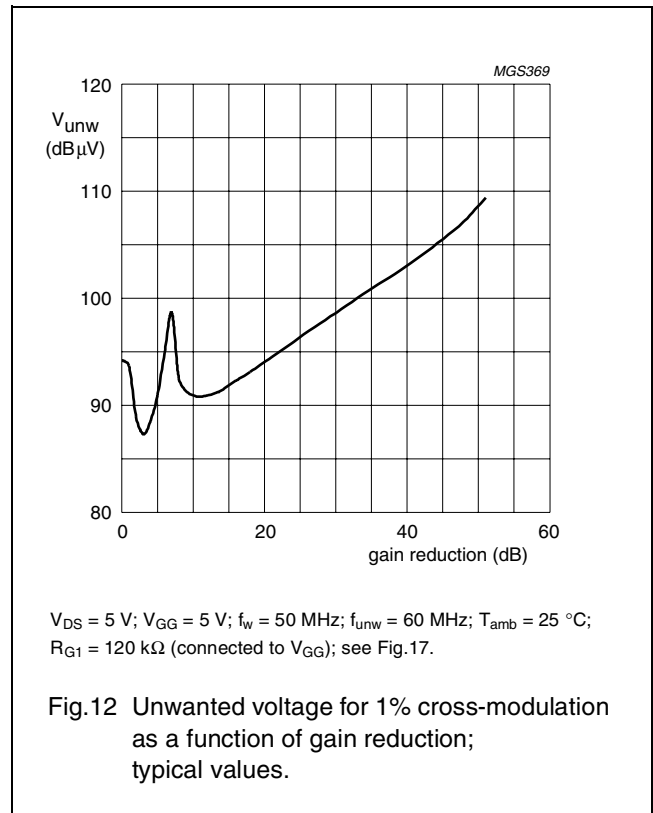
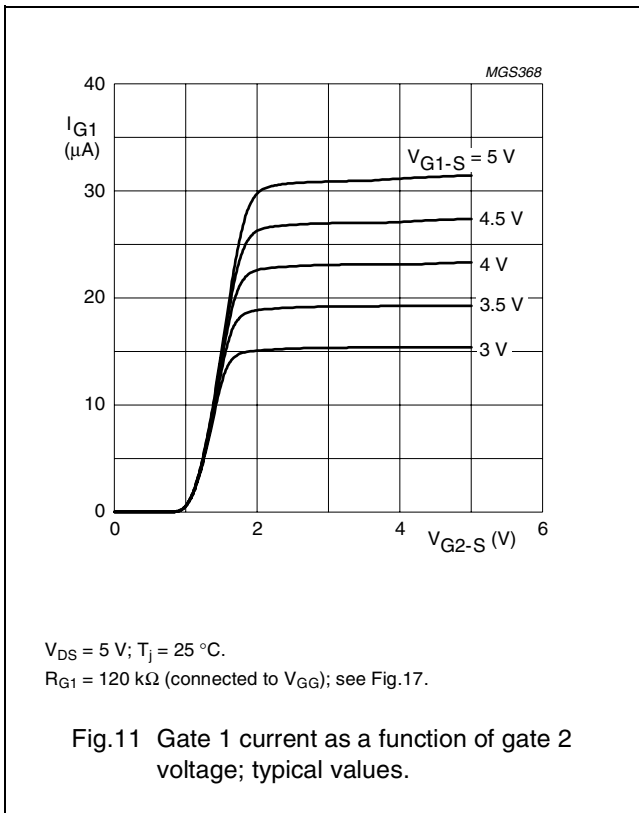
Dual N-channel dual gate MOS-FET

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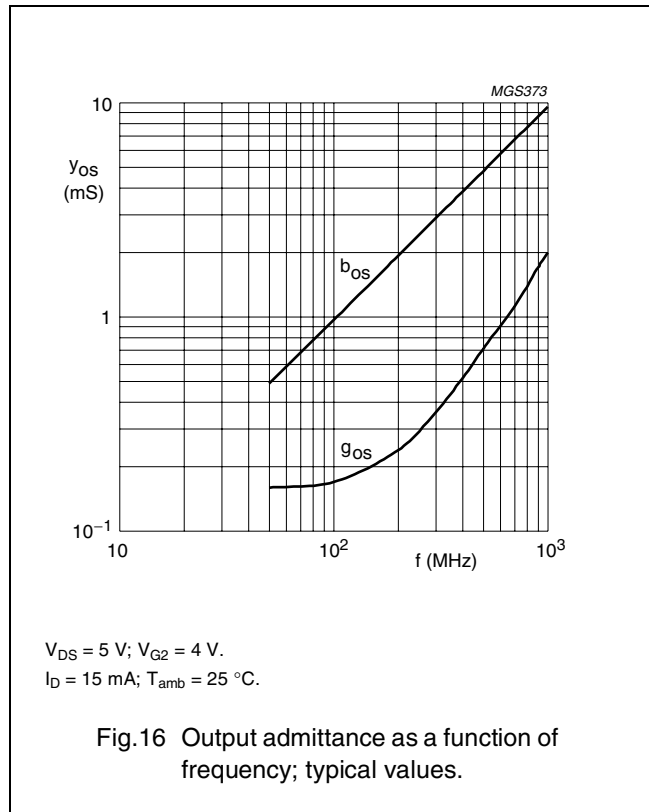
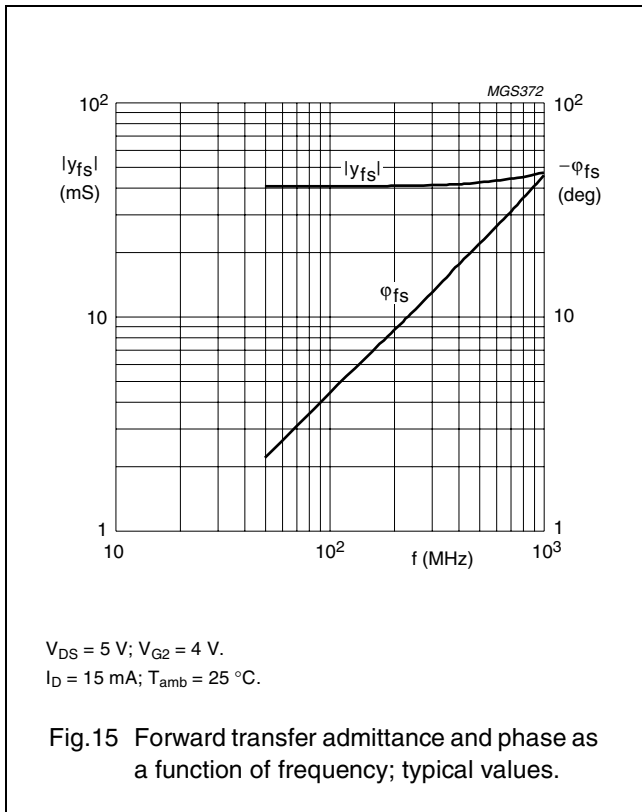
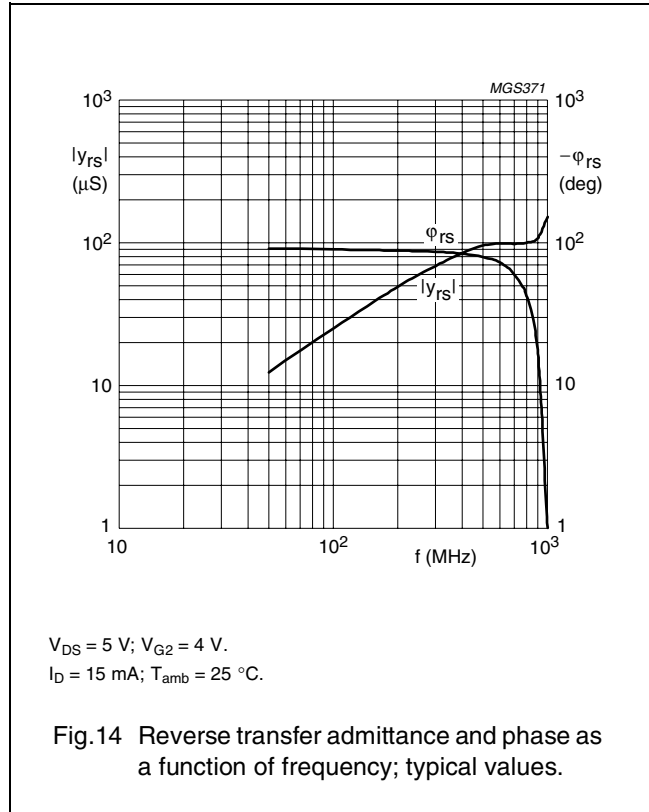
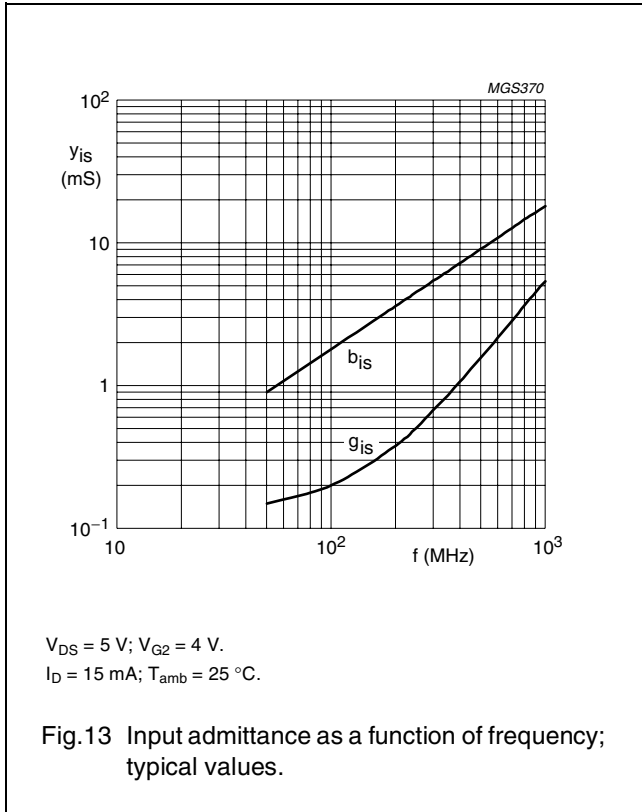
Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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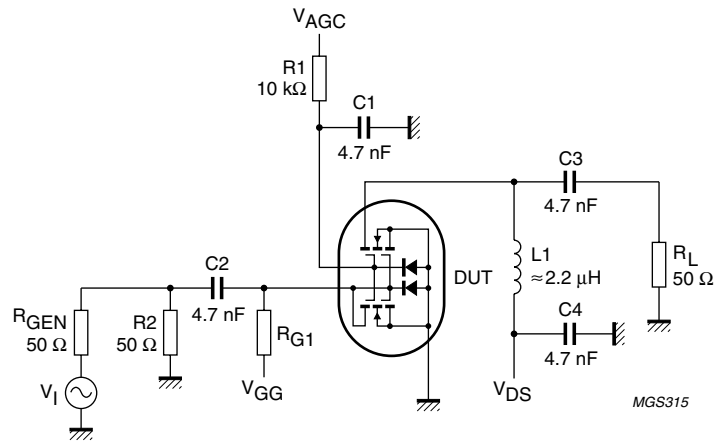


Fig.17 Cross-modulation test set-up (for one MOS-FET).

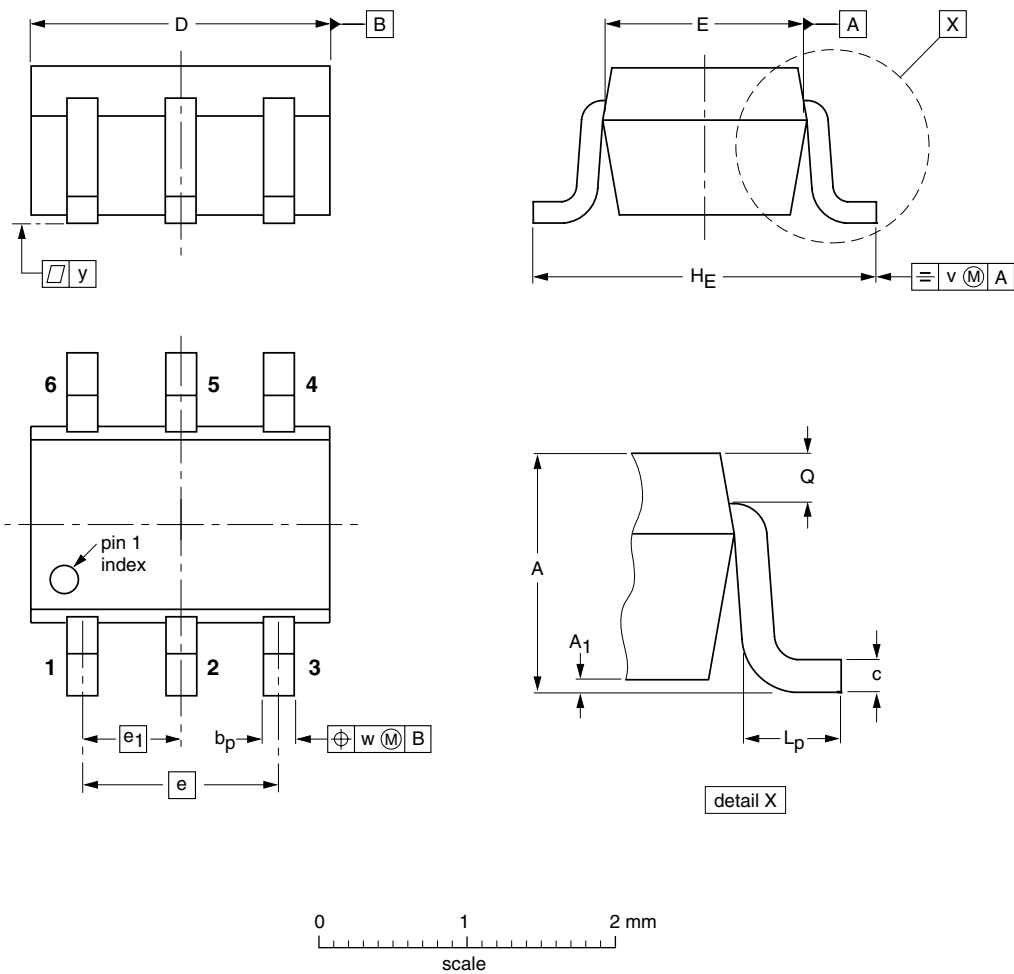
Dual N-channel dual gate MOS-FET

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Dual N-channel dual gate MOS-FET

BF1102

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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