

## CD4512BM/CD4512BC 8-Channel Buffered Data Selector

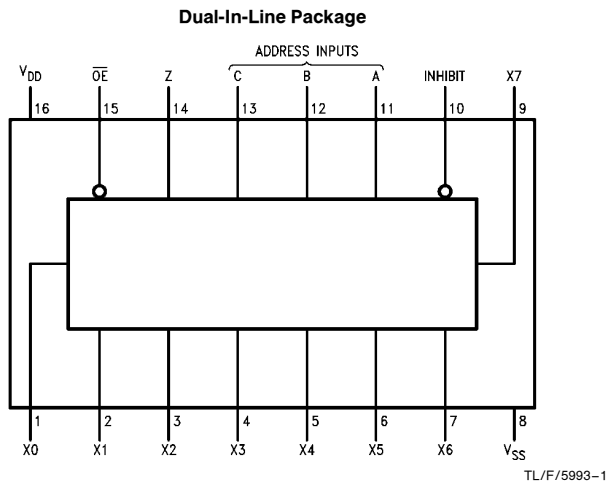
### General Description

The CD4512BM/CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable ( $\overline{OE}$ ) input forces the output into the TRI-STATE condition. Low levels at both the Inhibit and ( $\overline{OE}$ ) inputs allow normal operation.

### Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45  $V_{DD}$  (typ.)
- TRI-STATE output
- Low quiescent power dissipation 0.25  $\mu$ W/package (typ.) @  $V_{CC} = 5.0V$
- Plug-in replacement for Motorola MC14512

### Connection Diagram and Truth Table



Order Number CD4512B

Top View

Address Inputs			Control Inputs		Output
C	B	A	Inhibit	$\overline{OE}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
⊙	⊙	⊙	1	0	0
⊙	⊙	⊙	⊙	1	Hi-Z

⊙ = Don't care

Hi-Z = TRI-STATE condition

Xn = Data at input n

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### Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 to $V_{DD}$ + 0.5 $V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature, ( $T_L$ )	
(Soldering, 10 seconds)	260°C

### Recommended Operating Conditions (Note 2)

DC Supply Voltage ( $V_{DD}$ )	3.0 to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$
Operating Temperature Range ( $T_A$ )	
CD4512BM	-55°C to +125°C
CD4512BC	-40°C to +85°C

### DC Electrical Characteristics CD4512BM (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		5.0		0.005	5.0		150	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		10		0.010	10		300	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.015	20		600	$\mu A$
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
$V_{IL}$	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6.75	4.0		4.0	V
$V_{IH}$	High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	8.25		11.0		V
$I_{OL}$	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.78		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.0		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	7.8		2.4		mA
$I_{OH}$	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.25		-0.2			-0.14		mA
		$V_{DD} = 10V, V_O = 9.5V$	-0.62		-0.5			-0.35		mA
		$V_{DD} = 15V, V_O = 13.5V$	-1.8		-1.5			-1.1		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		$-10^{-5}$	-0.1		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		$10^{-5}$	0.1		1.0	$\mu A$
$I_{OZ}$	TRI-STATE Output Current	$V_{DD} = 15V, V_O = 0V$ $V_{DD} = 15V, V_O = 15V$		$\pm 0.1$		$-10^{-5}$	$\pm 0.1$		$\pm 3.0$	$\mu A$

### DC Electrical Characteristics CD4512BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.005	20		150	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		40		0.010	40		300	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		80		0.015	80		600	$\mu A$
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
$V_{IL}$	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6.75	4.0		4.0	V

## DC Electrical Characteristics CD4512BC (Note 2) (Continued)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High Level Input Voltage	V <sub>DD</sub> = 5V, V <sub>O</sub> = 4.5V	3.5		3.5	2.75		3.5		V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.0V	7.0		7.0	5.50		7.0		V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 13.5V	11.0		11.0	8.25		11.0		V
I <sub>OL</sub>	Low Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.4V	0.52		0.44	0.78		0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 0.5V	1.3		1.1	2.0		0.9		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V	3.6		3.4	7.8		2.4		mA
I <sub>OH</sub>	High Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 4.6V	-0.2		-0.16			-0.12		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.5	-0.5		-0.4			-0.3		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 13.5V	-1.4		-1.2			-1.0		mA
I <sub>IN</sub>	Input Current	V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V		-0.3		-10 <sup>-5</sup>	-0.3		-1.0	μA
		V <sub>DD</sub> = 15V, V <sub>IN</sub> = 15V		0.3		10 <sup>-5</sup>	0.3		1.0	μA
I <sub>OZ</sub>	TRI-STATE Output Current	V <sub>DD</sub> = 15V, V <sub>O</sub> = 0V V <sub>DD</sub> = 15V, V <sub>O</sub> = 15V		±1.0		±10 <sup>-5</sup>	±1.0		±7.5	μA

## AC Electrical Characteristics\* T<sub>A</sub> = 25°C, t<sub>r</sub> = t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF

Symbol	Parameter	Conditions	CD4512BM			CD4512BC			Units
			Min	Typ	Max	Min	Typ	Max	
t <sub>PHL</sub>	Propagation Delay High-to-Low Level	V <sub>DD</sub> = 5V		225	500		225	750	ns
		V <sub>DD</sub> = 10V		75	175		75	200	ns
		V <sub>DD</sub> = 15V		57	130		57	150	ns
t <sub>PLH</sub>	Propagation Delay Low-to-High Level	V <sub>DD</sub> = 5V		225	500		225	750	ns
		V <sub>DD</sub> = 10V		75	175		75	200	ns
		V <sub>DD</sub> = 15V		57	130		57	150	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time	V <sub>DD</sub> = 5V		70	200		70	200	ns
		V <sub>DD</sub> = 10V		35	100		35	100	ns
		V <sub>DD</sub> = 15V		25	80		25	80	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Propagation Delay into TRI-STATE from Logic Level	V <sub>DD</sub> = 5V		50	125		50	125	ns
		V <sub>DD</sub> = 10V		25	75		25	75	ns
		V <sub>DD</sub> = 15V		19	60		19	60	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Propagation Delay to Logic Level from TRI-STATE	V <sub>DD</sub> = 5V		50	125		50	125	ns
		V <sub>DD</sub> = 10V		25	75		25	75	ns
		V <sub>DD</sub> = 15V		19	60		19	60	ns
C <sub>IN</sub>	Input Capacitance	(Note 4)		7.5	15		7.5	15	pF
C <sub>OUT</sub>	TRI-STATE Output Capacitance	(Note 4)		7.5	15		7.5	15	pF
C <sub>PD</sub>	Power Dissipation Capacity	(Note 5)		150			150		pF

\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

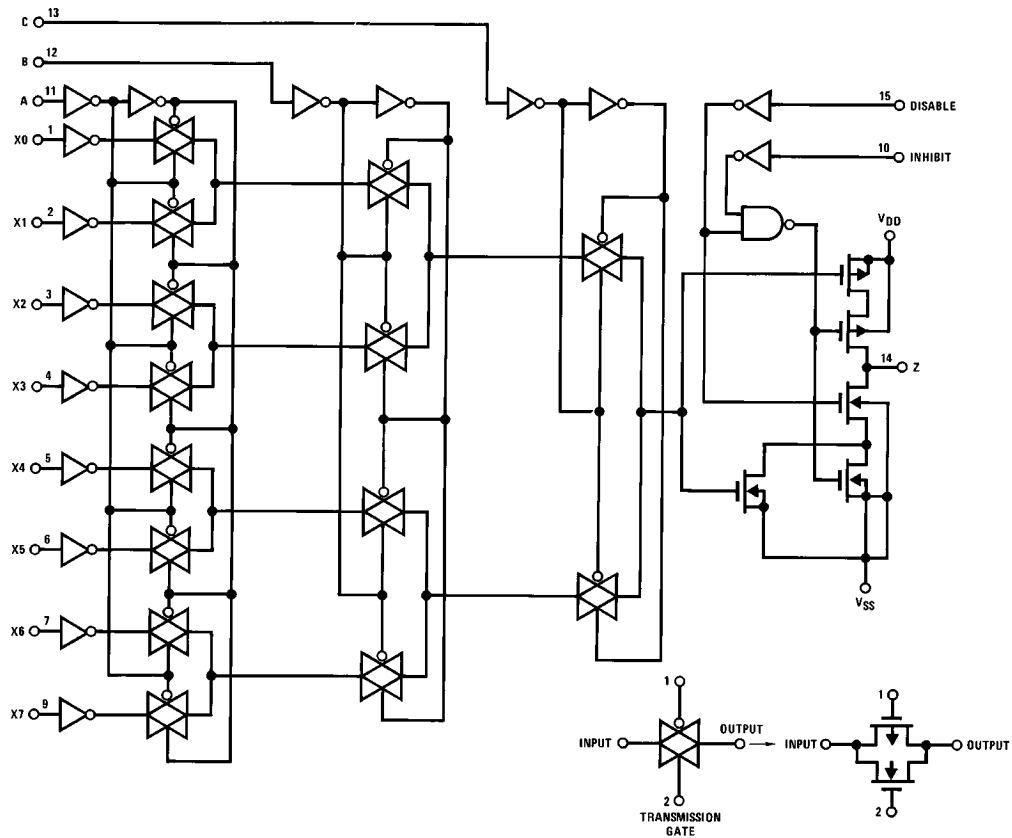
**Note 2:** V<sub>SS</sub> = 0V unless otherwise specified.

**Note 3:** I<sub>OH</sub> and I<sub>OL</sub> are tested one output at a time.

**Note 4:** Capacitance guaranteed by periodic testing.

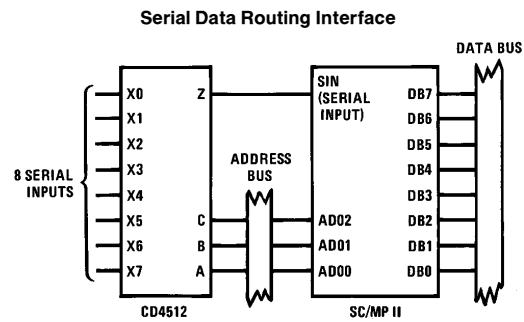
**Note 5:** C<sub>PD</sub> determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note, AN-90.

## Logic Diagram



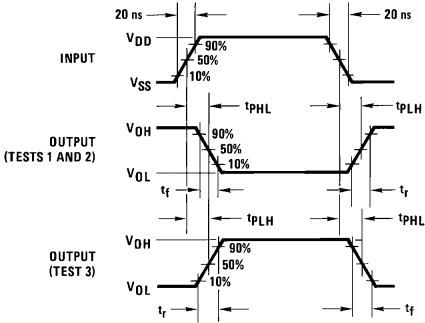
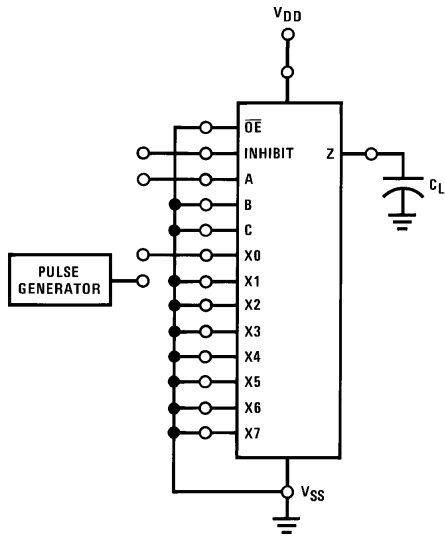
TL/F/5993-2

## Typical Application



TL/F/5993-3

## AC Test Circuit and Switching Time Waveforms



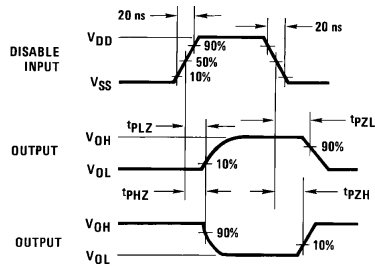
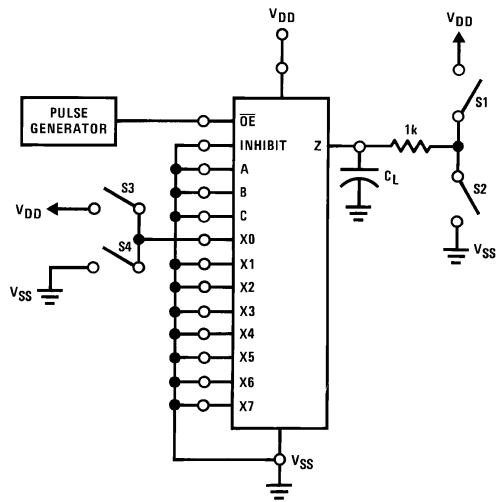
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TL/F/5993-4

Input Connections for  $t_r$ ,  $t_f$ ,  $t_{PLH}$ ,  $t_{PHL}$

Test	Inhibit	A	X0
1	PG	GND	$V_{DD}$
2	GND	PG	$V_{DD}$
3	GND	GND	PG

## TRI-STATE AC Test Circuit and Switching Time Waveforms



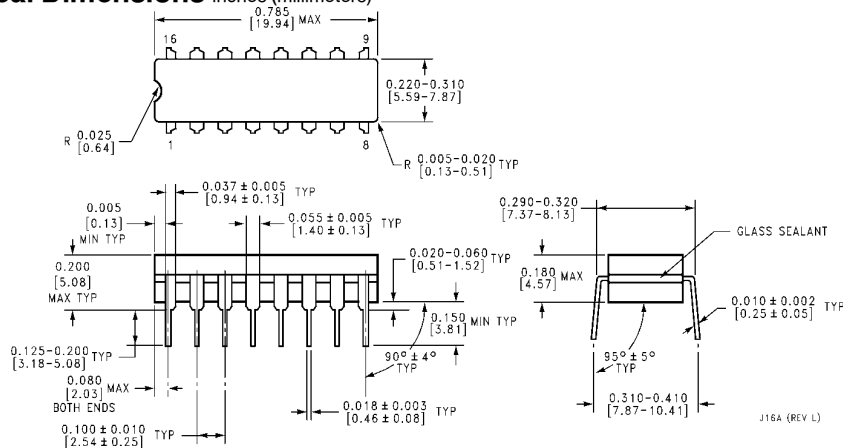
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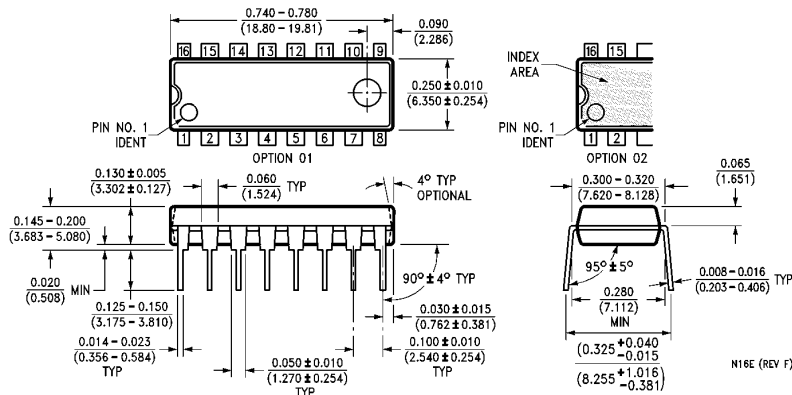
Switch Positions for TRI-STATE Test

Test	S1	S2	S3	S4
$t_{PHZ}$	Open	Closed	Closed	Open
$t_{PLZ}$	Closed	Open	Open	Closed
$t_{PZH}$	Closed	Open	Open	Closed
$t_{PZH}$	Open	Closed	Closed	Open

**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number CD4512BMJ or CD4512BCJ**  
**NS Package Number J16A**



**Molded Dual-In-Line Package (N)**  
**Order Number CD4512BMN or CD4512BCN**  
**NS Package Number N16E**

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