National Semiconductor

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ADC14061
Self-Calibrating 14-Bit, 2.5 MSPS, 390 mW A/D Converter

General Description

The ADC14061 is a self-calibrating 14-bit, 2.5 Megasample per second analog to digital converter. It operates on a single +5V supply, consuming just 390mW (typ).

The ADC14061 provides an easy and affordable upgrade from 12 bit converters. The ADC14061 may also be used to replace many hybrid converters with a resultant saving of space, power and cost.

The ADC14061 operates with excellent dynamic performance at input frequencies up to ½ the clock frequency. The calibration feature of the ADC14061 can be used to get more consistent and repeatable results over the entire operating temperature range. On-command self-calibration reduces many of the effects of temperature-induced drift, resulting in more repeatable conversions.

The Power Down feature reduces power consumption to less than 2mW.

The ADC14061 comes in a TQFP and is designed to operate over the commercial temperature range of 0˚C to +70˚C.

Features

- Single +5V Operation
- Auto-Calibration
- Power Down Mode
- TTL/CMOS Input/Output compatible

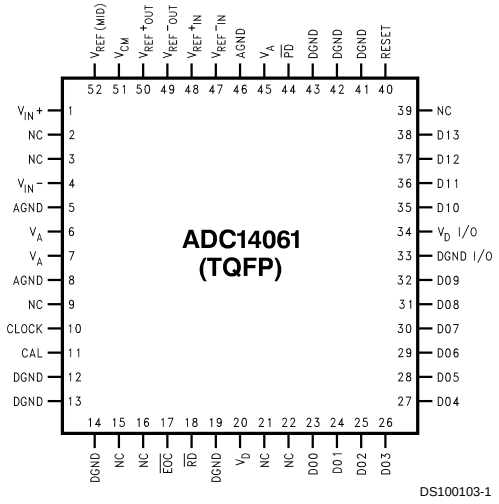
Key Specifications

■ Resolution	14 Bits
■ Conversion Rate	2.5 Msps (min)
■ DNL	0.3 LSB (typ)
■ SNR (f_{IN} = 500 kHz)	80 dB (typ)
■ ENOB	12.8 Bits (typ)
■ Supply Voltage	+5V ±5%
■ Power Consumption	390mW (typ)

Applications

- Instrumentation
- PC-Based Data Acquisition
- Data Communications
- Blood Analyzers
- Sonar/Radar

Connection Diagram



DS100103-1

Ordering Information

Commercial ($0^{\circ}C \leq TA \leq +70^{\circ}C$)	Package
ADC14061CCVT	VEG52A 52 Pin Thin Quad Flat Pack

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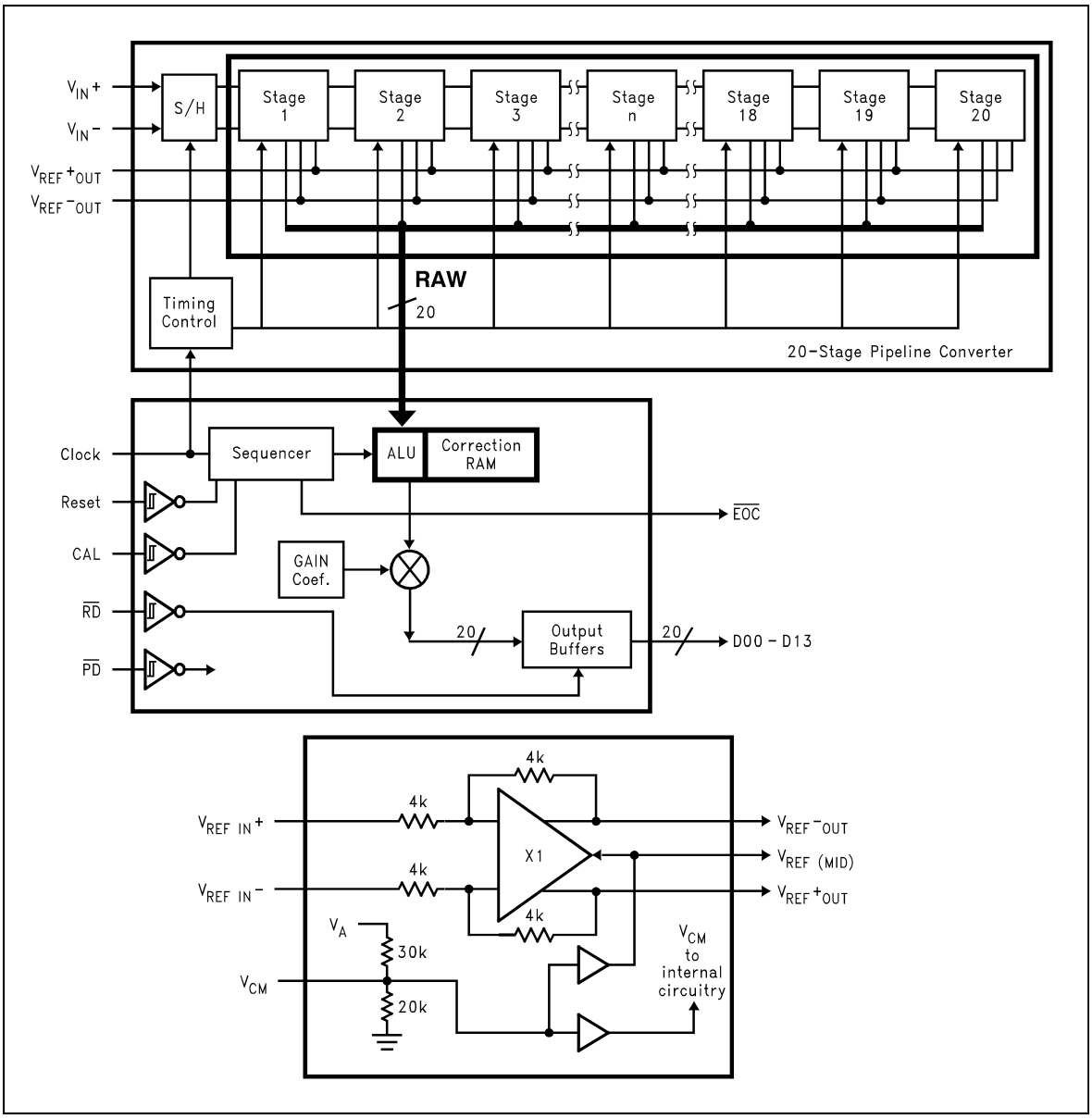
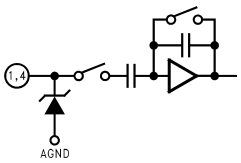
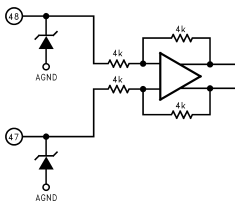
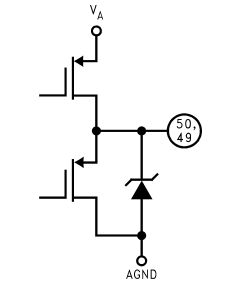
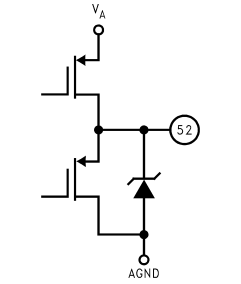
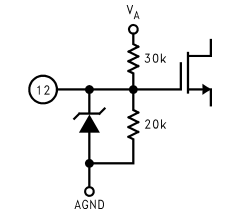
Block Diagram



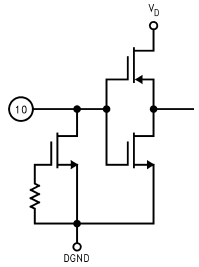
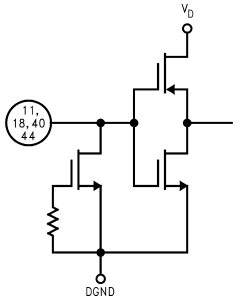
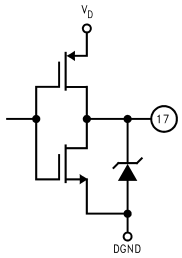
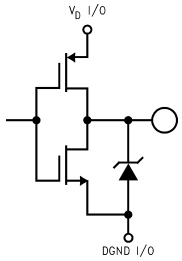
DS100103-2

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
1	$V_{IN}+$		Non-Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 volt to 3.0 Volts.
4	$V_{IN}-$		Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 Volt to 3.0 Volts. The input signal should be balanced for best performance.
48	$V_{REF}+$ IN		Positive reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+$ minus V_{REF-} IN should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+$ IN minus $V_{REF}-$ IN.
47	$V_{REF}-$ IN		Negative reference input. In most applications this pin should be connected to AGND and the full reference voltage applied to $V_{REF}+$ IN. If the application requires that $V_{REF}-_{IN}$ be offset from AGND, this pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+$ IN minus V_{REF-} IN should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+$ IN minus $V_{REF}-$ IN .
50	$V_{REF}+$ OUT		Output of the high impedance positive reference buffer. With a 2.0V reference input, and with a V_{CM} of 2.0V, this pin will have a 3.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
49	REF− OUT		The output of the negative reference buffer. With a 2.0V reference and a V_{CM} of 2.0V, this pin will have a 1.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
52	$V_{REF\ (MID)}$		Output of the reference mid-point, nominally equal to 0.4 V_A (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. This voltage is derived from V_{CM}.
51	V_{CM}		Input to the common mode buffer, nominally equal to 40% of the supply voltage (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. Best performance is obtained if this pin is driven with a low impedance source of 2.0V.

Pin Descriptions and Equivalent Circuits (Continued)

Digital I/O

10	Clock		Digital clock input. The input voltage is captured t_{AD} after the fall of the clock signal. The range of frequencies for this input is 300 kHz to 2.5 MHz. The clock frequency should not be changed or interrupted during conversion or while reading data output.
11	CAL		CAL is a level-sensitive digital input that, when pulsed high for at least two clock cycles, puts the ADC into the CALIBRATE mode. Calibration should be performed upon ADC power-up (after asserting a reset) and each time the temperature changes by more than 50˚C since the ADC14061 was last calibrated. See Section 2.3 for more information.
40	RESET		RESET is a level-sensitive digital input that, when pulsed high for at least 2 CLOCK cycles, results in the resetting of the ADC. This reset pulse must be applied after ADC power-up, before calibration.
18	$\overline{RD}$		$\overline{RD}$ is the (READ) digital input that, when low, enables the output data buffers. When this input pin is high, the output data bus is in a high impedance state.
44	$\overline{PD}$		$\overline{PD}$ is the Power Down input that, when low, puts the converter into the power down mode. When this pin is high, the converter is in the active mode.
17	$\overline{EOC}$		$\overline{EOC}$ is a digital output that, when low, indicates the availability of new conversion results at the data output pins.
23-32 35-38	D00-13		Digital data outputs that make up the 14-bit TRI-STATE conversion results. D00 is the LSB, while D13 is the MSB (SIGN bit) of the two's complement output word.

Analog Power

6, 7, 45	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet +5V source and bypassed to AGND with 0.1 µF monolithic capacitors in parallel with 10 µF capacitors, both located within 1 cm of these power pins.
5, 8, 46	AGND		The ground return for the analog supply. AGND and DGND should be connected together directly beneath the ADC14061 package. See Section 5 (Layout and grounding) for more details).

Pin Descriptions and Equivalent Circuits (Continued)

Digital Power			
20	V_D		Positive digital supply pin. This pin should be connected to the same clean, quiet +5V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10µF capacitor, both located within 1 cm of the power pin.
12,13 14,19, 41,42, 43	DGND		The ground return for the digital supply. AGND and DGND should be connected together directly beneath the ADC14061 package. See Section 5 (Layout and Grounding) for more details.
34	V_D I/O		Positive digital supply pin for the ADC14061's output drivers. This pin should be connected to a +3V to +5V source and bypassed to DGND I/O with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF capacitor. All bypass capacitors should be located within 1 cm of the supply pin.
33	DGND I/O		The ground return for the digital supply for the ADC14061's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC14061's DGND or AGND pins. See Section 5.0 (Layout and Grounding) for more details.
NC			
2, 3, 9, 15, 16, 21, 22, 39	NC		All pins marked NC (no connect) should be left floating. Do not connect the NC pins to ground, power supplies, or any other potential or signal. These pins are used for test in the manufacturing process.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A, V_D, V_D I/O)	6.5V
Voltage on Any I/O Pin	−0.3V to V^+ +0.3V
Input Current at Any Pin (Note 3)	±25mA
Package Input Current (Note 3)	±50mA
Power Dissipation at T_A = 25˚C	(Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	1500V
Machine Model	200V
Soldering Temp., Infrared, 10 sec. (Note 6)	300˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	0˚C ≤ T_A ≤ +70˚C
V_A, V_D	+4.75V to +5.25V
V_D I/O	2.7V to V_D
V_{REF} − IN	1.0V to 3.0V
V_{REF}− IN	AGND to 0.1V
Digital Inputs	−0.05V to V_D + 0.05V
$\|V_A - V_D\|$	≤ 100 mV
|AGND - DGND |	0V to 100 mV

Converter Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V^+ = V_A = V_D = +5.0V, V_D I/O = 3.0V or 5.0V, $\overline{PD}$ = +5V, $V_{REF+\ IN}$ = +2.0V, $V_{REF-\ IN}$ = AGND, f_{CLK} = 2.5 MHz, C_L = 50 pF/pin. After Auto-Cal @ Temperature. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX}:** all other limits T_A = T_J = 25˚C(Notes 7, 8, 9)

Symbol	Parameter	Conditions		Typical (Note 10)	Limits (Note 11)	Units
Static Converter Characteristics						
	Resolution with No Missing Codes				**14**	Bits(min)
INL	Integral Non Linearity			±0.75	**±2.5**	LSB(max)
DNL	Differential Non Linearity			±0.3	**±1.0**	LSB(max)
	Full-Scale Error			±0.4	**±2.8**	% FS(max)
	Zero Offset Error			+0.1	**±0.6**	% FS(max)
Reference and Analog Input Characteristics						
V_{IN}	Input Voltage Range (V_{IN+} − V_{IN-})	V_{REF} = V_{REF}+ $_{IN}$ − V_{REF}+ $_{IN}$ −		2.0	**1.8** **2.2**	V(min) V(max)
C_{IN}	Input Capacitance	V_{IN} = 1.0V + 0.7Vrms	(CLK LOW)	12		pF
			(CLK HIGH)	28		pF
V_{REF}	Reference Voltage Range [(V_{REF}+ $_{IN}$) − (V_{REF} −$_{IN}$)] (Note 14)			2.00	**1.8** **2.2**	V(min) V(max)
	Reference Input Resistance			3.5		KΩ
Dynamic Converter Characteristics						
BW	Full Power Bandwidth			8		MHz
SNR	Signal-to-Noise Ratio	f_{IN} = 500 kHz, V_{IN} = 1.9V_{P-P}		80		dB
SINAD	Signal-to-Noise & Distortion	f_{IN} = 500 kHz, V_{IN} = 1.9V_{P-P}		79		dB
ENOB	Effective Number of Bits	f_{IN} = 500 kHz, V_{IN} = 1.9V_{P-P}		12.8		Bits
THD	Total Harmonic Distortion	f_{IN} = 500 kHz, V_{IN} = 1.9V_{P-P}		−88		dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 500 kHz, V_{IN} = 1.9V_{P-P}		90		dB
IMD	Intermodulation Distortion	f_{IN1} = 95 kHz f_{IN2} = 105 kHz		−97		dB

DC and Logic Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, $V^+ = V_A = V_D$ = +5.0V, V_D I/O = 3.0V or 5.0V, $\overline{PD}$ = +5V, V_{REF+} = +2.0V, V_{REF_IN} = AGND, f_{CLK} = 2.5 MHz, RS = 25Ω, C_L = 50 pF/pin. After Auto-Cal @ Temperature.
Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}: all other limits $T_A = T_J$ = 25˚C(Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
CLOCK, $\overline{RD}$, $\overline{PD}$ Digital Input Characteristics					
$V_{IN(1)}$	Logical ″1″ Input Voltage	V^+ = 5.25V		**2.0**	V(min)
$V_{IN(0)}$	Logical ″0″ Input Voltage	V^+ = 4.75V		**0.8**	V(max)
$I_{IN(1)}$	Logical ″1″ Input Current	V_{IN} = 5.0V	5		µA
$I_{IN(0)}$	Logical ″0″ Input Current	V_{IN} = 0V	−5		µA
C_{IN}	V_{IN} Input Capacitance		5		pF
CAL, RESET Digital Input Characteristics					
$V_{IN(1)}$	Logical ″1″ Input Voltage	V^+ = 5.25V		**3.5**	V(min)
$V_{IN(0)}$	Logical ″0″ Input Voltage	V^+ = 4.75V		**1.0**	V(max)
$I_{IN(1)}$	Logical ″1″ Input Current	V_{IN} = 5.0V	5		µA
$I_{IN(0)}$	Logical ″0″ Input Current	V_{IN} = 0V	−5		µA
C_{IN}	Input Capacitance		5		pF
D00 - D13 Digital Output Characteristics					
$V_{OUT(1)}$	Logical ″1″ Output Voltage	V_D I/O = 4.75V, I_{OUT} = −360 µA		**4.5**	V(min)
$V_{OUT(1)}$	Logical ″1″ Output Voltage	V_D I/O = 2.7V, I_{OUT} = −360 mA		**2.5**	V(min)
$V_{OUT(0)}$	Logical ″0″ Output Voltage	V_D I/O = 5.25V, I_{OUT} = 1.6 mA		**0.4**	V(max)
		V_D I/O = 3.3V, I_{OUT} = 1.6 µA		**0.4**	V(max)
I_{OZ}	TRI-STATE Output Current	V_{OUT} = 3V or 5V	100		nA
		V_{OUT} = 0V	−100		nA
$+I_{SC}$	Output Short Circuit Source Current	V_{OUT} = 0V, V_D I/O = 3V	−10		mA
$-I_{SC}$	Output Short Circuit Sink Current	V_{OUT} = V_D I/O = 3V	12		mA
Power Supply Characteristics					
I_A	Analog Supply Current	$\overline{PD}$ = V_D I/O	70	**85**	mA(max)
I_D	Digital Supply Current	$\overline{PD}$ = V_D I/O	7	**8**	mA(max)
I_D I/O	Output Bus Supply Current	$\overline{PD}$ = V_D I/O	1	**2**	mA(max)
	Total Power Consumption	$\overline{PD}$ = V_D I/O	390	**475**	mW(max)
		$\overline{PD}$ = DGND	<2		mW
PSRR	Power Supply Rejection Ratio	250 mV_{PP} DC to 10 MHz riding on V_A	54		dB
		½LSB Error			

AC Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, $V^+ = V_A = V_D$ = +5.0V, V_D I/O = 3.0V or 5.0V, $\overline{PD}$ = +5V, V_{REF+} = +2.0V, V_{REF_IN} = AGND, f_{CLK} = 2.5 MHz, RS = 25Ω, C_L = 50 pF/pin. After Auto-Cal @ Temperature.
Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}: all other limits $T_A = T_J$ = 25˚C(Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
f_{CLK}	Conversion Clock (CLOCK) Frequency		300		kHz(min)
			3	**2.5**	MHz(max)
	Conversion Clock Duty Cycle		45		**%(min)**
			55		**%(max)**
t_{CONV}	Conversion Latency		13		Clock Cycles
t_{AD}	Aperture Delay		9		ns

AC Electrical Characteristics (Continued)

The following specifications apply for AGND = DGND = DGND I/O = 0V, $V^+ = V_A = V_D$ = +5.0V, V_D I/O = 3.0V or 5.0V, $\overline{PD}$ = +5V, V_{REF+} = +2.0V, V_{REF_IN} = AGND, f_{CLK} = 2.5 MHz, RS = 25Ω, C_L = 50 pF/pin. After Auto-Cal @ Temperature. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}:** all other limits $T_A = T_J$ = 25˚C(Notes 7, 8, 9)

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units (Limits)
t_{OD}	Falling Edge of CLK to Data Valid		50		ns
t_{EOCL}	Falling edge of CLK to falling edge of EOC		$1/(4f_{CLK})$	**90** **130**	ns(min) ns(max)
t_{DATA_VALID}	Falling edge of CLOCK to Data Valid		$1/(8f_{CLK})$	**38** **95**	ns(min) ns(max)
t_{AD}	Aperture Delay		9		ns
t_{ON}	$\overline{RD}$ low to data valid on D00 -D13		23	**33**	ns(max)
t_{OFF}	$\overline{RD}$ high to D00 -D13 in TRI-STATE		25	**33**	ns(max)
t_{CAL}	Calibration Time		110		ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND I/O = 0V, unless otherwise specified.

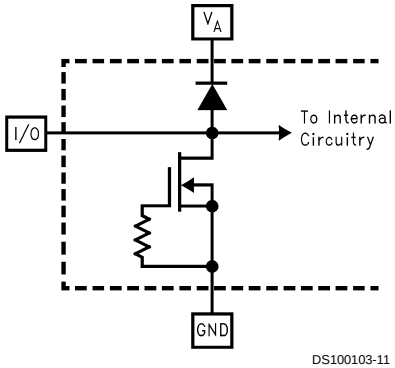
Note 3: When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150˚C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. In the 52-pin TQFP, θ_{JA} is 70˚C/W, so P_DMAX = 1,785 mW at 25˚C and 1,142 mW at the maximum operating ambient temperature of 70˚C. Note that the power dissipation of this device under normal operation will typically be about 410 mW (390 mW quiescent power + 20 mW due to 1 TTL load on each digital output. The values for maximum power dissipation listed above will be reached only when the ADC14061 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

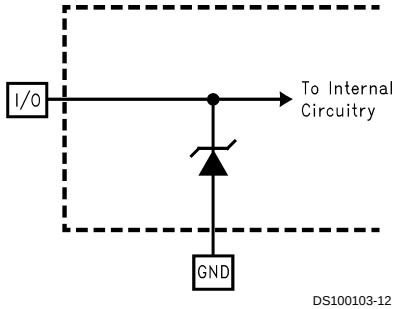
Note 5: Human body model is 100 pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220 pF discharged through ZERO Ω.

Note 6: See AN450, ″Surface Mounting Methods and Their Effect on Product Reliability″, or the section entitled ″Surface Mount″ found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The inputs are protected as shown below. Input voltage magnitudes up to 5V above V_A or to 5V below GND will not damage this device, provided current is limited per Note 3. However, errors in the A/D conversion can occur if the input goes above V_A or below GND by more than 100 mV. As an example, if V_A is 4.75 V_{DC}, the full-cale input voltage must be ≤4.85V_{DC} to ensure accurate conversions



ESD Protection Scheme for Digital Input pins



ESD Protection Scheme for Analog Input and Digital Output pins

Note 8: To guarantee accuracy, it is required that V_A and V_D be connected together and to the same power supply with separate bypass capacitors at each V^+ pin.

Note 9: With the test condition for V_{REF} = (V_{REF}+ − V_{REF}−) given as +2.0V, the 14-bit LSB is 122 µV.

Note 10: Typical figures are at $T_A = T_J$ = 25˚C, and represent most likely parametric norms.

Note 11: Tested limits are guaranteed to Nationsl's AOQL (Average Outgoing Quality Level).

Note 12: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and negative full-scale.

Note 13: Timing specifications are tested at the TTL logic levels, V_{IL} = 0.4V for a falling edge and V_{IH} = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 14: Optimum SNR performance will be obtained by keeping the reference input in the 1.8V to 2.2V range. The LM4041CIM3-ADJ (SOT-23 package), the LM4041CIZ-ADJ (TO-92 package), or the LM4041CIM-ADJ (SO-8 package) bandgap voltage reference is recommended for this application.

AC Electrical Characteristics (Continued)

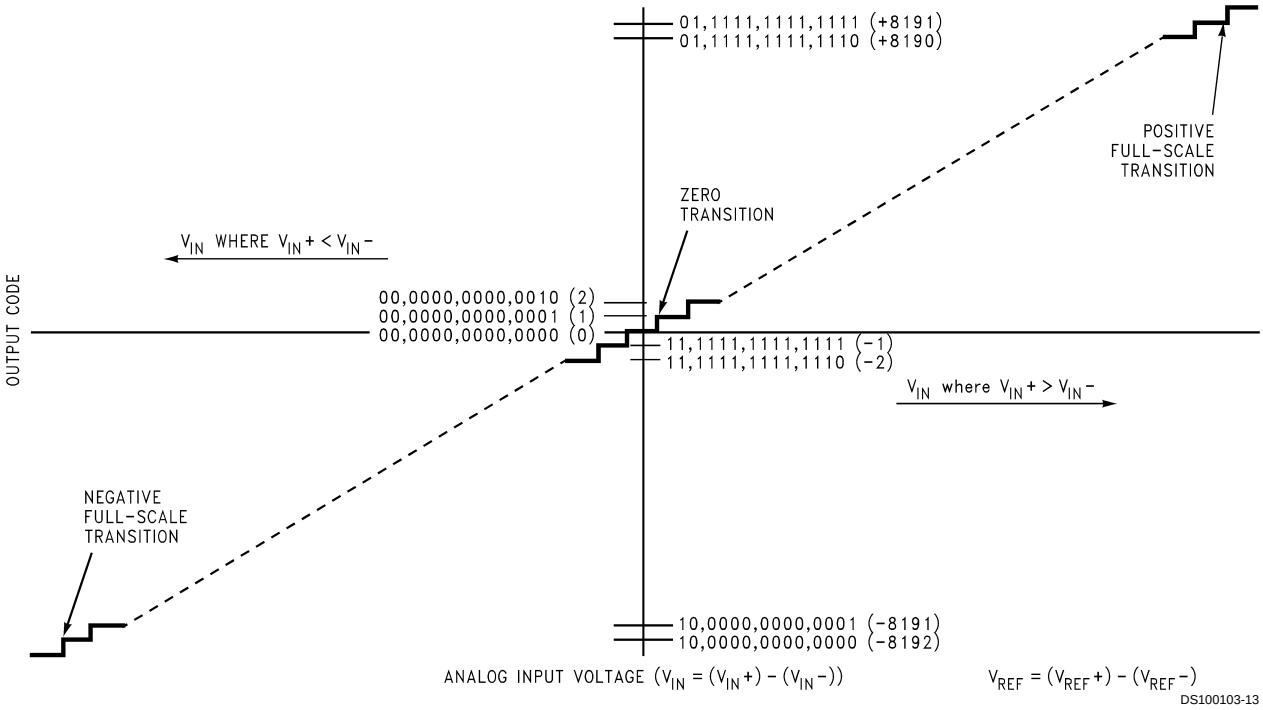


FIGURE 1. Transfer Characteristics

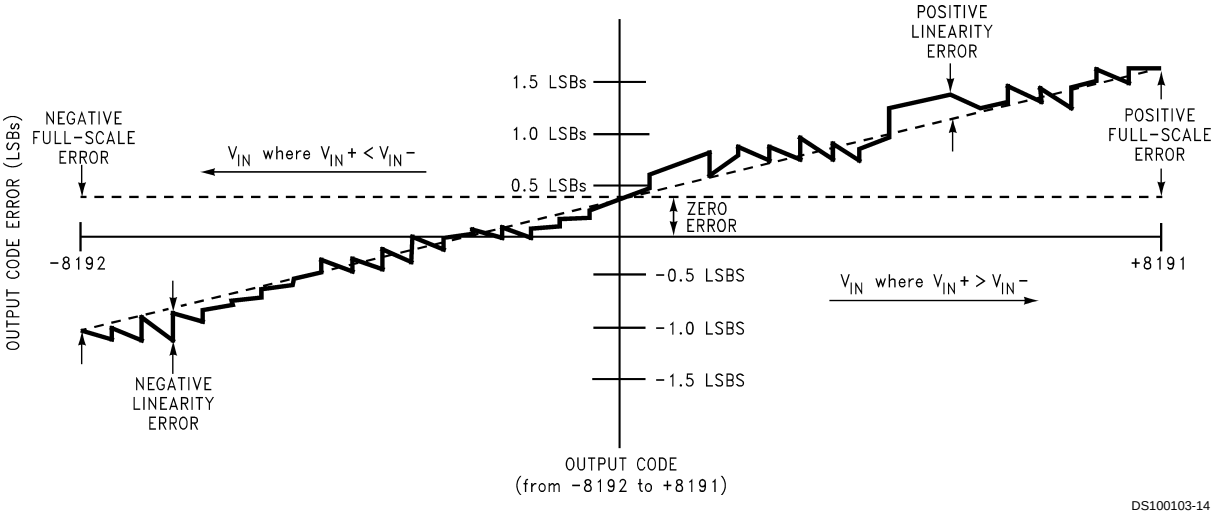
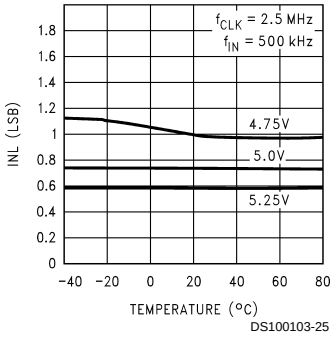


FIGURE 2. Errors removed by Auto-Cal cycle

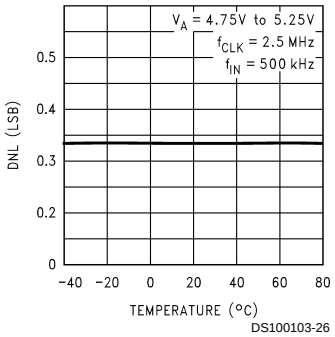
Typical Performance Characteristics

INL vs Temperature



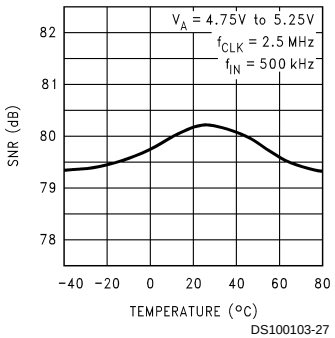
DS100103-25

DNL vs Temperature



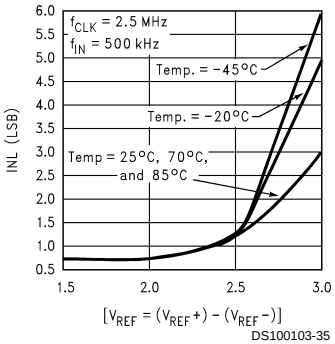
DS100103-26

SNR vs Temperature



DS100103-27

INL vs V_{REF} and Temperature



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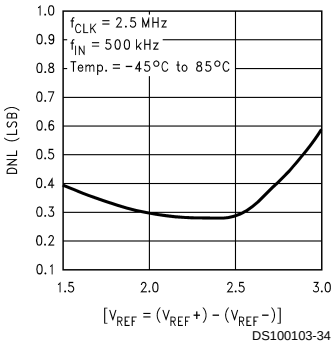
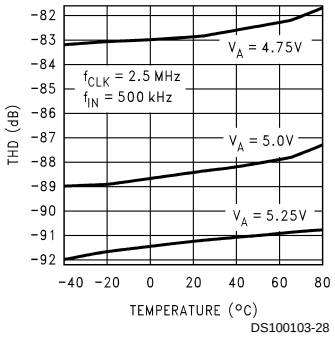
DNL vs V_{REF}



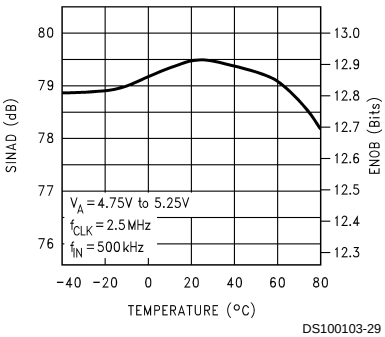
DS100103-34

THD vs Temperaure



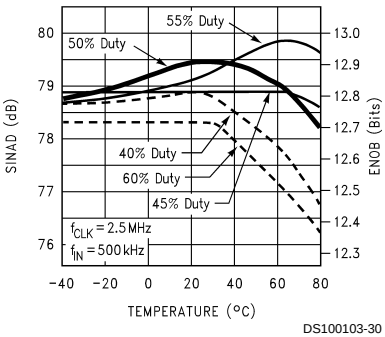
DS100103-28

SINAD & ENOB vs Temperature



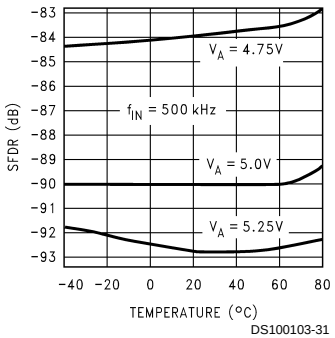
DS100103-29

SINAD & ENOB vs Clock Duty Cycle



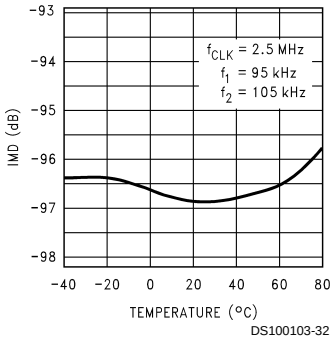
DS100103-30

SFDR vs Temperature



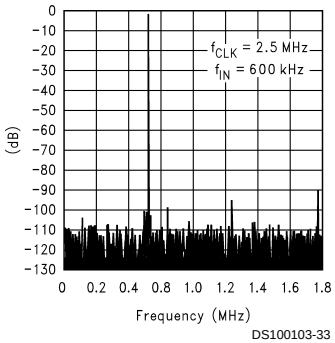
DS100103-31

IMD



DS100103-32

Spectral Response



DS100103-33

Specification Definitions

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

APERTURE DELAY is the time required after the falling edge of the clock for the sampling switch to open. In other words, for the Track/Hold circuit to go from ″track″ mode into the ″hold″ mode. The Track/Hold circuit effectively stops capturing the input signal and goes into the ″hold″ mode t_{AD} after the fall of the clock.

OFFSET ERROR is the difference between the ideal LSB transition to the actual transition point. The LSB transition should occur when $V_{IN}+ = V_{IN}-$.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD −1.76) / 6.02.

FULL SCALE ERROR is the difference between the input voltage $[(V_{IN}+) - (V_{IN}-)]$ just causing a transition to positive full scale and V_{REF} − 1.5 LSB, where V_{REF} is $(V_{REF}+_{IN}) - (V_{REF}-_{IN})$.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with f_{IN} equal to 100 kHz plus integral multiples of f_{CLK}. The input frequency at which the output is −3 dB relative to the low frequency input signal is the full power bandwidth.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in the original frequencies. IMD is usually expressed in dB.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output stage. Data for any given sample is available the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

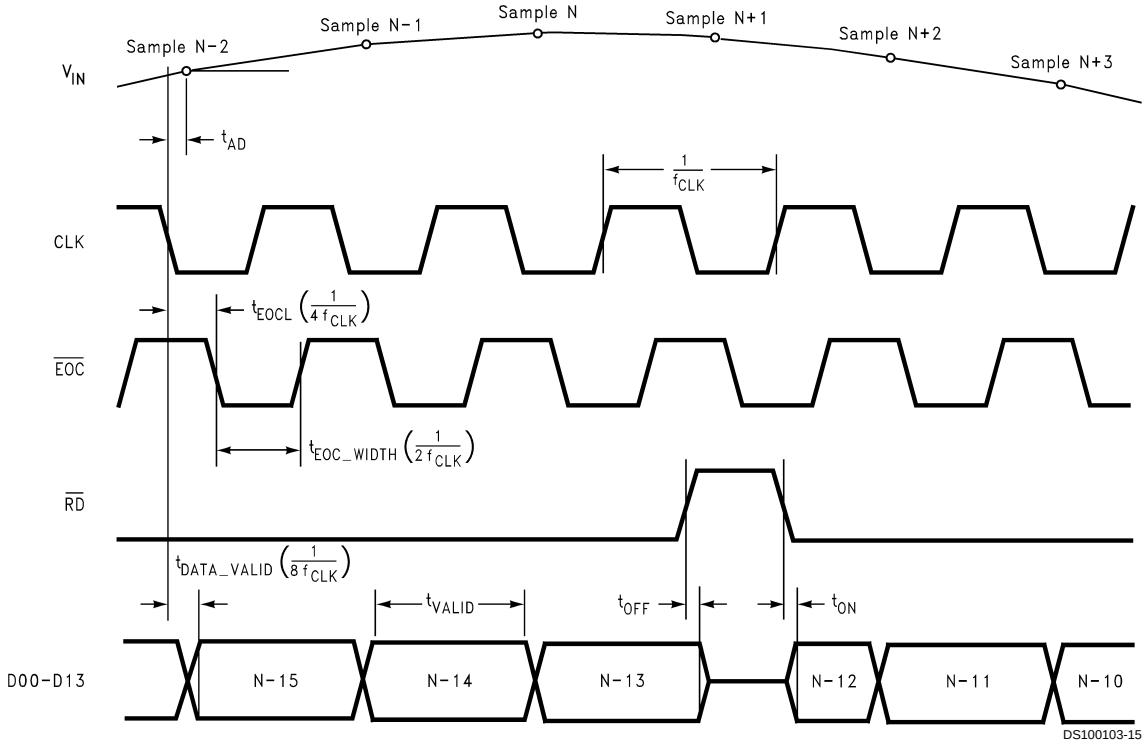
SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD)) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

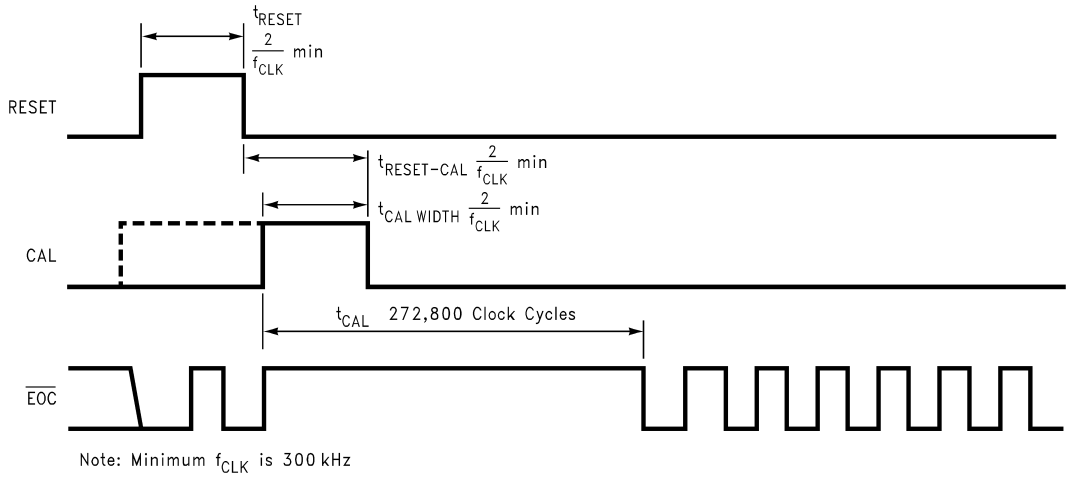
TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first six harmonic components, to the rms value of the input signal.

Timing Diagrams



TIMING DIAGRAM 1. Output Timing

Timing Diagrams (Continued)



TIMING DIAGRAM 2. Reset and Calibration

Functional Description

Operating on a single +5V supply, the ADC14061 uses a pipelined architecture and has error correction circuitry and a calibration mode to help ensure maximum performance at all times.

Balanced analog signals with a peak-to-peak voltage equal to the input reference voltage, V_{REF}, and centered around the common mode input voltage, V_{CM}, are digitized to 14 bits (13 bits plus sign). Neglecting offsets, positive input signal voltages ($V_{IN}+ - V_{IN}- > 0$) produce positive digital output data and negative input signal voltages ($V_{IN}+ - V_{IN}- < 0$) produce negative output data. The input signal can be digitized at any clock rate between 300 Ksps and 2.5 Msps.

Input voltages below the negative full scale value will cause the output word to take on the negative full scale value of 10,0000,0000,0000. Input voltage above the positive full scale value will cause the output word to take on the positive full scale value of 01,1111,1111,1111.

The output word rate is the same as the clock frequency. The analog input voltage is acquired at the falling edge of the clock and the digital data for that sample is delayed by the pipeline for 13 clock cycles plus t_{DATA_VALID}. The digital output is undefined if the chip is being reset or is in the calibration mode. The output signal may be inhibited by the $\overline{RD}$ pin while the converter is in one of these modes.

The $\overline{RD}$ pin must be low to enable the digital outputs. A logic low on the power down ($\overline{PD}$) pin reduces the converter power consumption to less than two milliwatts.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC14061:

$4.75V \le V_A \le 5.25V$

$5.25V \le V_D \le 5.25V$

$3.0V \le V_D$ I/O $\le$ VD

$0.3MHz \le f_{CLK} \le 2.5$ MHz

V_{CM} = 2.0V (forced)

$V_{REF\ IN}+$ = 2.0V

$V_{REF\ IN}-$= AGND

1.1 The Analog Inputs

The ADC14061 has two analog signal inputs, $V_{IN}+$ and $V_{IN}-$. These two pins form a balanced signal input. There are two reference pins, $V_{REF}+_{\ IN}$ and $V_{REF}-_{\ IN}$. These pins form a fully differential input reference.

1.2 Reference Inputs

$V_{REF}+_{\ IN}$ should always be more positive than $V_{REF}-_{\ IN}$. The effective reference voltage, V_{REF}, is the difference between these two voltages:

$$V_{REF} = (V_{REF}+_{\ IN}) - (V_{REF}-_{\ IN}).$$

The operational voltage range of $V_{REF}+_{\ IN}$ is +1.8 Volts to +3.0 Volts. The operational voltage range of $V_{REF}-_{\ IN}$ is ground to 1.0V. For best performance, the difference between $V_{REF}+_{\ IN}$ and $V_{REF}-_{\ IN}$ should remain within the range of 1.8V to 2.2V. Reducing the reference voltage below 1.8V will decrease the signal-to-noise ratio (SNR) of the ADC14061. Increasing the reference voltage (and, consequently, the input signal swing) above 2.2V will increase THD.

$V_{REF\ (MID)}$ is the reference mid-point and is derived from V_{CM}. This point is brought out only to be by passed. By pass this pin with 0.1µF capacitor to ground. Do not load this pin.

It is very important that all grounds associated with the reference voltage make connection to the analog ground plane at a single point to minimize the effects of noise currents in the gound path.

1.3 Signal Inputs

The signal inputs are $V_{IN}+$ and $V_{IN}-$. The signal input, V_{IN}, is defined as

$$V_{IN} = (V_{IN}+) - (V_{IN}-).$$

Figure 3 indicates the relationship between the input voltage and the reference voltages. *Figure 4* shows the expected input signal range.

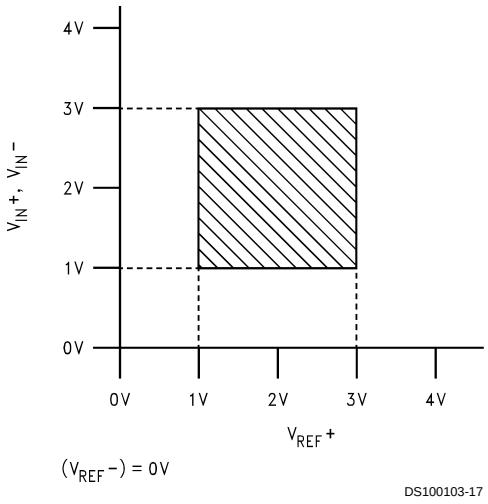


FIGURE 3. Typical Input to Reference Relationaship.

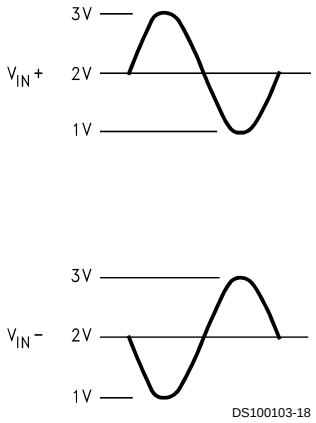


FIGURE 4. Expected Input Signal Range.

The ADC14061 performs best with a balanced input centered around V_{CM}. The peak-to-peak voltage swing at either $V_{IN}+$ or $V_{IN}-$ should be less than the reference voltage and each signal input pin should be centered on the V_{CM} voltage. The two V_{CM}-centered input signals should be exactly 180° out of phase from each other. As a simple check to ensure this, be certain that the average voltage at the ADC iinput pins is equal to V_{CM}. Drive the analog inputs with a source impedance less than 100 Ohms.

Applications Information (Continued)

The sign bit of the output word will be a logic low when V_{IN}+ is greater than V_{IN}− . When V_{IN}+ is less than V_{IN}−, the sign bit of the output word will be a logic high.

For single ended operation, one of the analog inputs should be connected to V_{CM}. However, SNR and SINAD are reduced by about 12dB with a single ended input as compared with differential inputs.

An input voltage of V_{IN} = (V_{IN}+) − (V_{IN}−) = 0 will be interpreted as mid-scale and will thus be converted to 00,0000,0000,0000, plus any offset error.

The V_{IN}+ and the V_{IN}− inputs of the ADC14061 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 12 pF when the clock is low, and 28 pF when the clock is high. It is recommended that the ADC14061 be driven with a low impedance source of 100 Ohms or less.

A simple application circuit is shown in *Figure 6* and *Figure 7*. Here we use two LM6172 dual amplifiers to provide a balanced input to the ADC14061. Note that better noise performance is achieved when V_{REF}+ $_{IN}$ voltage is forced with a well-bypassed resistive divider. The resulting offset and offset drift is minimal.

Since a dynamic capacitance is more difficult to drive than is a fixed capacitance, choose driving amplifiers carefully. The CLC427, CLC440, LM6152, LM6154, LM6172, LM6181 and LM6182 are excellent amplifiers for driving the ADC14061.

1.4 V_{CM} Analog Inputs

The V_{CM} input of the ADC14061 is internally biased to 40% of the V_A supply with on-chip resistors, as shown in *Figure 5*. The V_{CM} pin must be bypassed to prevent any power supply noise from modulating this voltage. Modulation of the V_{CM} potential will result in the introduction of noise into the input signal. The advantage of simply bypassing V_{CM} (without driving it) is the circuit simplicity. On the other hand, if the V_A supply can vary for any reason, V_{CM} will also vary at a rate and amplitude related to the RC filter created by the bypass capacitor and the internal divider resistors. However, performance of this approach will be adequate for many applications.

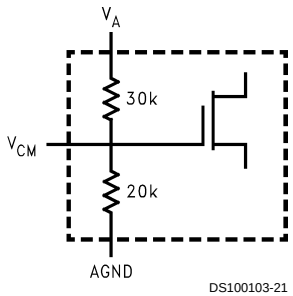


FIGURE 5. V_{CM} input to the ADC14061 V_{CM} is set to 40% of V_A with on-chip resistors. Performance is improved when V_{CM} is driven with a stable, low impedance source

By forcing V_{CM} to a fixed potential, you can avoid the problems mentioned above. One such approach is to buffer the 2.0 Volt reference voltage to drive the V_{CM} input, holding it at a constant potential as shown in *Figure 6* and *Figure 8*. If the reference voltage is different from the desired V_{CM}, that desired V_{CM} voltage may be derived from the reference or from another stable source.

Note that the buffer used for this purpose should be a slow, low noise amplifier. The LMC660, LMC662, LMC272 and LMC7101 are good choices for driving the V_{CM} pin of the ADC14061.

If it is desired to use a multiplexer at the analog input, that multiplexer should be switched at the rising edge of the clock signal.

2.0 DIGITAL INPUTS

Digital Inputs consist of CLOCK, RESET, CAL, $\overline{RD}$ and $\overline{PD}$. All digital input pins should remain stable from the fall of the clock until 30ns after the fall of the clock to minimize digital noise corruption of the input signal on the die.

2.1 The CLOCK signal drives an internal phase delay loop to create timing for the ADC. Drive the clock input with a stable, low phase jitter clock signal in the range of 300 kHz to 2.5 MHz. The trace carrying the clock signal should be as short as possible. This trace should not cross any other signal line, analog or digital, not even at 90˚.

The CLOCK signal also drives the internal state machine. If the clock is interrupted, the data within the pipeline could become corrupted.

A 100 Ohm damping resistor should be placed in series with the CLOCK pin to prevent signal undershoot at that input.

2.2 The RESET input is level sensitive and must be pulsed high for at least two clock cycles to reset the ADC after power-up and before calibration (See Timing Diagram 2).

2.3 The CAL input is level sensitive and must be pulsed high for at least two clock cycles to begin ADC calibration (See Timing Diagram 2). Reset the ADC14061 before calibrating. Re-calibrate after the temperature has changed by more than 50˚C since the last calibration was performed and after return from power down.

During calibration, use the same clock frequency that will be used for conversions to avoid excessive offset errors.

Calibration takes 272,800 clock cycles. Irrelevant data may appear at the data outputs during RESET or CAL and for 13 clock cycles thereafter. Calibration should not be started until the reference outputs have settled (100mS with 1µF capacitors on these outputs) after power up or coming out of the power down mode.

2.4 $\overline{RD}$ pin is used to READ the conversion data. When the $\overline{RD}$ pin is low, the output buffers go into the active state. When the $\overline{RD}$ input is high, the output buffers are in the high impedance state.

2.5 The $\overline{PD}$ pin, when low, holds the ADC14061 in a power-down mode where power consumption is typically less than 2mW to conserve power when the converter is not being used. The ADC14061 will begin normal operation within t_{WU} after this pin is brought high, provided a valid CLOCK input is present. Power dissipation during shut-down is not affected by the clock frequency, or by whether there is a clock signal present. The data in the pipeline is corrupted while in the power down mode. The ADC14061 should be reset and calibrated upon returning to normal operation after a power down.

3.0 OUTPUTS

The ADC14061 has four analog outputs: V_{REF}+ $_{OUT}$, V_{REF}− $_{OUT}$, $V_{REF\ (MID)}$ and V_{CM} .There are 15 digital outputs: EOC (End of Conversion) and 14 Data Output pins.

Applications Information (Continued)

3.1 The reference output voltages are made available only for the purpose of bypassing with capacitors. These pins should not be loaded with more than 10 µA DC. These output voltages are described as

$$V_{REF}+ \text{ OUT} = V_{CM} + \tfrac{1}{2}V_{REF}$$

$$V_{REF}- \text{ OUT} = V_{CM} - \tfrac{1}{2}V_{REF}$$

where $V_{REF} = (V_{REF}+ \text{ IN}) - (V_{REF}+ \text{ IN})$

$$V_{REF\ (MID)} = (V_{REF}+ \text{ OUT} + V_{REF}- \text{ OUT}) / 2.$$

To avoid signal clipping and distortion, $V_{REF}+$ OUT should not exceed 3.3V, $V_{REF}-$ OUT should not be below 750 mV and V_{CM} should be held in the range of 1.8V to 2.2V.

3.2 The /EOC output goes low to indicate the presence of valid data at the output data lines. Valid data is present the entire time that this signal is low except during reset. Corrupt or irrelevant data may appear at the data outputs when the RESET pin or the CAL pin is high.

3.3 The Data Outputs are TTL/CMOS compatible. The output data format is two's complement. Valid data is present at these outputs while the $\overline{EOC}$ pin is low. While the t_{EOCL} time and the t_{DATA_VALID} time provide information about output timing, a simple way to capture a valid output is to latch the data on the rising edge of the CLOCK (pin 10).

Also helpful in minimizing noise due to output switching is to minimize the load currents at the digital outputs. This can be done by connecting buffers between the ADC outputs and any other circuitry. Only one input should be connected to each output pin. Additionally, inserting series resistors of 47 or 56 Ohms at the digital outputs, close to the ADC pins, will isolate the outputs from other circuitry and limit output currents. (See *Figure 6*).

4.0 POWER SUPPLY CONSIDERATIONS

Each power supply pin should be bypassed with a parallel combination of a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. The chip capacitors should be within ½ centimeter of the power pins. Leadless chip capacitors are preferred because they provide low lead inductance.

While a single 5V source is used for the analog and digital supplies of the ADC14061, these supply pins should be well isolated from each other to prevent any digital noise from being coupled to the analog power pins. Supply isolation with ferrite beads is shown in *Figure 6* and *Figure 8*.

As is the case with all high-speed converters, the ADC14061 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 100 mV_{P-P}.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even at power up.

The V_D I/O provides power for the output drivers and may be operated from a supply in the range of 3.0V to the V_D supply (nominal 5V). This can simplify interfacing to 3.0 Volt devices and systems. Powering V_D I/O from 3 Volts will also reduce power consumption and noise generation due to output switching. **DO NOT operate the V_D I/O at a voltage higher than V_D or V_A.**

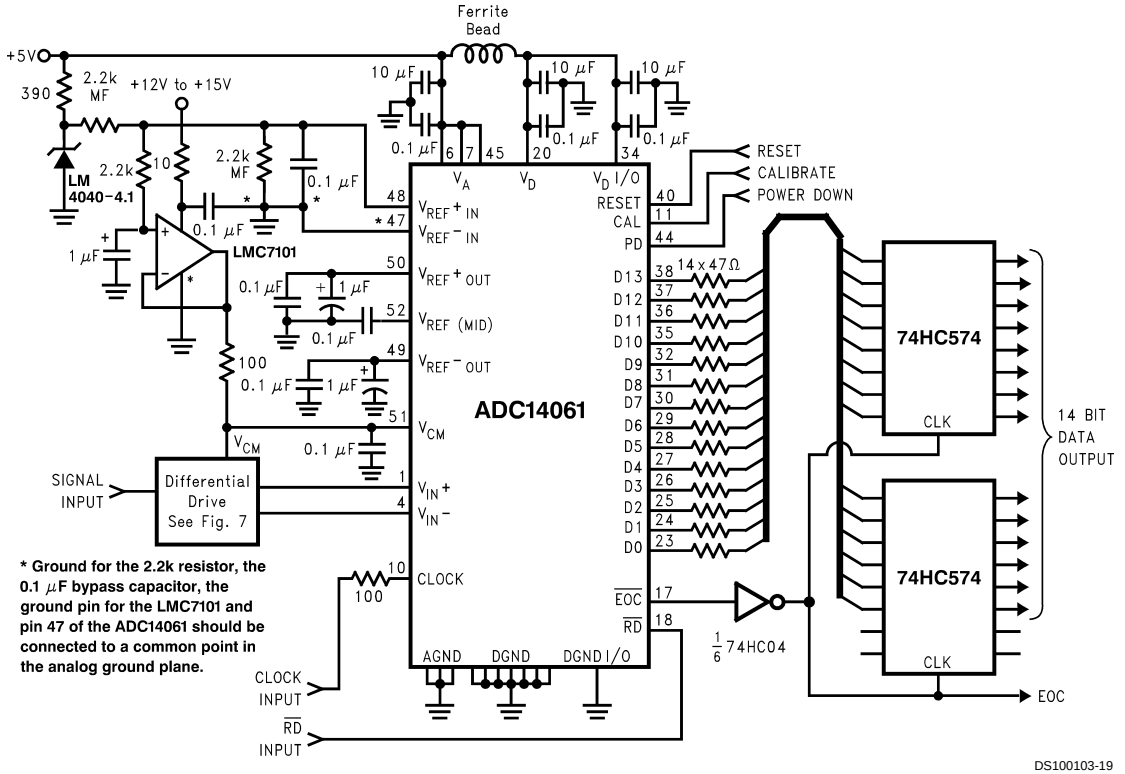


FIGURE 6. Simple application circuit with single-ended to differential buffer.

Applications Information (Continued)

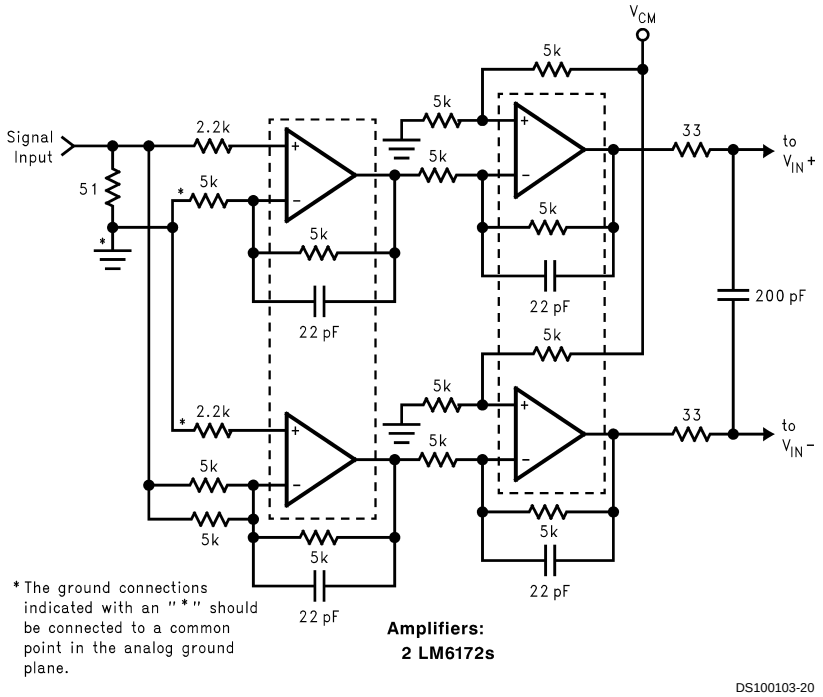


FIGURE 7. Differential drive circuit of *Figure 6*. All 5k resistors are 0.1%. Tolerance of the other resistors is not critical.

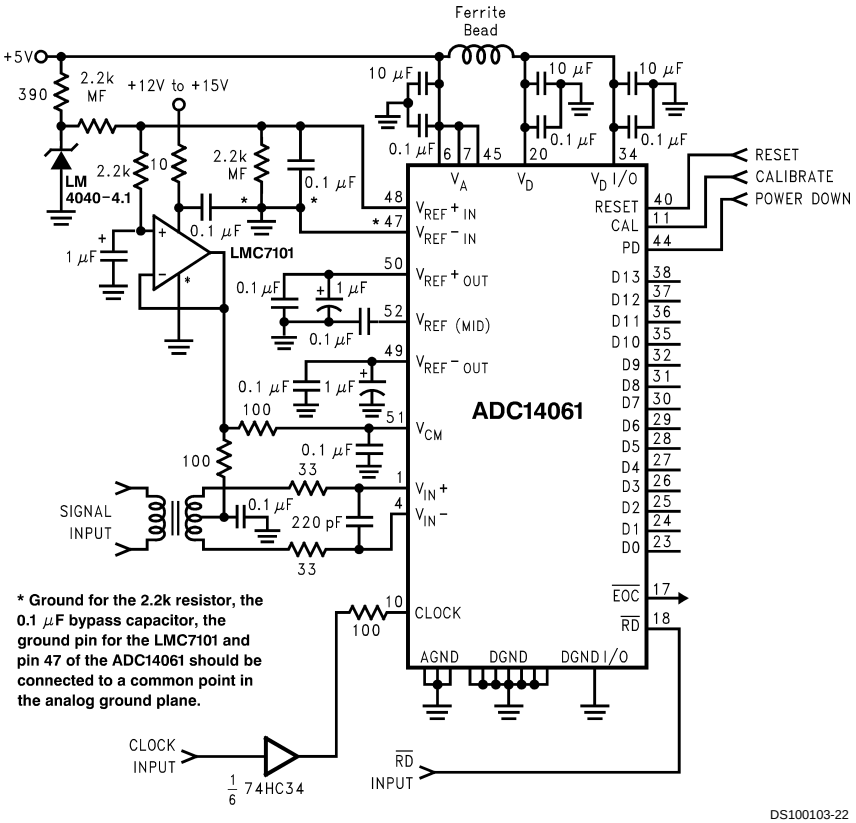


FIGURE 8. Driving the signal inputs with a transformer.

Applications Information (Continued)

5.0 LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. Separate analog and digital ground planes that are connected beneath the ADC14061 are required to achieve specified performance. The analog and digital grounds may be in the same layer, but should be separated from each other and should never overlap each other. Separation should be at least ⅛ inch, where possible.

The ground return for the digital supply (DGND I/O) carries the ground current for the output drivers. This output current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DGND I/O pin should **NOT** be connected in close proximity to any of the ADC14061's ground pins.

Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry separated from the digital circuitry and from the digital ground plane.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by connecting the analog and digital ground planes together beneath the ADC with a copper trace that is very narrow compared with the rest of the ground plane. A typical width is 3/16 inch (4 to 5 mm).This narrowing beneath the converter provides a fairly high impedance to the high frequency components of the digital switching currents, directing them away from the analog pins. The relatively lower frequency analog ground currents see a relatively low impedance across this narrow ground connection.

Generally, analog and digital lines should cross each other at 90 degrees to avoid getting digital noise into the analog path. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep any clock lines isolated from ALL other lines, including other digital lines. Even the generally accepted 90 degree crossing should be avoided as even a little coupling can cause problems at high frequencies. This is because other lines can introduce phase noise (jitter) into the clock line, which can lead to degradation of SNR.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side, even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane.

Figure 9 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed on or over the analog ground plane. All digital circuitry and I/O lines should be placed over the digital ground plane.

All ground connections should have a low inductance path to ground.

Applications Information (Continued)

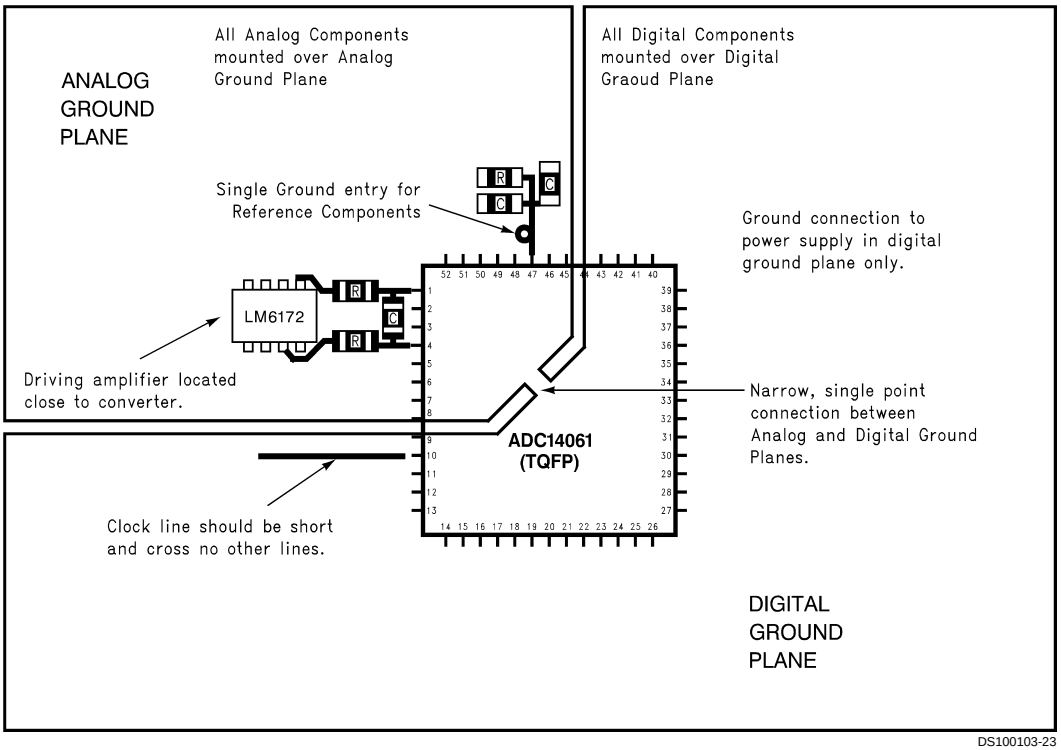


FIGURE 9. Example at a suitable layout.

6.0 DYNAMIC PERFORMANCE

The ADC14061 can achieve impressive dynamic performance. To achieve the best dynamic performance with the ADC14061, the clock source driving the CLK input must be free of jitter. For best ac performance, isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in *Figure 10*.

As mentioned in section 5.0, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce phase noise (jitter) into the clock signal, which can lead to increased distortion. Even lines with 90˚ crossings have capacitive coupling, so try to avoid even these 90˚ crossings of the clock line.

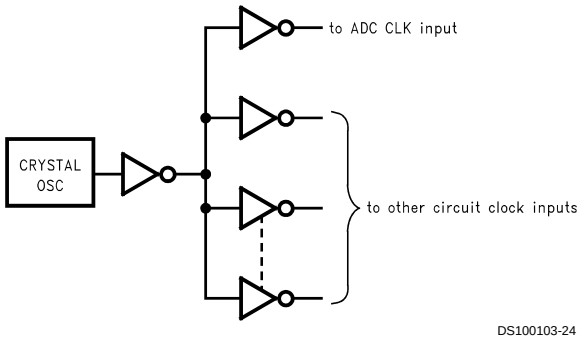


FIGURE 10. Isolating the ADC clock from other circuitry with a clock tree.

7.0 COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A resistor of about 50 to 100Ω in series with the offending digital input will eliminate the problem.

Do not allow input voltages to exceed the supply voltage during power up.

Be careful not to overdrive the inputs of the ADC14061 with a device that is powered from supplies outside the range of the ADC14061 supply. Such practice may lead to conversion inaccuracies and even to device damage.

Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through V_D I/O and DGND I/O. These large charging current spikes can couple into the analog circuitry of the ADC14061, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem. The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC14061, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 47Ω.

Using an inadequate amplifier to drive the analog input. As explained in Section 1.3, the capacitance seen at the in-

Applications Information (Continued)

put alternates between 12 pF and 28 pF, depending upon the phase of the clock. This dynamic loaad is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. Amplifiers that have been used sucessfully to dirve the analog inputs of the ADC14061 include the CLC427, CLC440, LM6152, LM6154, LM6181 and the LM6182. A small series reistor at each amplifier output and a capacitor across the analog inputs (as shown in *Figure 7*) will often improve performance.

Operating with the reference pins outside of the specified range. As mentioned in section 1.2, V_{REF} should be in the range of

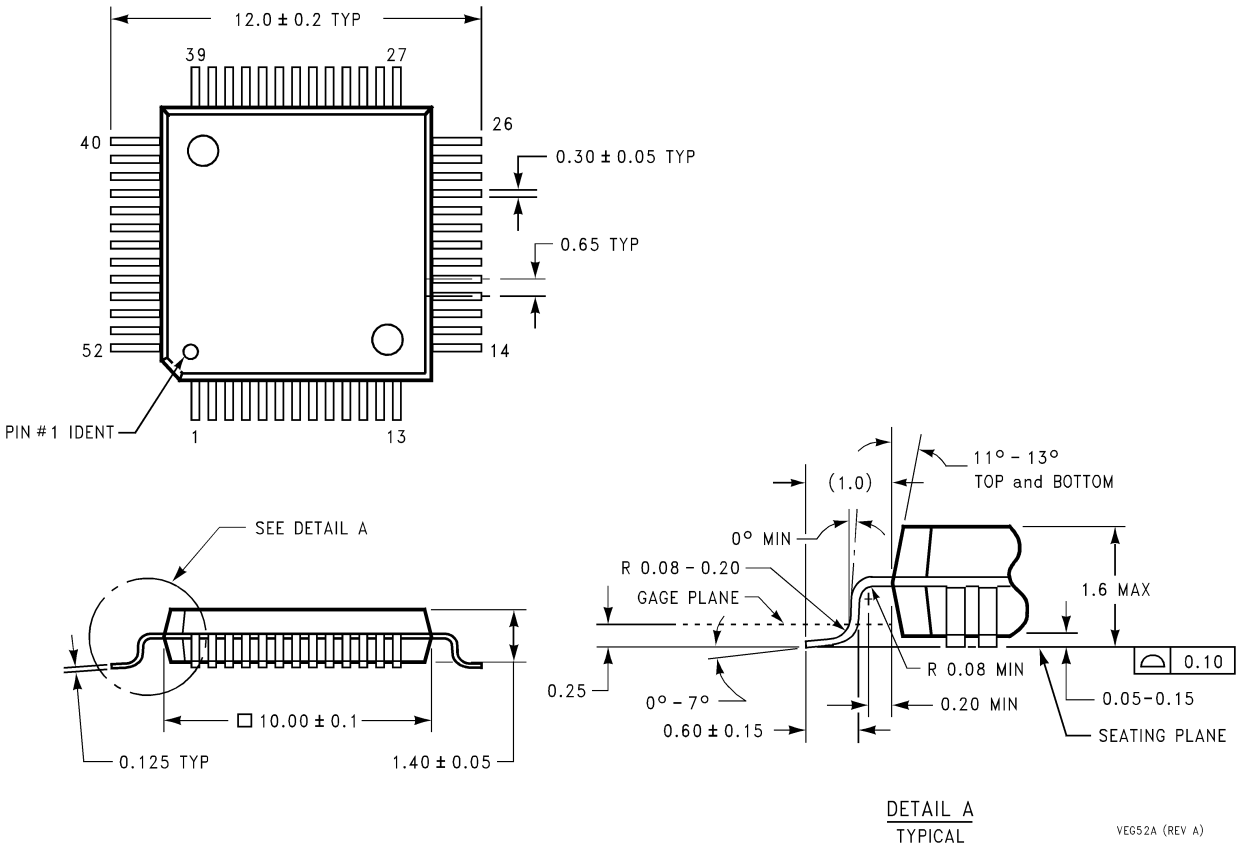
$$1.8V \leq V_{REF} \leq 2.2V$$

with $V_{REF}- _{IN} \leq 1.0V$. Operating outside of these limits could lead to signal distortion.

Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Connecting pins marked ″NC″ to any potential. Some of these pins are used for factory testing. They should all be left floating. Connecting them to ground, power supply, or some other voltage could result in a non-functional device.

Physical Dimensions inches (millimeters) unless otherwise noted



52-Lead Thin Quad Flat Pack
Ordering Information Package ADC14061CCVT
NS Package Number VEG52A

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