National Hybrid, Inc.

Mil-Std-1553/1760

Remote Terminal Products

User's Manual

Version 3.2
April 1996

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1.0 SCOPE

This document defines the functional and electrical specification for National Hybrid's series of MIL-STD-1553B Remote Terminals (NHI-RT).

2.0 APPLICABLE DOCUMENTS

MIL-STD-1553B, NOTICES I, II
MIL-STD-1760A, NOTICES I, II, III
EFA/STANAG-3838

3.0 INTRODUCTION

The NHI-RT is an intelligent interface between a dual redundant MIL-STD-1553B bus and a host bus. The device contains two +5V transceivers, a single protocol chip, and an 8K byte RAM. All the 1553 protocol as well as the RAM control and arbitration logic are contained in the protocol chip. The NHI-RT implements all MIL-STD-1553B requirements and options for Remote Terminals. The only external components required are 2 coupling transformers. Since the Remote Terminal manages the 1553B protocol autonomously, host overhead is reduced to an absolute minimum.

The NHI-RT appears to the host computer as 4K words of 16 bit-wide memory controlled by standard RAM signals. The device can thus be easily interfaced with all popular processors and buses.

3.1 FEATURES

The NHI-RT implements the following features:

- Contains two +5 volt only transceivers.
- Has onboard memory of 4K words by 16 bits wide.
- Complies with all MIL-STD-1553B Notice I and II requirements and options.
- Complies with MIL-STD-1760A Notices I, II, and III.
- Complies with EFA/STANAG-3838 requirements for Eurofighter Aircraft.
- Interfaces with a dual redundant 1553 bus.
- Accesses data tables via pointers residing in RAM which facilitates multiple buffering (buffers can be changed without moving data) and promotes efficient use of RAM space (data tables can have programmable sizes and locations).
- Message Illegality is internally programmable. DOES NOT require external PROMS or glue logic.
- Employs data tables with individual tag words which indicate whether or not the data is valid, updated since last read, in the process of being updated, was received via broadcast command, or has been lost (i.e., updated more than once by a receive message before being read).

- Watchdog timer inhibits encoder if continuous transmission exceeds 768 microseconds.

- Optionally sets the subsystem flag bit whenever stale data is transmitted or received data is overwritten.

- Issues interrupts to the host for any subset of subaddresses and mode commands.

- Stores interrupt vectors in a 4 word deep FIFO.

- Built-in interrupt controller.

- Provides interrupt priority input and output pins for daisy-chaining interrupt requests.

- Includes a 32 bit real-time clock with programmable resolution for tagging receive, transmit, and mode code messages.

- Optionally resets the real-time clock in response to a "Synchronize" mode command.

- Optionally updates the lower 16 bits of the real-time clock in response to a "Synchronize With Data" command.

- Interfaces with an 8 bit discrete I/O bus.

- Indicates the reception of specific commands by outputting pulses on any one of 8 pins.

- Internally loops-back messages under host control for test purposes.

- Employs a decoder algorithm which ensures high noise immunity and a low error rate (word error rate typically less than 10^{-9} for 1553 noise test).

- Operates from 10 Mhz clock.

- Low power CMOS technology.

- Single 5 volt supply.

- Low total power consumption.

3.2 BLOCK DIAGRAM

A functional block diagram is shown in Figure 1. The NHI-RTs contains two +5 volt transceivers, an ASIC, and an 8K x 8 SRAM. The ASIC performs all 1553 protocol functions and controls accesses to the RAM such that it appears to the host CPU as a 4K x 16 dual port memory. Although the RAM chip is only 8 bits wide, this is transparent to the user because the ASIC executes two fast RAM accesses for every 16 bit wide host access.

Since the NHI-RT appears to its host as RAM, no external logic is required when interfacing to the device. It is simply connected to the CPU's address bus, data bus, and control lines. There are NO EPROMS required to illegalize commands. Illegalization is performed internal to the protocol

chip in the NHI-RT. The user sets up command illegalization when the NHI-RT is initialized. See sections on Message Illegalization and Host Initialization.

The NHI-RT can be interfaced to an 8 bit data bus by folding the upper and lower bytes on top of each other and performing byte wide data transfers.

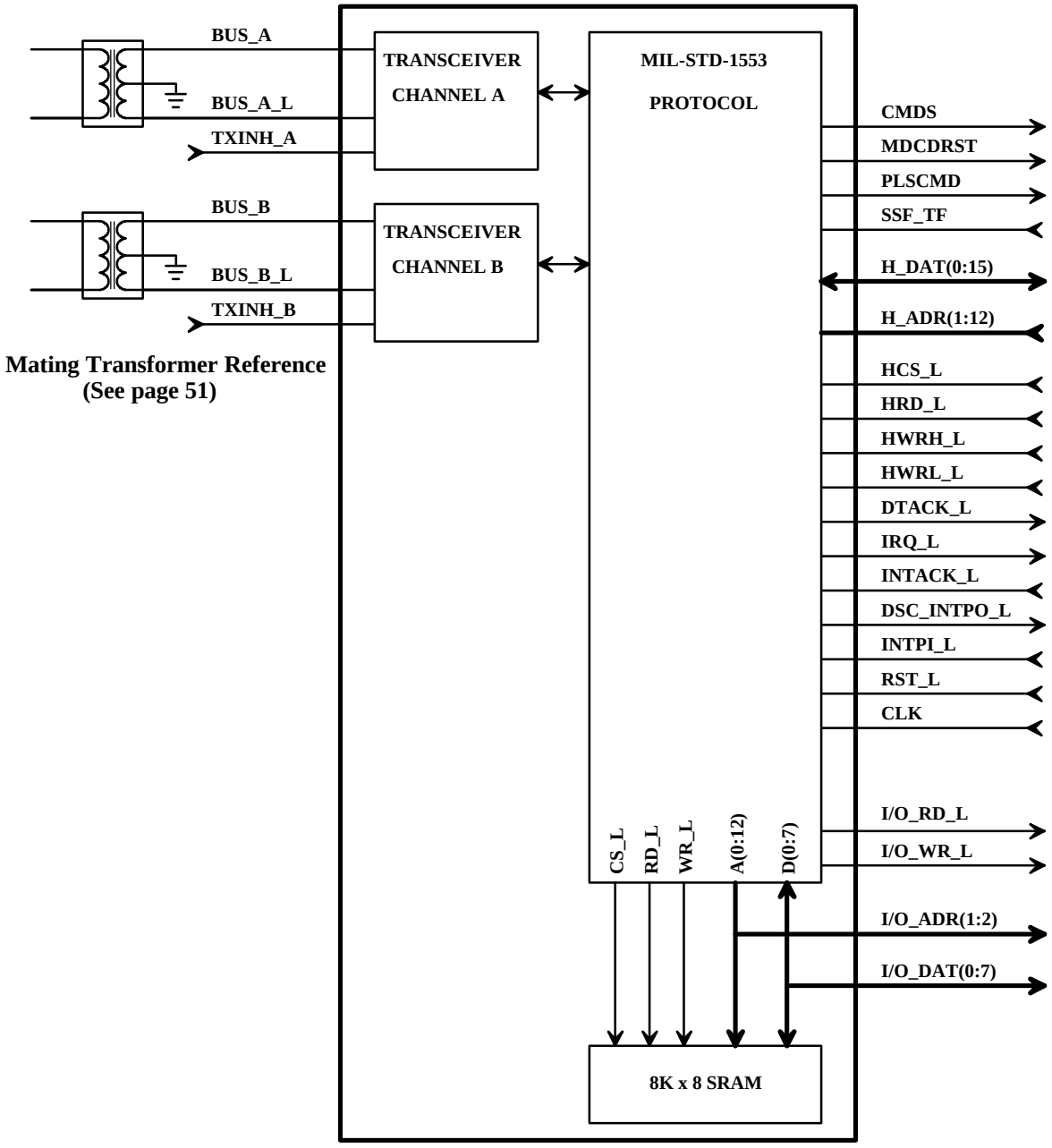


FIGURE 1: NHI REMOTE TERMINAL FUNCTIONAL BLOCK DIAGRAM

3.3 PROTOCOL CHIP DESCRIPTION

The protocol chip contains the following modules:

- Host Bus Interface Unit (HBIU)
- I/O Bus Interface Unit (IBIU)
- Interrupt Controller Unit (ICU)
- Dual Redundant 1553 Front End (DRFE)
- Message Processor Unit (MPU)

3.3.1 HOST BUS INTERFACE UNIT

The HBIU provides a standard RAM interface to the host bus. The module performs the following functions:

- Provides NHI-RT device select and decodes host address to select registers.
- Transfers data between the NHI-RT and the host (word and byte mode as well as read-modify-write are supported).
- Provides priority input and output for daisy chaining host interrupts.
- Outputs *DTACK signal indicating end of bus cycle.

3.3.2 I/O BUS INTERFACE UNIT

The IBIU controls the RAM and I/O residing on the I/O bus so that it appears to the host as a pseudo dual port RAM (i.e., shared memory). The unit implements the following functions:

- Arbitrates between host and protocol chip initiated accesses to the RAM and host data bus.
- Decodes address lines to select device (e.g. RAM, external byte-wide I/O, external terminal address buffer, command output register).
- Generates control signals to access the selected device.

By default, the host has priority in accessing the I/O bus. When the host requests access to a device already in use by the protocol chip, the host *DTACK (*READY) signal is delayed by the NHI-RT. If either side (protocol chip or host) waits for access during the current cycle, it is automatically granted priority for the next cycle. The host can retain priority for successive cycles accessing the same address (this is required to guarantee the proper operation of host read-modify-write instructions - see pin *HCS for details) by keeping *HCS low.

3.3.3 INTERRUPT CONTROL UNIT

The ICU is a 6 input vectored interrupt controller. It contains four registers as well as a FIFO for storing pending interrupt vectors.

3.3.3.1 ICU REGISTERS

The ICU contains the following registers:

INTERRUPT REQUEST register (IRR)

INTERRUPT MASK register (IMR)

INTERRUPT VECTOR register (IVR)

AUXILIARY VECTOR register (AVR)

The INTERRUPT REQUEST register samples 6 inputs originating from internal modules. Since the host can write to this register, all interrupt sequences can be software driven for program debugging. The inputs and their priorities (level 7 has highest priority) are as follows:

PRIORITY	INTERRUPT INPUT
0	END of VALID TX/RX MESSAGE
1	INVALID DATA or EXTRA WORD in TX/RX MESSAGE
2	END of VALID MODE MESSAGE
3	INVALID DATA or EXTRA WORD in MODE MESSAGE
4	FIFO OVERFLOW
5	N/A
6	N/A
7	TIMEOUT

During normal operation, 1553 messages can never cause 2 simultaneous interrupt requests. As soon as an interrupt is requested, its vector is pushed onto the FIFO - so the chronological order of the requests normally determines the order in which they will be serviced. Simultaneous requests can be generated in 2 ways:

- by the host setting at least 2 bits in the INTERRUPT REQUEST register
- by a transmission timeout on one bus together with an interrupt generated by the second bus

In the above 2 cases, the order of the vectors in the FIFO is determined by the interrupt priority.

The INTERRUPT MASK register masks the corresponding inputs to the INTERRUPT REQUEST register.

The INTERRUPT VECTOR register holds the 3 bit interrupt priority level and an additional 5 bit programmable displacement field (see paragraph on INTERRUPT VECTOR register for details).

The AUXILIARY VECTOR register contains an additional byte of information related to the interrupt request (see paragraph on AUXILIARY VECTOR register for details).

3.3.3.2 ICU FIFO

The ICU FIFO is 10 bits wide and 4 words deep. Whenever an unmasked interrupt request is issued by the message processor, a word is pushed onto the FIFO. When an interrupt is acknowledged by the host, a word is popped from the FIFO and used to update the 3 bit interrupt level in the IVR and the 7 least significant bits in the AVR.

The host can read the FIFO by simply popping its contents. This is done by reading the FIFO located at address 8 (refer to address map). The interrupt request output, *IRQ, will go inactive after the FIFO is emptied in this way.

The host can mask the *IRQ output by resetting the INTERRUPT REQUEST ENABLE bit in the CONTROL register; however this does not prevent the device from pushing interrupt requests onto the FIFO.

If an interrupt request occurs when the FIFO is full, a vector indicating FIFO overflow is first pushed onto the FIFO and then the vector which caused the overflow is pushed onto the FIFO. As a result, the 2 oldest vectors are lost. All further pushes are then inhibited until the host pops the vector indicating the overflow.

The above mechanism ensures that the host will always be notified of FIFO overflows and will always obtain the 2 interrupt vectors immediately preceding the overflow condition.

The FIFO can be emptied by writing (any value) to address 8 (in words).

3.3.4 DUAL REDUNDANT 1553 FRONT END

The DRFE performs serial to parallel and parallel to serial conversion as well as basic format and timing validation. The unit contains the following:

- Two Manchester decoders
- Manchester encoder
- Gap counter
- No response counter
- Minimum response time counter
- Timeout counter

3.3.4.1 MANCHESTER DECODER

The decoder translates serial Manchester bi-phase signals to 16-bit words and outputs the following signals:

- Valid command word received
- Valid data word received
- Invalid word received (parity, incorrect bit count, invalid Manchester encoding, gap)

- Broadcast command received

- Begin new message (i.e., end of a valid legal command for this Remote Terminal)

3.3.4.2 MANCHESTER ENCODER

The encoder receives 16 bit words and transmits them with the appropriate sync and parity as a serial Manchester bi-phase signal. The outputs of the encoder can be loop-backed into either decoder for test purposes.

3.3.4.3 GAP COUNTER.

The gap counter checks contiguity of successive words. If the time between "contiguous" words (measured from zero-cross of parity to zero-cross of sync) exceeds 3.5 - 3.7 microseconds, the message is invalidated.

3.3.4.4 NO RESPONSE COUNTER

The no response counter checks the response time of the transmitting RT in a RT to RT transfer. If the response time is exceeded, the message is invalidated. The response time is software programmable (14, 18, 26, 42 microseconds) to accommodate systems with long cables and/or slow terminals.

3.3.4.5 MINIMUM RESPONSE TIME COUNTER

The minimum response time counter ensures that the response will be no sooner than 6 microseconds (measured from zero-cross of parity to zero-cross of sync).

3.3.4.6 TIMEOUT COUNTER

This counter inhibits the encoder outputs and issues a TIMEOUT interrupt whenever continuous transmission exceeds 768 microseconds. Transmission will remain inhibited until a command is received on the same bus.

3.3.5 MESSAGE PROCESSOR UNIT

The MPU forms the heart of the protocol chip and controls the operation of the Dual Decoder, Encoder, and Interrupt Controller. This unit is activated by the reception of a valid legal command addressed to the RT.

The MPU performs the following functions:

- Recognizes the various message types (transmit, receive, RT-RT, mode, broadcast) and responds with the appropriate sequence of control signals.

- Validates format and timing of received data words.

- Checks command legality.

- Responds with status/data.

- Calculates all data bus addresses for accessing the RAM and discrete I/O.

- Updates RAM data table contents, including tag words.
- Optionally time tags data tables.
- Issues interrupt requests to the ICU.

If the host and RT do not contend while the RT prepares the status for transmission, the maximum response time is 7.0 microseconds (measured from zero-cross to zero-cross). During the preparation of the status, the RT only performs one access which can potentially contend with the host; thus, the response time is delayed by at most the width of a single host access (see pin *HCS for details).

3.4 HARDWIRE TERMINAL ADDRESS

The terminal address of the NHI-RT can be hardwired using I/O DAT(5:0). I/O DAT(4:0) are used for the terminal address, I/O DAT0 being the LSB, and I/O DAT5 is used to set odd parity in the address. These pins CANNOT be directly connected to +5 or ground since the I/O data bus drives the NHI-RT's internal RAM. The address must be wired using pull-up and pull-down resistors. There are 64K internal pull-up resistors in the protocol chip, so only external pull-down resistors of 4.7K are required. The Hardwire Address is read and loaded into the terminal at Power-On Reset, Hardware Reset, Software Reset, and receipt of Mode Code Reset. See section on NHI-RT Initialization.

The terminal address can be changed at any time through software by writing a new address to the Basic Status Register, however, if any of the above resets occur, the Hardwire Address will be re-loaded into the terminal.

4.0 DATA STRUCTURE

4.1 ADDRESS MAP

The NHI-RT appears to the host as 4K words of memory divided into the following blocks:

Address Range	Description
0 - 29	Internal Control and Status registers
30	External RT address / Command output pins
31	I/O tag word
32 - 35	I/O space (accessed on the Discrete I/O bus)
64 - 4095	Shared RAM (accessed on the Host I/O bus)

The following table defines all addresses relevant to the user.

ADDRESS	CONTENTS/OPERATION	R/W
0	CONTROL REGISTER	R/W
1	POINTER TABLE ADDRESS REGISTER	R/W
2	BASIC STATUS REGISTER	R/W
3	IMR (lower byte)	R/W
3	IVR (upper byte)	R
3	IRR (upper byte)	W
4	IVR (lower byte)	R/W
4	AVR (upper byte)	R
5	RTC_HIGH	R
6	RTC_LOW	R
7	RTC CONTROL REGISTER	R/W
8	FIFO READ	R
8	FIFO RESET (both bytes)	W
11	LAST COMMAND REGISTER	R
12	LAST STATUS REGISTER	R
15	RESET RT (both bytes)	W
18	ENCODER STATUS REGISTE	R
19	CONDITION REGISTER	R
23	ENCODER DATA REGISTER	R/W*
24	ENCODER DATA TX REQUEST (both bytes)	W*
25	ENCODER CMD TX REQUEST (both bytes)	W*
30	EXTERNAL RT ADR BUFFER (lower byte)	R
30	COMMAND OUTPUT PINS	W
31	I/O TAG REGISTER	R/W

* In order to write to addresses 23, 24, or 25, the RT must be in loop-back mode (see CONTROL register for details).

4.2 INTERNAL REGISTERS

4.2.1 CONTROL REGISTER

This register controls the general operation of the NHI-RT. After Power-On-Reset (POR), the bits MIO and NTAG are set to 1 and all other bits are reset to 0.

15	14	13	12	11	10	9	8
HWD	**RSP1**	**RSP0**	**POL**	**NBCST**	**TXINH**	**LOOPB**	**LOOPA**

7	6	5	4	3	2	1	0
IRE	**MIO**	**CMDO**	**SRQRST**	**SSF_TF**	**NTAG**	**BINH**	**AINH**

HWD

HWD=1 enables high word detection.

This option allows words to be invalidated when bus activity is detected instead of a gap (e.g.: extra bits/words following a transmit command or the last data word in a receive message).

RSP0, RSP1
These bits define the response timeout for RT-RT messages as follows:

RSP1	RSP0	Timeout
0	0	14 uSec
0	1	18 uSec
1	0	26 uSec
1	1	42 uSec

POL
This bit must always remain equal to 0.

NBCST
NBCST=1 specifies that broadcast commands should be ignored.

TXINH
TXINH=1 inhibits transmission by forcing TXA=TXAN=0 and TXB=TXBN=0.

LOOPA(B)
LOOPA(B)=1 defines that decoder A (B) inputs shall be connected internally to the encoder outputs rather than the 1553 transceiver for test purposes.

IRE
IRE=1 enables the interrupt request output, *IRQ.
IRE=0 disables all interrupt requests; however, interrupt vectors are still pushed onto the FIFO.

MIO
MIO=1 defines that certain reserved mode commands with data shall be legal and access the I/O bus without dependence on host initialization or the BUSY bit in the BASIC STATUS register. This feature can be used, for example, to set a watchdog timer or read a hardware status register via the 1553 bus even though the host's state may be undefined.

The I/O operations are restricted to the data word's lower byte. The mode commands and their corresponding I/O addresses are as follows:

T/R	MODE CODE (Decimal)	I/O ADR(2,1)	*I/O WR	*I/O RD
T	24	00	1	0
T	25	10	1	0
R	27	10	0	1
R	28	00	0	1

CMDO
CMDO=0 Specifies that after a legal valid command is received, a pulse shall be outputted on a pin specified by the PULSE field in the corresponding data table tag word. The pulse is activated together with 2 I/O control signals (CMDS=1 and *I/O WR = 0).

CMDO=1 Specifies that after a valid legal command is received, the word count/mode code field (together with CMDS=1 and *I/O WR = 0) shall be outputted on the 5 least significant bits of the discrete I/O bus. (Although the protocol chip outputs the entire command, only 5 bits are outputted by the NHI-RT due to pin-out restrictions).

SRQRST
SRQRST=1 specifies that the service request bit in the STATUS register will be reset upon reception of a valid "Transmit Vector Word" mode command.

SSF_TF (Signal not available on all NHI-RTs, see device outlines in section 9.0)
SSF_TF=0 specifies that the sub-system flag in the 1553 status word will be determined by the value of the SSF_TF pin.

SSF_TF=1 specifies that the terminal flag in the 1553 status word will be determined by the value of the SSF_TF pin.

NTAG
NTAG=1 specifies that all the data tables shall be without tag words. This mode of operation can be used to store received data from several subaddresses into a contiguous block without interspersed tag words. This feature can facilitate, for example, software upload.

BINH
BINH=1 disables reception on bus B.

AINH
AINH=1 disables reception on bus A.

4.2.2 POINTER TABLE ADDRESS REGISTER

This register holds the address of the table of pointers used by the NHI-RT when accessing data tables. The address is specified as a word address from the start of the 4K word memory space. After POR the register is initialized with the value 1000 (hex).

4.2.3 BASIC STATUS REGISTER

This register defines the terminal address as well as default values for all status bits. The 1553 status word is OR'ed with this register before transmission. The bits in the BASIC STATUS register correspond to the bits in the STATUS register and their function is defined in MIL-STD-1553B.

15	14	13	12	11	10	9	8
TADR4	TADR3	TADR2	TADR1	TADR0	ME	INSTR	SREQ

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	BCR	BUSY	SSF	DBCA	TF

The mechanism employed by the protocol chip for initializing the terminal address is designed to avoid dedicated pins. Upon POR the terminal address and its parity are automatically read from address 30 on the I/O bus. The value can be supplied in 2 ways: by enabling the output of an external terminal address buffer or by employing pull-up/down resistors to define a default value for the 6 least significant bits of the I/O data bus. Odd parity is used to define a valid terminal address; even parity will inhibit reception on both buses. After POR, the host can change the terminal address through software by writing to the TADR field with any desired value. In addition, this operation will enable reception.

The host can check the validity of the parity bit obtained from the I/O bus by reading address 30; if the most significant bit in the lower byte equals 1, the parity is invalid.

If the TADR is not defined externally (by pull-down resistors or a buffer), there is no danger of a false response before host initialization because internal pull-up resistors on the I/O bus guarantee an incorrect terminal address parity.

When BUSY=1, 1553 message accesses to the RAM are inhibited, however the RT will respond with status as required by MIL-STD-1553B. The mode commands "Transmit Status Word", "Transmit Last Command Word", "Reset Remote Terminal", "Transmitter Shutdown", "Override Transmitter Shutdown" and the reserved mode commands legalized by MIO (see the CONTROL register for details) are not affected by BUSY. In addition, all output pulses issued after valid command reception are inhibited when BUSY=1 (except for the signal MDCDRST which is pulsed after receiving the mode command "Reset").

After POR, BUSY is set to "1"; this prevents the RT from using undefined pointers before the host has had a chance to initialize the POINTER TABLE. The default value for all other status bits is "0" and the TADR field is loaded with the hardwired address. The *RST pin, "Reset" mode command, and writing to the reset address will each have the same effect on this register as POR (see initialization section).

The BUSY Bit in the LAST STATUS REGISTER is cleared on receipt of the first command after any RESET, except if that command is TRANSMIT LAST STATUS or TRANSMIT LAST COMMAND mode command.

4.2.4 INTERRUPT REQUEST REGISTER

7	6	5	4	3	2	1	0
IREQ7	X	X	IREQ4	IREQ3	IREQ2	IREQ1	IREQ0

The INTERRUPT REQUEST register holds 6 types of interrupt requests (see section on INTERRUPT CONTROL UNIT for details). Interrupt requests are active high and upon POR the register is cleared (see initialization section).

4.2.5 INTERRUPT MASK REGISTER

7	6	5	4	3	2	1	0
IMSK7	X	X	IMSK4	IMSK3	IMSK2	IMSK1	IMSK0

The INTERRUPT MASK register masks the corresponding inputs to the INTERRUPT REQUEST register; the bits mask when high. Upon POR, all interrupts are masked (see initialization section).

4.2.6 INTERRUPT VECTOR REGISTER

7	6	5	4	3	2	1	0
D	D	D	D	D	L	L	L

The INTERRUPT VECTOR register holds the interrupt priority (LLL) determined by the message processor and a host programmable 5 bit displacement DDDDD. The LLL field is popped from the FIFO and latched into the IVR during the interrupt acknowledge cycle or whenever the FIFO is popped by a host read instruction. Upon POR, this register is undefined.

4.2.7 AUXILIARY VECTOR REGISTER

This register contains additional information related to the interrupt request. The lower 7 bits are popped from the FIFO and latched into the AVR during the interrupt acknowledge cycle or whenever the FIFO is popped by a host read instruction to address 8. Upon POR, this register is undefined.

7	6	5	4	3	2	1	0
EMP	BUS	T/R	SADR/ MODE(4)	SADR/ MODE(3)	SADR/ MODE(2)	SADR/ MODE(1)	SADR/ MODE(0)

EMP
EMP=1 Indicates that the FIFO is empty. This bit can be used to poll for interrupt requests.

BUS
BUS=0 (1) Indicates that the message was on bus A (B).

T/R
T/R=0 (1) indicates a receive (transmit) message.

SADR / MODE

This field defines the sub-address or mode code (Note: the interrupt level distinguishes between regular transmit/receive commands and mode commands).

4.2.8 REAL-TIME CLOCK

The RTC is a 32 bit up-counter which can be used for time-tagging transmit, receive, and mode code messages. If the time-tagging option (as defined by the data table pointer words) is in effect, the RTC is sampled immediately after command reception and stored in the 2 words following the data table tag word. The most significant word is stored first.

When transmit messages are time-tagged, the host should not write to the first 2 locations following the data table tag word since they will be overwritten with the value of the transmitted RTC. In the case of mode commands, the RTC will not be sent, however, it will still be stored in the data table.

The RTC can be reset by the mode command "Synchronize Without Data" and the least significant 16 bits can be updated by "Synchronize With Data". In order to increase the accuracy of the update, two corrections are added to the received data before it is stored into the RTC. The first correction equals the delay from the end of the mode command to the write operation which updates the RTC, and the second correction equals a constant (see OFST field of RTC CONTROL register for details) to compensate for the bus propagation delay.

The RTC can be read and reset by the host at any time. Since the RTC consists of 32 bits, at least 2 memory cycles are required to read all of its value. As a result, a carry-out from the lower word can occur between the read cycles. A mechanism is therefore provided to solve this potential difficulty.

If the host reads the RTC as two 16 bit words, *LOCK should be initialized to 1 in the RTC CONTROL register. In this case, when the host reads the upper word, all 32 bits are latched into the host output register. The value in the output register remains unchanged until the host finishes reading the lower word of the RTC.

If the host reads the RTC in bytes, *LOCK should be initialized to 0. In this case, when the host reads any of the bytes of the RTC, all 32 bits are latched into the host output register and its value remains unchanged until updating is re-enabled by reading the RTC CONTROL register. The RTC resolution can be programmed equal to 1, 4, 16 or 64 microseconds.

4.2.8.1 RTC CONTROL REGISTER

The RTC is controlled by the RTC CONTROL register which has the following format:

15	14	13	12	11	10	9	8
RTCRST	0	0	SYNUPD	*LOCK	SYNRST	RES	RES
7	6	5	4	3	2	1	0
M1760	OFST	OFST	0	0	0	0	0

NOTE: Bits 14, 13, 4-0 must all equal "0".

RTCRST
When a "1" is written to RTCRST, a reset pulse is issued to the RTC. The contents of the register are not affected by this operation and RTCRST is always read by the host as "0".

SYNUPD
SYNUPD=1 specifies that the lower 16 bits of the RTC will be updated whenever a valid mode command "Synchronize With Data" is received by the RT.

***LOCK**

*LOCK=0 enables updating of the host output register after the RTC CONTROL register is read (this feature is needed to support byte wide read cycles).

*LOCK=1 enables updating of the host output register after the lower RTC word is read.

SYNRST
SYNRST=1 specifies that the RTC shall be reset whenever a valid mode command "Synchronize Without Data" is received by the RT.

RES
This field defines the resolution of the RTC as follows:

Resolution	Microseconds
00	1
01	4
10	16
11	64

M1760
M1760=1 specifies that the RT shall comply with MIL-STD-1760A. This mode of operation has 2 consequences: first, the mode command "Synchronize With Data" updates the lower 16 bits of the RTC only if the least significant data bit is "0" and second, the IPO_DSC pin serves as a store disconnect signal rather than an interrupt priority output.

OFST
This field defines an offset which is added to the RTC whenever it is updated by the mode command "Synchronize With Data". The offset can be used to automatically compensate for bus propagation delays. The value of the offset depends on the RTC's resolution as defined below:

OFST	Microseconds
00	0 x RTC resolution
01	1 x RTC resolution
10	2 x RTC resolution
11	3 x RTC resolution

All bits in this register are cleared during initialization of the RT.

4.2.9 FIFO READ

This address is used to read the contents of the interrupt FIFO. Reading this address pops the FIFO and updates the IVR and the AVR.

4.2.10 FIFO RESET

Writing (any value) to this address empties the FIFO.

4.2.11 LAST COMMAND REGISTER

This register holds the last command word as defined by MIL-STD-1553B. The contents are not defined after initialization of the RT.

4.2.12 LAST STATUS REGISTER

This register holds the last status word as defined by MIL-STD-1553B. After initialization of the RT, the BUSY bit=1, the TADR field contains the hardwire address, and all other bits are set to 0.

4.2.13 RESET REMOTE TERMINAL

Writing a word to address 15 resets the RT and causes it to perform its initialization (see initialization section).

4.2.14 ENCODER STATUS

This register contains flags indicating the status of the encoder. These flags are intended to facilitate transmission of messages in loop-back mode during self-test.

15	14-8	7	6-0
*TXREQ	X	*EOTX	X

***TXREQ**

*TXREQ=0 indicates that the encoder is ready to accept the next word for transmission. This bit should equal "0" before loading the encoder with the next word. In order to transmit contiguous words, the next word should be loaded within 18 microseconds after *TXREQ transitions to "0".

***EOTX**

*EOTX=0 indicates that the encoder has completed transmission and that there are no pending requests.

4.2.15 CONDITION REGISTER

This register contains information about the command being processed by the NHI-RT. It also reports if the terminal flag is enabled and if the transmitters for bus "A" and bus "B" are enabled.

15	14	13	12	11	10	9	8-0
X	X	AXEN	BXEN	TFE	X	*MDCD	X

X = NOT USED

AXEN

AXEN=1 indicates that transmitter A is enabled. This bit is set to a "1": at POWER UP, if the NHI-RT is RESET, after receipt of a "Reset" mode code, or after receipt of an "Override Transmitter Shutdown" mode code on the B bus.

AXEN=0 indicates that transmitter A is inhibited. This bit is set to a "0" after receipt of a "Transmitter Shutdown" mode code on the B bus.

BXEN

BXEN=1 indicates that transmitter B is enabled. This bit is set to a "1": at POWER UP, if the NHI-RT is RESET, after receipt of a "Reset" mode code, or after receipt of an "Override Transmitter Shutdown" mode code on the A bus.

BXEN=0 indicates that transmitter B is inhibited. This bit is set to a "0" after receipt of a "Transmitter Shutdown" mode code on the A bus.

TFE

TFE=1 indicates that the TERMINAL FLAG bit in the status word can be set to a "1" through software via the BASIC STATUS REGISTER or by the TERMINAL FLAG pin on the NHI-RT. This bit is set to a "1": at POWER UP, if the NHI-RT is RESET, after receipt of a "Reset" mode code, or after receipt of an "Override Inhibit Terminal Flag" mode code.

TFE=0 indicates that the TERMINAL FLAG bit in the status word CANNOT be set to a "1". This bit is set to a "0" after receipt of an "Inhibit Terminal Flag" mode code.

***MDCD**

*MDCD=1 indicates that the last command received was NOT a mode code.

*MDCD=0 This bit is set to a "0" when a mode code is received.

4.2.16 ENCODER DATA REGISTER

This register contains data to be transmitted when performing a loop back test.

4.2.17 ENCODER DATA TRANSMIT REQUEST

Writing (any value) to this address causes the contents of the ENCODER DATA REGISTER to be sent as a data word. This instruction together with the ENCODER COMMAND TRANSMIT REQUEST can be used to loop-back entire messages for self-test purposes. The received data can be read from the data table associated with the command.

4.2.18 ENCODER COMMAND TRANSMIT REQUEST

Writing (any value) to this address causes the contents of the ENCODER DATA REGISTER to be sent as a command word. This instruction is useful for sending commands to the decoder while in loop-back mode. The command can then be read from the LAST COMMAND register.

4.2.19 EXTERNAL TERMINAL ADDRESS BUFFER

15-8	7	6	5	4-0
X	INVALP	DISCONN	TADRP	TADR

The terminal address may be hardwired using I/O DAT(5:0). External pull-down resistors of 4.7K are used to set a low, 64K internal pull-ups set a high. I/O DAT5 is wired for odd parity in the address. The hardwire terminal address and its parity can be obtained by reading I/O address 30. This address is unique since a read operation activates both the I/O bus command strobe and the I/O bus read signal (i.e., CMDS=1 and *I/O RD=0). As a result, a buffer containing the terminal address can be selected without decoding address lines. If an external buffer is not desired, pull-up/down resistors on the I/O data bus can be used instead (see BASIC STATUS register for details). The protocol chip also calculates the terminal address's parity and compares it to the value obtained from the I/O bus.

INVALP

INVALP=1 specifies that the terminal address which was read automatically by the protocol chip following reset (from I/O address 30) had invalid parity

DISCONN

DISCONN=0 specifies that the store is disconnected because a terminal address of 31 was detected on the I/O bus for at least 800 nanoseconds.

DISCONN=1 specifies that the store is connected.

This bit indicates the "disconnected store" condition defined by MIL-STD-1760A, provided that the store contains the pull-down resistors used for defining the terminal address (see BASIC STATUS register for details). After the store is disconnected, the standby state of all I/O lines will be high and will therefore define an illegal terminal address of 31.

TADRP

TADRP equals the value of the terminal address parity read from I/O address 30.

TADR

TADR equals the value of the terminal address read from I/O address 30.

4.2.20 COMMAND OUTPUT PINS

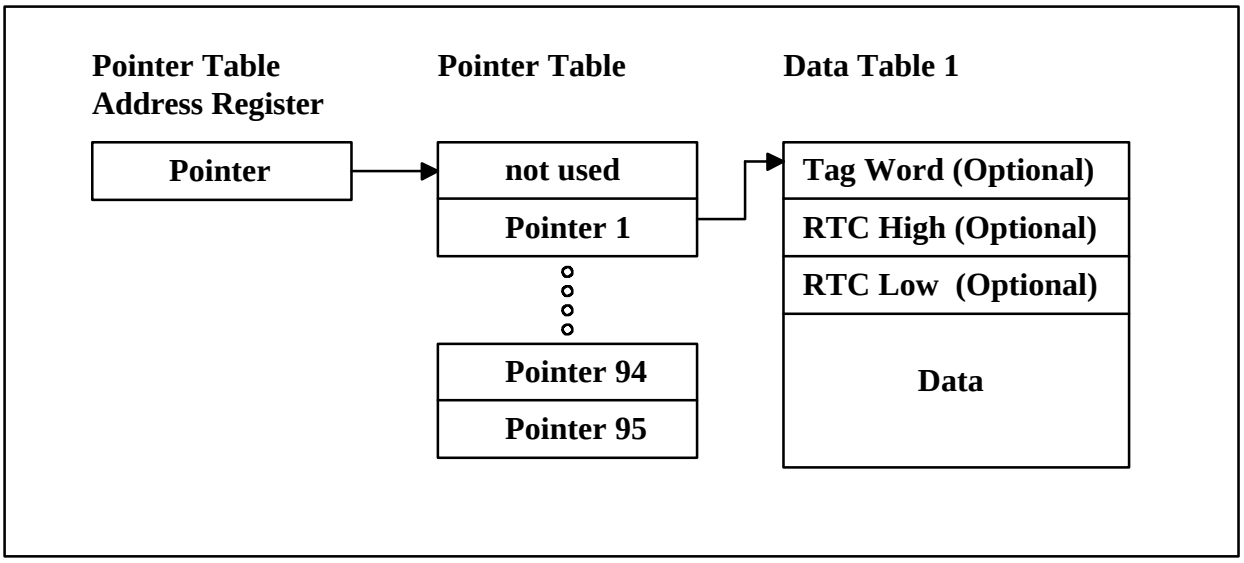
Writing a word to the COMMAND OUTPUT PINS (address 30 in the I/O space) can be used to simulate the option which outputs 5 bits onto the I/O bus following valid command reception (see CMDO bit in the CONTROL register for details). This address is unique since a write operation activates both the I/O bus COMMAND STROBE and the I/O bus write signal (i.e., CMDS=1 and *I/O WR=0). As a result, the bits can be latched without decoding address lines.

4.2.21 I/O TAG WORD REGISTER

When a data table is mapped to address 32 in the I/O space, its tag word is contained in this register. This tag word can be used, for example, to specify an output pulse whenever the data table is accessed. All other I/O space data tables are without internal tag words and have no pulses associated with them.

4.3 DATA TABLES

The data words associated with transmit/receive messages and mode commands are stored in data tables. The data table addresses are stored in a POINTER TABLE located in the RAM. The data tables themselves can be individually allocated to either the RAM or the I/O space. Data tables mapped to the I/O space can be used for discrete I/O without requiring host intervention. The mapping scheme is illustrated in the following diagram:



The T/R, subaddress, and word count fields in the command are used to index the pointer table as defined below:

Index	T/R	Subaddress	Mode Code	Command Type
0		not used		
1-30	0	1-30		Receive
31-32		not used		
33-62	1	1-30		Transmit
63		not used		
64-95	X	0,31	0-31	Mode Codes

4.3.1 MESSAGE ILLEGALITY

Commands are illegalized by setting the address field of the corresponding data table pointer to 0. When the protocol chip receives an illegal command, it responds with ME=1 in the status; in addition, data transmission and storage are suppressed. All undefined mode commands as well as "Dynamic Bus Control" are ignored.

4.3.2 DATA TABLE TAG WORD

The data table's first word can be defined to be either a data word or a TAG WORD (see the NTAG field in the CONTROL register) which defines the table's status and associated options. The TAG WORD has the following format:

15	14	13	12	11-8	7	6	5	4-0
UPD	SSFENA	BCST	X	PULSE (3:0)	LOCK	INV	OVW	WCNT

UPD

UPD=1 Indicates that the table was updated with data by the host or a 1553 message. The host should set this bit after writing to the table and reset the bit after reading the table.

SSFENA

SSFENA=1 Enables setting the subsystem flag in the status word whenever the RT transmits stale data or overwrites received data (i.e., whenever data is transmitted from a table with UPD=0, or is stored into a table with UPD=1).

BCST

BCST=1 Indicates that the table contains data from a valid broadcast message.

BCST=0 Indicates that the table contains data from a non-broadcast message.

PULSE (3:0) This field defines which pin should be pulsed at the end of a valid message which accesses the data table (see CMDO in the CONTROL register for details). The field is defined as follows:

PULSE FIELD VALUE	PULSED OUTPUT PIN
0	No Pulse
1-8	I/O DATA(0),..., (7)
14	PLSCMD

LOCK

LOCK=1 Indicates that the protocol chip is currently using the table for a message, either writing receive data or reading transmit data.

INV

INV=1 Indicates that the table contains invalid data.

OVW

OVW=1 Indicates that data received from the 1553 bus caused the data to be overwritten before its previous contents were read by the host or that the host did not update the data since the last transmission (i.e., whenever data is transmitted from a table with UPD=0, or is stored into a table with UPD=1). This bit is similar to the subsystem flag returned to the Bus Controller when SSFENA=1.

WCNT This field contains the word count/mode code in the command which referenced the data table.

4.3.3 DATA TABLE POINTER

The DATA TABLE POINTER has the following format:

15	14	13	12-1	0
INTREQ	RTCENA	X	ADDRESS	X

INTREQ
INTREQ=1 Specifies that an interrupt shall be issued after the completion of a message which accesses the data table.

RTCENA
RTCENA=1 Specifies that the data table shall be time-tagged with the RTC.

ADDRESS Defines the location of the data table in the 4K word address space. Since data tables always begin on word boundaries, the register's LSB (which specifies byte boundaries) is ignored. If the address field is set to 0, the command associated with the pointer is illegalized.

4.3.4 DATA TABLE BUFFERING SCHEME

Since the host and the NHI-RT can access data tables asynchronously, data integrity must be ensured by a suitable buffering scheme. The method employed by the RT assumes that there are two pointer tables; one specifies data tables accessed by the RT and the other tables accessed by the host. The host's pointer table can reside anywhere in its memory space since it is never accessed by the RT. Data buffers are switched by the host exchanging pointers as explained below.

4.3.4.1 RT RAM ACCESS

When the RT wants to read or write to a data table, it fetches the corresponding data table pointer from its pointer table. It then sets the LOCK bit in the data table's TAG WORD to 1 and proceeds with the update. At the completion of the update, the RT sets the LOCK bit to 0 and also sets the UPD bit in the TAG WORD to 1 if it wrote to the data table or 0 if it read the data table. If the condition of the UPD bit at the start of the RT access indicates that the host has not read from or written to the data table since the last RT access to that table, the RT sets the OVW bit in the TAG WORD to 1 to tell the host stale data has been transmitted by the RT or data has been overwritten by the RT.

Since the RT may fetch a data table pointer while the host is in the process of exchanging the corresponding pointers, there is a possibility that the RT's pointer will point to the table used by the host. In order to avoid this potential conflict, the host should check the LOCK bit in its data table tag word **AFTER** exchanging the pointers but **BEFORE** reading the data. If LOCK=1, the host should either re-exchange the pointers or wait until LOCK=0.

NOTE : The LOCK bit is ALWAYS set in the TAG WORD of the data table accessed by the RT, irrespective of when the pointers are exchanged by the host. This is guaranteed because the RT reads the data table's pointer and sets the LOCK bit in the TAG WORD using a read - read - modify - write sequence which cannot be interrupted by the host (i.e., read POINTER - read TAG WORD - modify LOCK bit - write back TAG WORD with LOCK bit modified).

4.3.4.2 HOST RAM ACCESS

When the host wants to access a RECEIVE data table, it first exchanges the pointer in its pointer table with the corresponding pointer in the RT's table. Then, the host reads the LOCK bit in the TAG WORD. If the LOCK bit is 0, the host proceeds with its access. If, however, the LOCK bit is 1, this informs the host that the RT is accessing that data table. The host should then delay its access until the LOCK bit has been set to 0 by the RT. When the host finishes accessing the RECEIVE data table, it should set the UPD bit in the data table's TAG WORD to 0. This will tell the RT the host has taken the data.

When the host wants to access a TRANSMIT data table, it first reads the LOCK bit in the TAG WORD of the table belonging to the host. If the LOCK bit is 0, the host proceeds with its access. If, however, the LOCK bit is 1, this informs the host that the RT is still accessing that data table. The host should then delay its access until the LOCK bit has been set to 0 by the RT. When the host finishes updating its TRANSMIT data table, it should set the UPD bit in the data table's TAG WORD to 1 and then exchange corresponding pointers. This will ensure that updated data for transmission is made available to the RT as soon as possible and inform the RT that it will be transmitting fresh data.

Since the host can change its table of pointers at any time, the above mapping scheme can be used to achieve any desired depth of buffering by simply employing a "round-robin" of pointers.

4.3.4.3 READ-MODIFY-WRITE

The host Read-Modify-Write cycle is used to support CPUs similar to the Motorola 680X0 where certain instructions (eg:, test and set) require two contiguous accesses to memory. Such accesses are unique in that the address strobe (ASN) remains active for both cycles.

5.0 MODE CODE OPERATION

5.1 GENERAL

This section will define the operation of the NHI-RT during reception of all the mode commands. The following terms are used in this section:

VALID COMMAND
A command meeting the criteria established by the 1553B standard in paragraph 4.4.1.1.

INVALID COMMAND
A command NOT meeting the criteria established by the 1553B standard in paragraph 4.4.1.1.

UNIMPLEMENTED COMMAND
A command not implemented by the NHI-RT.

The following general response characteristics apply to the NHI-RT when operating on the bus:

RECEIPT OF AN INVALID COMMAND
There is no response and the command is ignored.

RECEIPT OF AN UNIMPLEMENTED COMMAND
There is no response and the command is ignored.

The following abbreviations are used in this discussion:

SW = STATUS REGISTER
CDR = CONDITION REGISTER
TW = TAG WORD IN DATA TABLE
ME = MESSAGE ERROR BIT
BCR = BROADCAST BIT

Additional information about each mode code is available in the INTERRUPT VECTOR REGISTER and the AUXILIARY VECTOR REGISTER if it is set to be interrupt driven (see Data Table Pointer word, Interrupt Vector Register and Auxiliary Vector Register).

The table on the following pages will describe the response and the action taken by the NHI-RT to all of the mode codes.

5.2 TABLE OF MODE CODE RESPONSES

5.2.1 DYNAMIC BUS CONTROL (00000; T/R=1)

UNIMPLEMENTED MODE CODE

5.2.2 SYNCHRONIZE WITHOUT DATA (00001; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.3 TRANSMIT LAST STATUS WORD (00010; T/R=1)

VALID COMMAND
Responds with status except if broadcast. Status NOT updated.
Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
Status not cleared. No status response.

Bits set: *MDCD to "0" in CDR. INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.4 INITIATE SELF TEST (00011; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.5 TRANSMITTER SHUTDOWN (00100; T/R=1)

VALID COMMAND
Responds with status except if broadcast. Transmitter on alternate bus inhibited. Alternate bus transmitter re-enabled by: Reset mode code, Override Transmitter Shutdown mode code, resetting RT, or power up. Bits set: *MDCD to "0" and alt bus (A) (B) XEN to "0" in CDR.

If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.6 OVERRIDE TRANSMITTER SHUTDOWN (00101; T/R=1)

VALID COMMAND
Responds with status except if broadcast. Transmitter on alternate bus enabled.
Bits set: *MDCD to "0" and alt bus (A) (B) XEN to "1" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.7 INHIBIT TERMINAL FLAG (00110; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" and TFE to "0" in CDR. Terminal Flag inhibited in SW.

If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.8 OVERRIDE INHIBIT TERMINAL FLAG (00111; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" and TFE to "1" in CDR. Terminal Flag enabled in SW.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.9 RESET REMOTE TERMINAL (01000; T/R=1)

VALID COMMAND
Responds with status except if broadcast. Both Transmitters enabled and Terminal Flag enabled. Pointer base address register set to 2048 dec. External terminal address loaded.

Bits set: *MDCD to "1", TFE to "1", AXEN to "1", and BXEN to "1" in CDR.
BUSY to "1" in SW.
If broadcast- BCR, BCST in SW & TW set to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.10 RESERVED MODE CODES (01001-01111; T/R=1)]

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME and BCR set to "1" in SW.
INV and BCST set to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.11 TRANSMIT VECTOR WORD (10000; T/R=1)

VALID COMMAND
Responds with status followed by vector word except if broadcast.
Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD

UNIMPLEMENTED COMMAND

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.12 SYNCHRONIZE WITH DATA WORD (10001; T/R=0)

VALID COMMAND
Responds with status except if broadcast. Data word stored into RAM. Data word will update lower 16 bits of real time clock depending on the configuration of the RTC CONTROL REGISTER.

Bits set: *MDCD to "0" in CDR.

If broadcast- BCR, BCST in SW & TW to "1".

COMMAND NO DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.

COMMAND + EXTRA DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV set to "1" in TW.

BROADCAST + EXTRA DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME and BCR to "1" in SW.
INV and BCST to "1" in TW.

T/R=1
UNIMPLEMENTED COMMAND

T/R=1 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.13 TRANSMIT LAST COMMAND (10010; T/R=1)

VALID COMMAND
Responds with status followed by LAST VALID COMMAND word except if broadcast. Status and command registers NOT updated.

Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR.
INV to "1" in TW.

BROADCAST COMMAND

UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD
UNIMPLEMENTED COMMAND

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.14 TRANSMIT BIT WORD (10011; T/R=1)

VALID COMMAND
Responds with status followed by BIT word.
Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD
UNIMPLEMENTED COMMAND

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.15 SELECTED TRANSMITTER SHUTDOWN (10100; T/R=0)
UNIMPLEMENTED COMMAND

5.2.16 OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101; T/R=0)
UNIMPLEMENTED COMMAND

5.2.17 RESERVED MODE CODES (10110-11111; T/R=1)

VALID COMMAND
Responds with status and data word.
Bits set: *MDCD to "0" in CDR.

COMMAND + DATA WORD
No response
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD
UNIMPLEMENTED COMMAND

5.2.18 RESERVED MODE CODES (10110-11111; T/R=0)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST to "1" in TW & SW.

COMMAND + EXTRA DATA WORD
No response
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

COMMAND WITHOUT DATA WORD
No response
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.

BROADCAST WITH EXTRA DATA WORD
No response
Bits set: *MDCD to "0" in CDR. ME & BCR to "1" in SW
INV & BCST to "1" in TW

BROADCAST WITHOUT DATA WORD
No response
Bits set: *MDCD to "0" in CDR. ME & BCR to "1" in SW

6.0 INITIALIZATION

There are two types of initialization that can set up the NHI-RT parameters. One is controlled by the various types of resets (POR, Hardware, Software, and Mode Code), and the other is controlled by the host. A brief description will be given for each type.

6.1 INTERNAL INITIALIZATION

There are four methods of initializing the NHI-RT without host intervention. Each will produce the same results. The four methods are: POR (Power On Reset), Hardware, Software (writing to address 15, data not used), and Mode Code (receipt of "Reset" mode code).

The hardwire terminal address is loaded when any of these initializations occur. The hardwire address is connected to I/O DAT(5:0) pins. I/O DAT(4:0) are used for the address and I/O DAT5 is used to set odd parity in the address. The address is wired using external 4.7K pull-down resistors to set a low and internal 64K pull-up resistors to set a high.

The following table summarizes the condition of the internal registers after an initialization has been performed.

REGISTER	**BITS=1**	**BITS=0**	**COMMENTS**
CONTROL	MIO, NTAG	ALL OTHERS	NHI-RT INITIALIZED WITHOUT A TAG WORD
POINTER ADDRESS			LOADED WITH 2048 DECIMAL WORD
BASIC STATUS	BUSY	ALL OTHERS	TADR FIELD GETS HARDWIRE ADDRESS
INT MASK	ALL		**ALL INTERRUPTS MASKED**
INT VEC			
INT REQ		ALL	
AUX VEC			UNDEFINED
RTC; HIGH-LOW		ALL	RTC RESET TO 0
RTC CONTROL		ALL	UPDATES IN BYTE MODE
FIFO			RESET AND CLEARED
LAST COMMAND			UNDEFINED
LAST STATUS	BUSY	ALL OTHERS	TADR FIELD GETS HARDWIRE ADDRESS
ENCODER STATUS		ALL	
CONDITION	ALL		

The RAM is not initialized or reset by any of the internal initialization routines performed by the RT. The pointer tables and data tables are not defined.

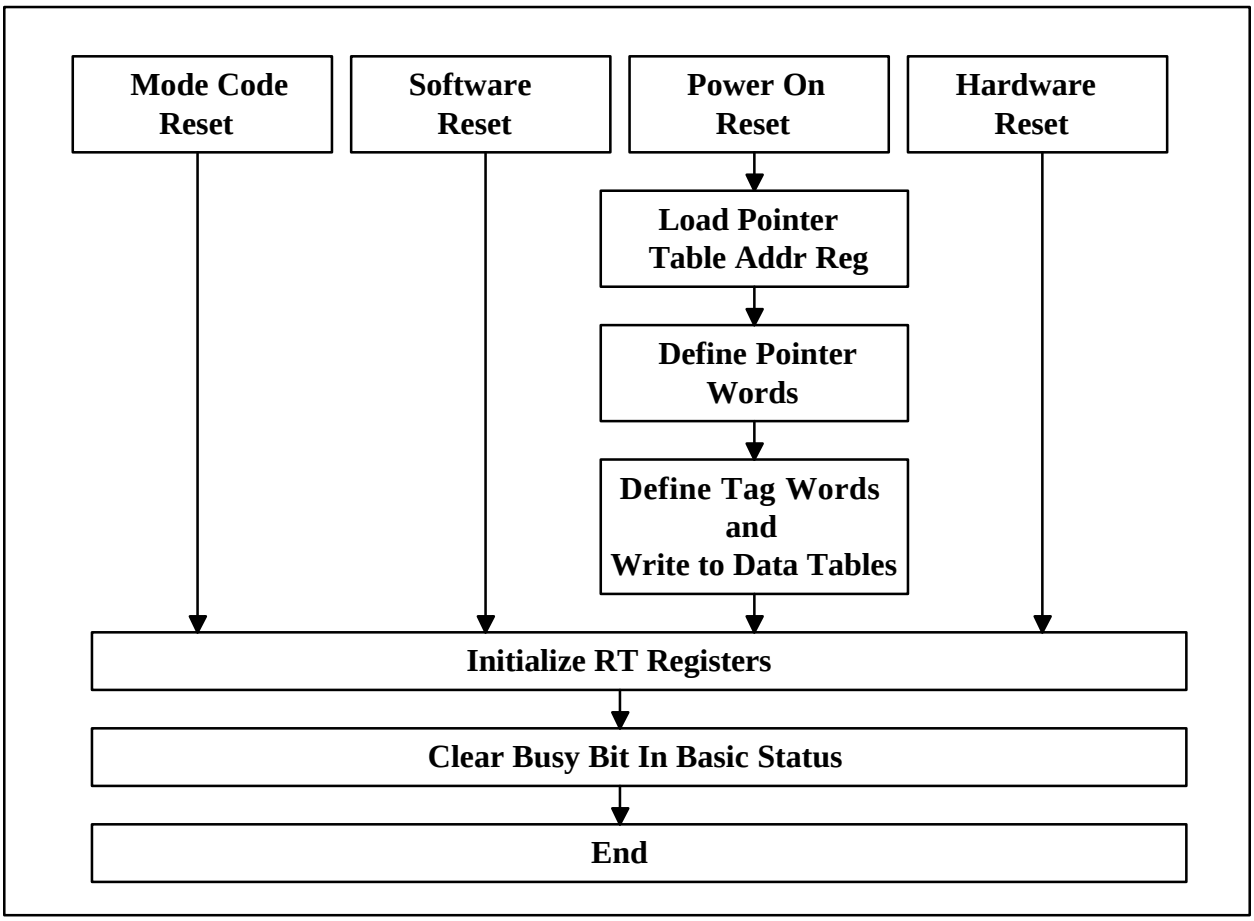
6.2 HOST INITIALIZATION OF NHI-RT

The host will usually want to initialize the RT at power up or at any other time it feels the procedure is necessary. At power up the host must initialize the registers discussed in the preceding section if the default settings of the internal initialization are not suitable. In addition the

host must initialize the RAM, the pointer tables, and the data table tag words for each command type and subaddress.

The host initialization of the registers is also required after a hardware reset or a software reset or after receipt of the "Reset" mode code because these resets invoke the internal initialization routine of the RT. Since the RAM is not affected by this routine, it does not have to be re-initialized, therefore the pointer tables will remain intact.

The following flow diagram is a suggested method of host initialization as a function of the type of reset which has occurred.



7.0 INTERRUPT HANDLING

When an interrupt request is received by the NHI-RT, the *IRQ line goes low and header information about the message that caused the interrupt is pushed on an internal FIFO. If another interrupt request is received before the CPU performs an acknowledge, it's header information is also pushed onto the FIFO. In this manner, there is no danger of losing interrupt vectors or header information due to receiving multiple interrupt requests before an acknowledge by the CPU takes place. The FIFO can hold header information for four interrupt messages. If an interrupt request occurs when the FIFO is full, a vector indicating FIFO overflow is first pushed onto the FIFO and then the header information for the message which caused the overflow is pushed onto the FIFO. As a result, the header information from the two oldest messages is lost.

7.1 HARDWARE INTERRUPT ACKNOWLEDGE

To acknowledge an interrupt in hardware, the *INTACK line is taken low, the *HCS line held high and the *INTPI line is held low. This pops the interrupt header information off the FIFO and into the IVR and AVR. The *IRQ line will go high and return low after about 400ns if there are more interrupt headers on the FIFO. Also, the IVR will be outputted on the upper and lower byte of the CPU data bus. If the *INTPI line is high, then *INTACK is ignored.

The IVR and AVR can be read from address 4 after performing the hardware interrupt.

If there are more interrupt headers on the FIFO, indicated by the *IRQ returning low after 400ns, the acknowledge procedure is repeated until the FIFO is empty. An empty FIFO is indicated by the *IRQ line remaining high after an interrupt acknowledge.

7.2 SOFTWARE INTERRUPT ACKNOWLEDGE

If the host CPU does not support a hardware interrupt acknowledge, a software acknowledge can be performed by reading address 8. This read pops the interrupt header information off the FIFO and into the IVR and AVR and places their contents on the CPU data bus. The *IRQ line will go high and return low after about 400 ns if there are more interrupt headers on the FIFO.

If there are more interrupt headers on the FIFO, indicated by the *IRQ returning low after 400 ns, the acknowledge procedure is repeated until the FIFO is empty. An empty FIFO is indicated by the *IRQ line remaining high after an interrupt acknowledge.

8.0 PIN FUNCTIONAL DESCRIPTION

The NHI-RT I/O pins are divided into 5 families:

- General purpose signals
- Host interface signals
- I/O bus interface signals
- 1553 interface signals
- Power

8.1 GENERAL PURPOSE SIGNALS

***RST:** *RST=0 (active low, input).
Initializes all registers and state machines. RT reads hardwire terminal address.

CLK: Clock from 10 Mhz oscillator (input).

8.2 HOST INTERFACE SIGNALS

H_DAT (15:0): HOST DATA bus (bi-directional).

H_ADR(12:1): HOST ADDRESS bus (input).

***HCS:** CHIP SELECT (active low, input).

Selects the NHI-RT. The falling edge of *HCS is used to latch the host's address and indicates the start of a host memory cycle. The rising edge terminates the current cycle. During a host read-modify-write cycle, this signal must remain active from the beginning of the read cycle to the end of the write cycle.

NOTE: The host should not hold *HCS active for more than 5 microseconds, otherwise timing errors on the 1553 bus may occur.

***HWRL:** HOST WRITE LOWER BYTE (active low, input).

***HWRH:** HOST WRITE UPPER BYTE (active low, input).

***HRD:** HOST READ (active low, input).

***DTACK(*READY):** HOST DATA TRANSFER ACKNOWLEDGE (active low, open drain output).

Indicates to the host that a data transfer has been completed. When the host reads data, it takes *HCS low and then *HRD low. The RT then indicates that stable data is on the bus by outputting a low on *DTACK. When the host writes data, it takes *HCS low and then *HWRL and/or *HWRH low. The RT then indicates that it has completed the write cycle by outputting a low on *DTACK.

***IRQ:** Host INTERRUPT REQUEST (active low, open drain output).

***INTACK:** Host INTERRUPT ACKNOWLEDGE (active low, input).

Indicates that the host is acknowledging an interrupt. When *HRD=0, *INTACK=0, and *HCS=1, an interrupt vector is popped from the FIFO, the IVR/AVR registers are updated, and the IVR is outputted onto both the lower and upper bytes of the host data bus provided that the *INTPI is low (see *INTPI description).

***INTPI:** INTERRUPT PRIORITY INPUT (active low, input).

This signal is used to daisy chain interrupt requests on the host bus. This signal must be active for the RT to output an interrupt vector.

***IPO_DSC:** INTERRUPT PRIORITY OUTPUT, DISCONNECT SIGNAL (output).

This pin has 2 possible functions, depending on the M1760 bit in the RTC CONTROL register.

If M1760=0, then the signal is used to daisy chain interrupt requests on the host bus. When the RT requests an interrupt, this signal is output high; otherwise, this signal is equal to *INTPI.

If M1760=1, then the pin is set to "1" when the store is disconnected (see EXTERNAL TERMINAL ADDRESS BUFFER for details).

8.3 DISCRETE I/O BUS INTERFACE SIGNALS

***I/O_RD:** I/O READ (active low, output).

***I/O_WR:** I/O WRITE (active low, output).

I/O_ADR (2:1): I/O ADDRESS (outputs).

These signals can be used to select 4 byte-wide input devices and 4 byte-wide output devices which reside on the I/O bus.

I/O_DAT (7:0): I/O DATA bus (bi-directional).

CMDS: COMMAND STROBE (active high, output).
This strobe is used for two special I/O operations. When the strobe is active during a write cycle (i.e., CMDS=1, *I/O WR=0), valid commands/pulses appear on the I/O bus (see the CMDO bit in CONTROL register for details). When the strobe is active during a read cycle (i.e., CMDS=1, *I/O RD=0), the EXTERNAL TERMINAL ADDRESS buffer is accessed.

PLSCMD: PULSE COMMAND (active high, output).
Depends on the value of the CMDO bit in the CONTROL register. If CMDO=0, then a pulse is issued whenever a 1553 message accesses a data table with PULSE (3:0)=14 (decimal) in its tag word. If CMDO=1, then a pulse is issued whenever a valid broadcast command is received.

Note:The NTAG bit in the CONTROL register must be 0 to get a pulse output.

MDCDRST: MODE COMMAND RESET (active high, output).
Pulsed high whenever a mode command "Reset" is received.

SSF_TF: SUBSYSTEM FLAG, TERMINAL FLAG (active high, input).
Sets either the SUBSYSTEM FLAG bit or the TERMINAL FLAG bit in the STATUS register. The SSF_TF bit in the CONTROL register determines which status bit will be set by this input (see CONTROL register for details).

8.4 MIL-STD-1553B INTERFACE SIGNALS

BUS A, *BUS A: 1553 BUS A signals (bi-directional).
Connected to a bus coupling transformer.

BUS B, *BUS B: 1553 BUS B signals (bi-directional).
See Bus A.

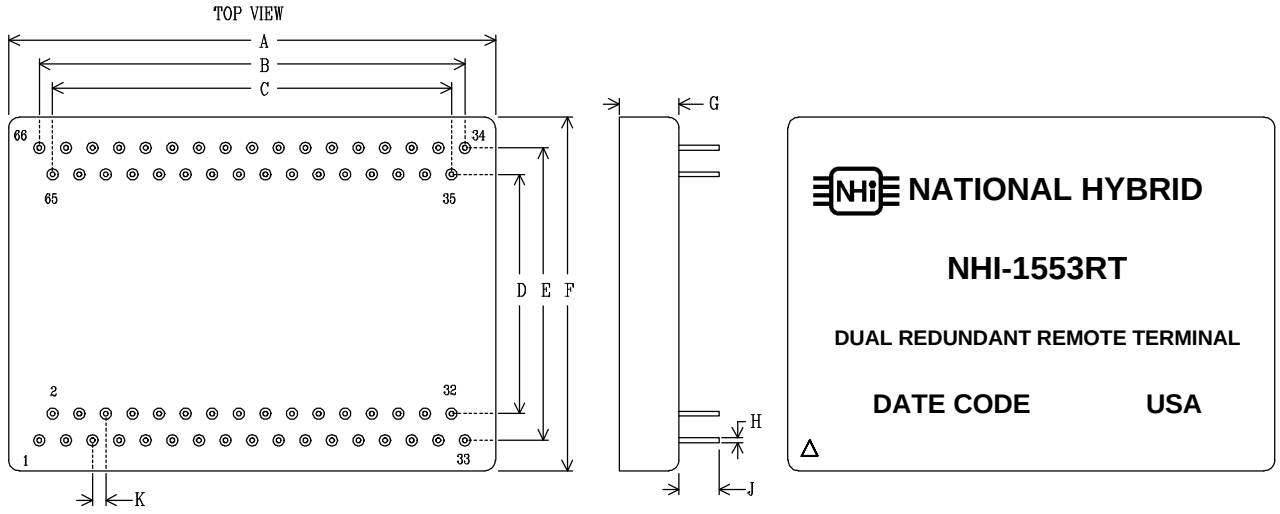
AINH: BUS A INHIBIT (input).
Inhibits the bus A transmitter.

BINH: BUS B INHIBIT (input).
Inhibits the bus B transmitter.

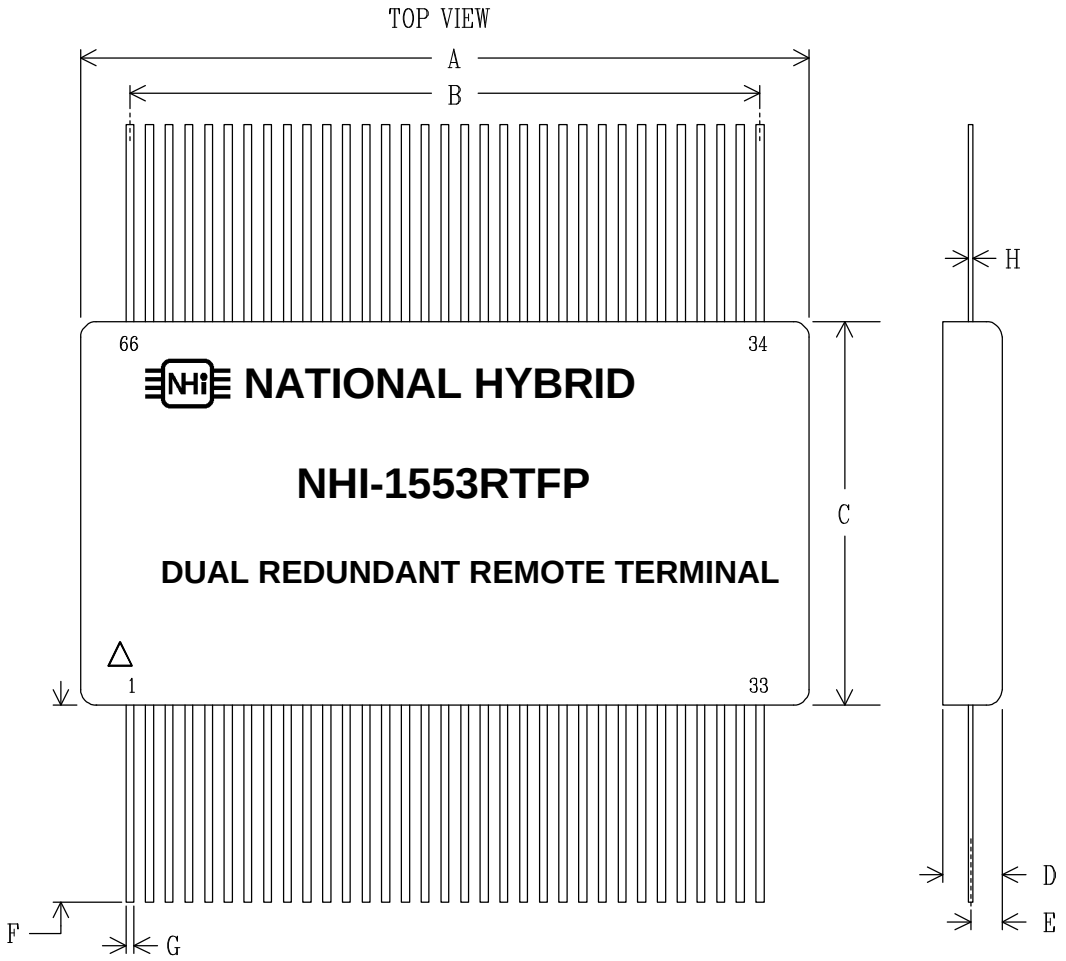
9.0 PIN FUNCTIONS AND MECHANICAL DRAWINGS

Pin Functions

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	TXINH_A	18	H_DAT3	34	BUS_B	51	+5V
2	+5V	19	H_DAT4	35	BUS_B_L	52	DSC_INTPO_L
3	H_ADR1	20	H_DAT5	36	GND	53	MDCDRST
4	H_ADR2	21	H_DAT6	37	I/O_DAT0	54	INTPI_L
5	H_ADR3	22	H_DAT7	38	I/O_DAT1	55	INTACK_L
6	H_ADR4	23	H_DAT8	39	I/O_DAT2	56	CMDS
7	H_ADR5	24	H_DAT9	40	I/O_DAT3	57	PLSCMD
8	H_ADR6	25	H_DAT10	41	I/O_DAT4	58	HWRL_L
9	H_ADR7	26	H_DAT11	42	I/O_DAT5	59	HRD_L
10	H_ADR8	27	H_DAT12	43	I/O_DAT6	60	I/O_RD_L
11	H_ADR9	28	H_DAT13	44	I/O_DAT7	61	I/O_WR_L
12	H_ADR10	29	H_DAT14	45	HCS_L	62	IRQ_L
13	H_ADR11	30	H_DAT15	46	+5V RAM	63	DTACK_L
14	H_ADR12	31	HWRH_L	47	RST_L	64	GND
15	H_DAT0	32	+5V	48	CLK	65	BUS_A_L
16	H_DAT1	33	TXINH_B	49	I/O_ADR1	66	BUS_A
17	H_DAT2			50	I/O_ADR2		



NHI-1553RT 66 Pin Plug-In Package Detail



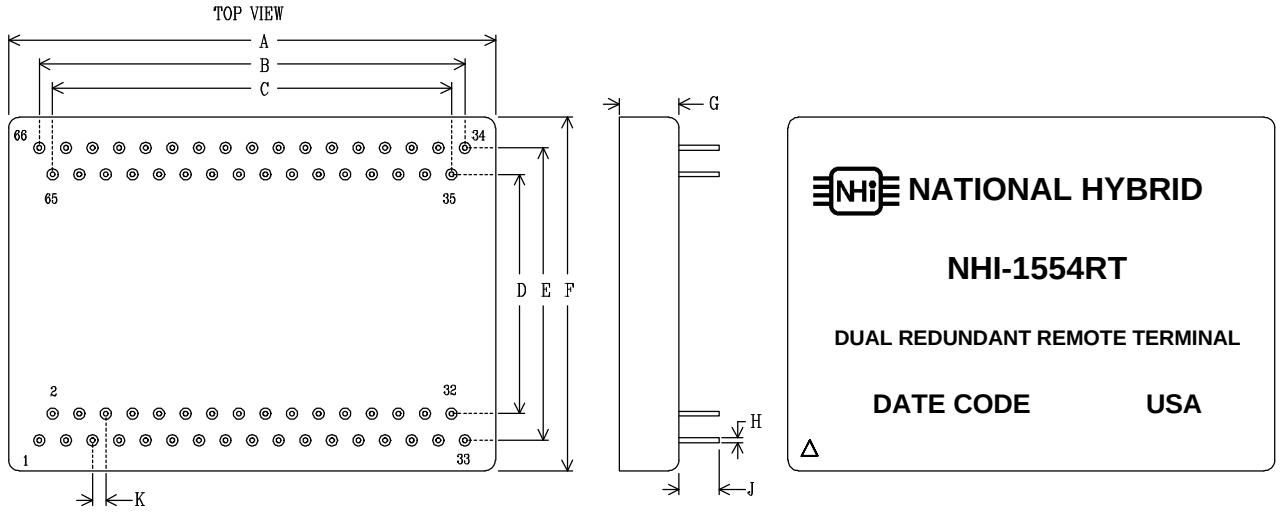
NHI-1553RTFP 66 Pin Flatpack Package Detail

Plug-In Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.830 "**	**0.010 "**
B	**16 EQ SP @**	**0.100 = 1.600 "**
C	**15 EQ SP @**	**0.100 = 1.500 "**
D	**0.900 "**	**0.010 "**
E	**1.100 "**	**0.010 "**
F	**1.330 "**	**0.010 "**
G	**0.225 "**	**MAX**
H	**0.018 " DIA.**	**0.002 "**
J	**0.200 "**	**MIN**

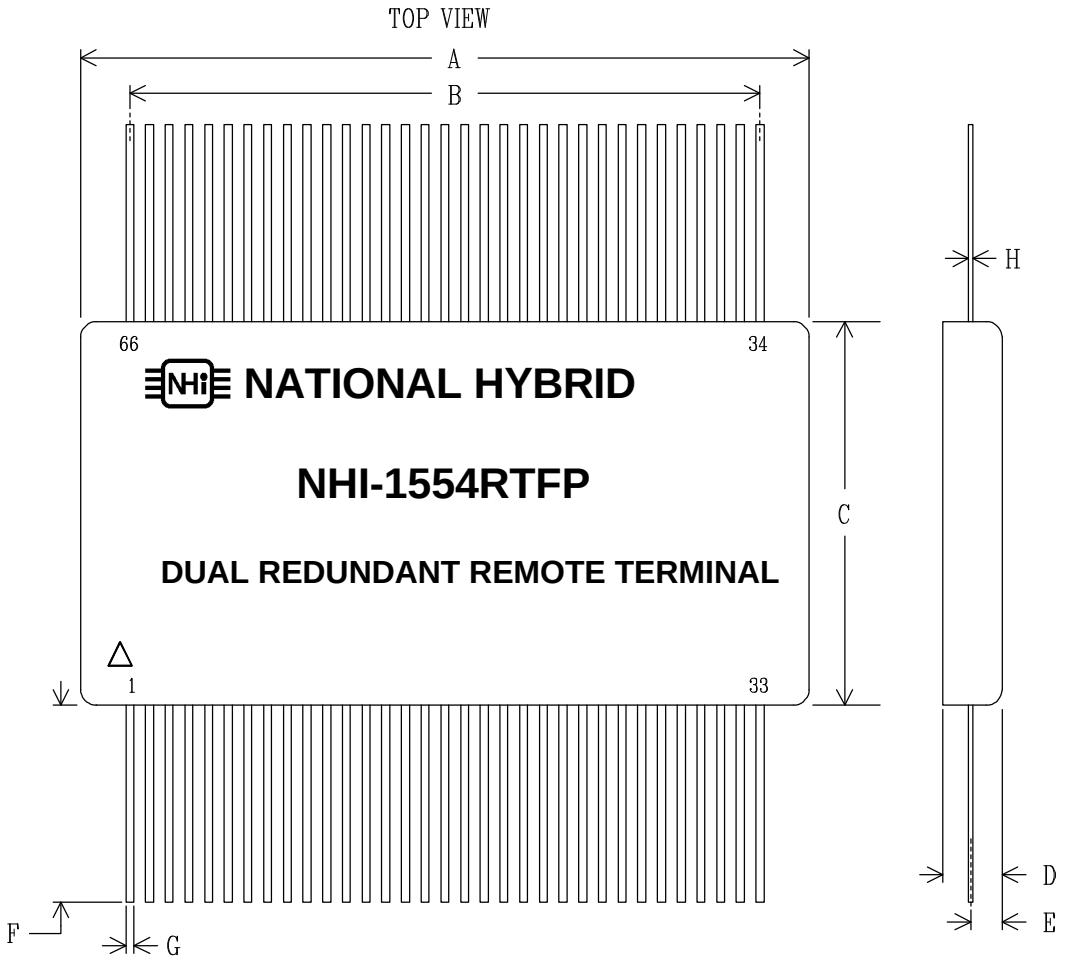
Flatpack Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.850 "**	**0.010 "**
B	**32 EQ SP @**	**0.050 =1.600 "**
C	**0.975 "**	**0.010 "**
D	**0.150 "**	**MAX**
E	**0.085 "**	**0.010 "**
F	**0.500 "**	**MIN**
G	**0.015 "**	**0.002 "**

Pin Functions

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	TXINH_A	18	H_DAT3	34	BUS_B	51	+5V
2	+5V	19	H_DAT4	35	BUS_B_L	52	DSC_INTPO_L
3	H_ADR1	20	H_DAT5	36	GND	53	MDCDRST
4	H_ADR2	21	H_DAT6	37	I/O_DAT0	54	INTPI_L
5	H_ADR3	22	H_DAT7	38	I/O_DAT1	55	INTACK_L
6	H_ADR4	23	H_DAT8	39	I/O_DAT2	56	CMDS
7	H_ADR5	24	H_DAT9	40	I/O_DAT3	57	PLSCMD
8	H_ADR6	25	H_DAT10	41	I/O_DAT4	58	HWRL_L
9	H_ADR7	26	H_DAT11	42	I/O_DAT5	59	HRD_L
10	H_ADR8	27	H_DAT12	43	I/O_DAT6	60	I/O_RD_L
11	H_ADR9	28	H_DAT13	44	I/O_DAT7	61	I/O_WR_L
12	H_ADR10	29	H_DAT14	45	HCS_L	62	IRQ_L
13	H_ADR11	30	H_DAT15	46	SSF_TF	63	DTACK_L
14	H_ADR12	31	HWRH_L	47	RST_L	64	GND
15	H_DAT0	32	+5V	48	CLK	65	BUS_A_L
16	H_DAT1	33	TXINH_B	49	I/O_ADR1	66	BUS_A
17	H_DAT2			50	I/O_ADR2		



NHI-1554RT 66 Pin Plug-In Package Detail

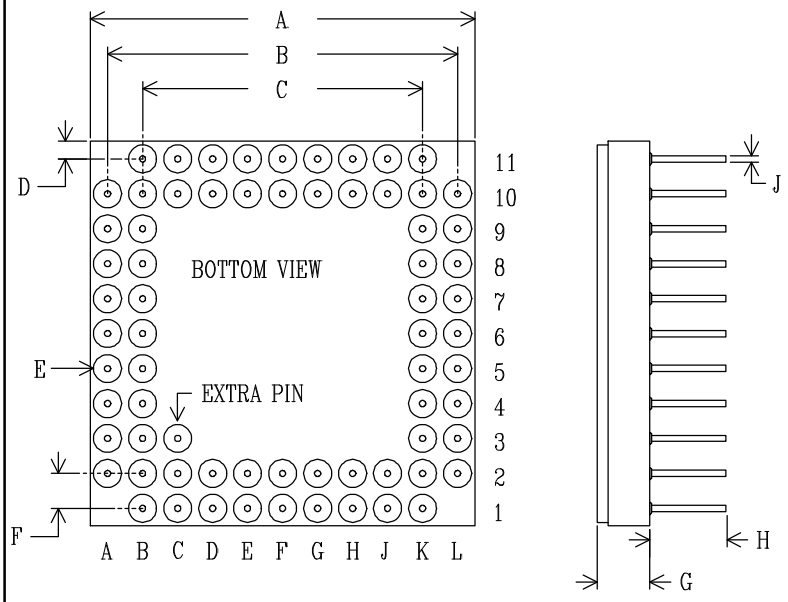


NHI-1554RTFP 66 Pin Flatpack Package Detail

Plug-In Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.830 "**	**0.010 "**
B	**16 EQ SP @**	**0.100 = 1.600 "**
C	**15 EQ SP @**	**0.100 = 1.500 "**
D	**0.900 "**	**0.010 "**
E	**1.100 "**	**0.010 "**
F	**1.330 "**	**0.010 "**
G	**0.225 "**	**MAX**
H	**0.018 " DIA.**	**0.002 "**
J	**0.200 "**	**MIN**

Flatpack Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.850 "**	**0.010 "**
B	**32 EQ SP @**	**0.050 =1.600 "**
C	**0.975 "**	**0.010 "**
D	**0.150 "**	**MAX**
E	**0.085 "**	**0.010 "**
F	**0.500 "**	**MIN**
G	**0.015 "**	**0.002 "**

NHI-1561RT 69 PGA Pin Functions							
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
A2	H_ADR7	B9	H_DAT8	F2	PLSCMD	K3	NC
A3	H_ADR8	B10	H_DAT9	F10	H_DAT15	K4	TXINH_B
A4	H_ADR10	B11	H_DAT10	F11	HWRH_L	K5	+5V
A5	H_ADR12	C1	H_ADR5	G1	H_DAT12	K6	INTACK_L
A6	H_DAT1	C2	BUS_A_L	G2	TXINH_A	K7	DSC_INTPO_L
A7	H_DAT2	C3	NC	G10	RST_L	K8	I/O_ADR1
A8	H_DAT4	C10	H_ADR1	G11	HCS_L	K9	I/O_DAT5
A9	H_DAT5	C11	H_DAT11	H1	BUS_B_L	K10	I/O_DAT4
A10	H_DAT6	D1	H_ADR3	H2	I/O_WR_L	K11	I/O_DAT0
B1	H_ADR6	D2	H_ADR4	H10	I/O_DAT2	L2	NC
B2	GND	D10	H_DAT13	H11	SSF_TF	L3	CMDS
B3	BUS_A	D11	HRD_L	J1	GND	L4	I/O_RD_L
B4	H_ADR9	E1	DTACK_L	J2	BUS_B	L5	+5V
B5	H_ADR11	E2	H_ADR2	J10	I/O_DAT3	L6	INTPI_L
B6	H_DAT0	E10	H_DAT14	J11	CLK	L7	I/O_ADR2
B7	H_DAT3	E11	HWRL_L	K1	GND	L8	I/O_DAT7
B8	H_DAT7	F1	IRQ_L	K2	MDCDRST	L9	I/O_DAT6
						L10	I/O_DAT1



TOP VIEW

NATIONAL HYBRID

NHI-1561RT

Mil-Std-1553
Remote Terminal

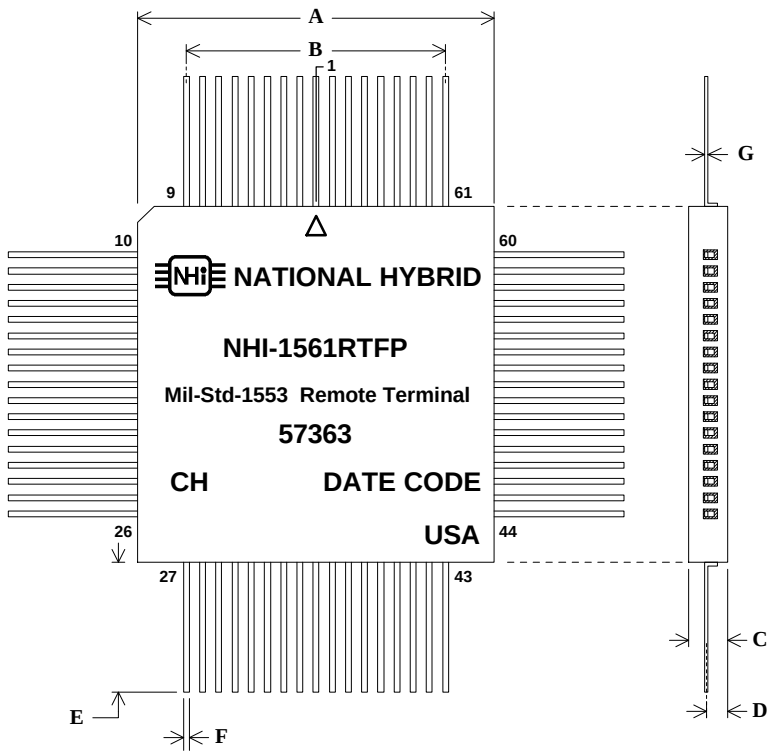
57363

USA

DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ.	0.010
B	10 EQ. SP. @ 0.100 = 1.000	
C	0.800	0.010
D	0.050	TYP
E	0.065 DIA	TYP
F	0.100	TYP
G	0.150	MAX
H	0.220	MIN
J	0.018 DIA.	0.002

NHI-1561RT 69 PGA Package Detail and Marking

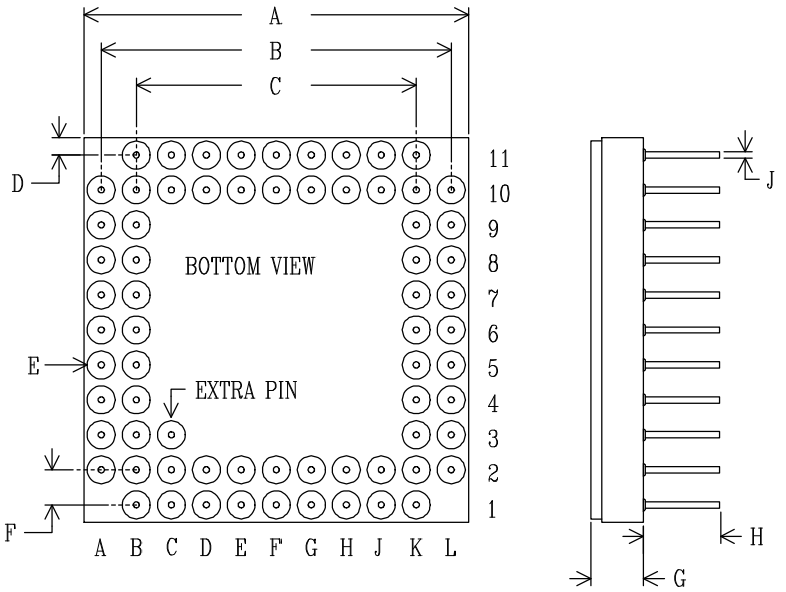
NHI-1561RTFP Pin Functions							
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	I/O_DAT1	18	BUS_A	35	H_ADR4	52	H_DAT3
2	I/O_DAT2	19	BUS_A_L	36	H_ADR5	53	H_DAT4
3	I/O_DAT3	20	NC	37	H_ADR6	54	H_DAT5
4	I/O_DAT4	21	CMDS	38	H_ADR7	55	H_DAT6
5	I/O_DAT5	22	TXINH_B	39	+5V	56	H_DAT7
6	I/O_DAT6	23	BUS_B	40	+5V	57	H_DAT8
7	I/O_DAT7	24	BUS_B_L	41	GND	58	H_DAT9
8	HCS_L	25	NC	42	GND	59	H_DAT10
9	SSF_TF	26	I/O_RD_L	43	GND	60	H_DAT11
10	RST_L	27	I/O_WR_L	44	H_ADR8	61	H_ADR1
11	CLK10	28	MDCDRST	45	H_ADR9	62	HRD_L
12	I/O_ADR1	29	PLSCMD	46	H_ADR10	63	HWRL_L
13	I/O_ADR2	30	IRQ_L	47	H_ADR11	64	HWRH_L
14	DSC_INTPO_L	31	DTACK_L	48	H_ADR12	65	H_DAT13
15	INTPI_L	32	H_DAT12	49	H_DAT0	66	H_DAT14
16	INTACK_L	33	H_ADR2	50	H_DAT1	67	H_DAT15
17	TXINH_A	34	H_ADR3	51	H_DAT2	68	I/O_DAT0



DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ	0.010
B	16 EQ SP @	0.050 = 0.800
C	0.140	MAX
D	0.065	0.010
E	0.400	MIN
F	0.018	0.002
G	0.010	0.002

NHI-1561RTFP 68 Pin Quad Flat Package Detail and Marking

NHI-1562RT 69 PGA Pin Functions							
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
A2	H_ADR7	B9	H_DAT8	F2	PLSCMD	K3	NC
A3	H_ADR8	B10	H_DAT9	F10	H_DAT15	K4	TXINH_B
A4	H_ADR10	B11	H_DAT10	F11	HWRH_L	K5	+5V
A5	H_ADR12	C1	H_ADR5	G1	H_DAT12	K6	INTACK_L
A6	H_DAT1	C2	BUS_A_L	G2	TXINH_A	K7	DSC_INTPO_L
A7	H_DAT2	C3	NC	G10	RST_L	K8	I/O_ADR1
A8	H_DAT4	C10	H_ADR1	G11	HCS_L	K9	I/O_DAT5
A9	H_DAT5	C11	H_DAT11	H1	BUS_B_L	K10	I/O_DAT4
A10	H_DAT6	D1	H_ADR3	H2	I/O_WR_L	K11	I/O_DAT0
B1	H_ADR6	D2	H_ADR4	H10	I/O_DAT2	L2	NC
B2	GND	D10	H_DAT13	H11	SSF_TF	L3	CMDS
B3	BUS_A	D11	HRD_L	J1	GND	L4	I/O_RD_L
B4	H_ADR9	E1	DTACK_L	J2	BUS_B	L5	+5V
B5	H_ADR11	E2	H_ADR2	J10	I/O_DAT3	L6	INTPI_L
B6	H_DAT0	E10	H_DAT14	J11	CLK	L7	I/O_ADR2
B7	H_DAT3	E11	HWRL_L	K1	GND	L8	I/O_DAT7
B8	H_DAT7	F1	IRQ_L	K2	MDCDRST	L9	I/O_DAT6
						L10	I/O_DAT1



TOP VIEW

NATIONAL HYBRID

NHI-1562RT

MacAir
Remote Terminal

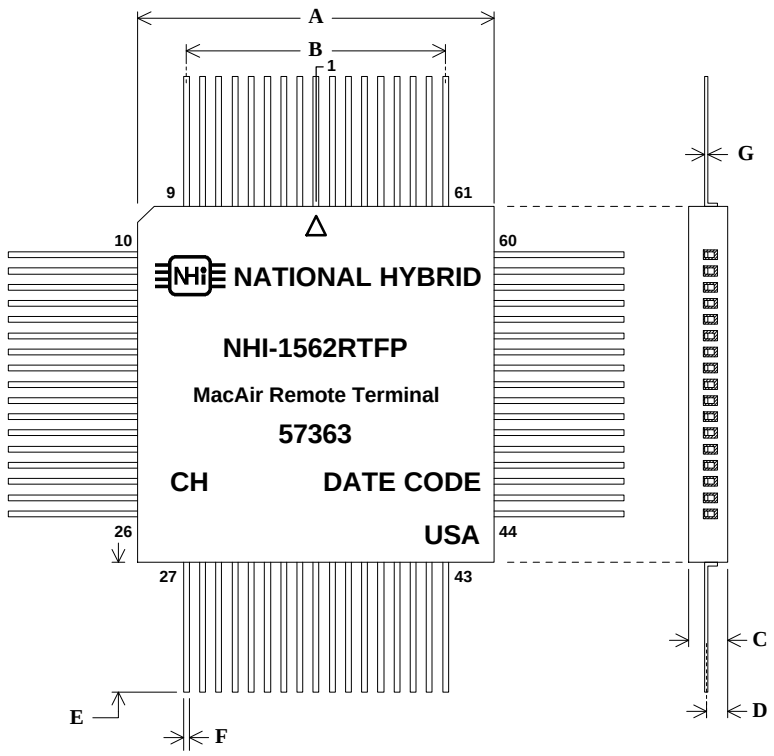
57363

USA △

DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ.	0.010
B	10 EQ. SP. @ 0.100 = 1.000	
C	0.800	0.010
D	0.050	TYP
E	0.065 DIA	TYP
F	0.100	TYP
G	0.150	MAX
H	0.220	MIN
J	0.018 DIA.	0.002

NHI-1562RT 69 PGA Package Detail and Marking

NHI-1562RTFP Pin Functions							
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
1	I/O_DAT1	18	BUS_A	35	H_ADR4	52	H_DAT3
2	I/O_DAT2	19	BUS_A_L	36	H_ADR5	53	H_DAT4
3	I/O_DAT3	20	NC	37	H_ADR6	54	H_DAT5
4	I/O_DAT4	21	CMDS	38	H_ADR7	55	H_DAT6
5	I/O_DAT5	22	TXINH_B	39	+5V	56	H_DAT7
6	I/O_DAT6	23	BUS_B	40	+5V	57	H_DAT8
7	I/O_DAT7	24	BUS_B_L	41	GND	58	H_DAT9
8	HCS_L	25	NC	42	GND	59	H_DAT10
9	SSF_TF	26	I/O_RD_L	43	GND	60	H_DAT11
10	RST_L	27	I/O_WR_L	44	H_ADR8	61	H_ADR1
11	CLK10	28	MDCDRST	45	H_ADR9	62	HRD_L
12	I/O_ADR1	29	PLSCMD	46	H_ADR10	63	HWRL_L
13	I/O_ADR2	30	IRQ_L	47	H_ADR11	64	HWRH_L
14	DSC_INTPO_L	31	DTACK_L	48	H_ADR12	65	H_DAT13
15	INTPI_L	32	H_DAT12	49	H_DAT0	66	H_DAT14
16	INTACK_L	33	H_ADR2	50	H_DAT1	67	H_DAT15
17	TXINH_A	34	H_ADR3	51	H_DAT2	68	I/O_DAT0

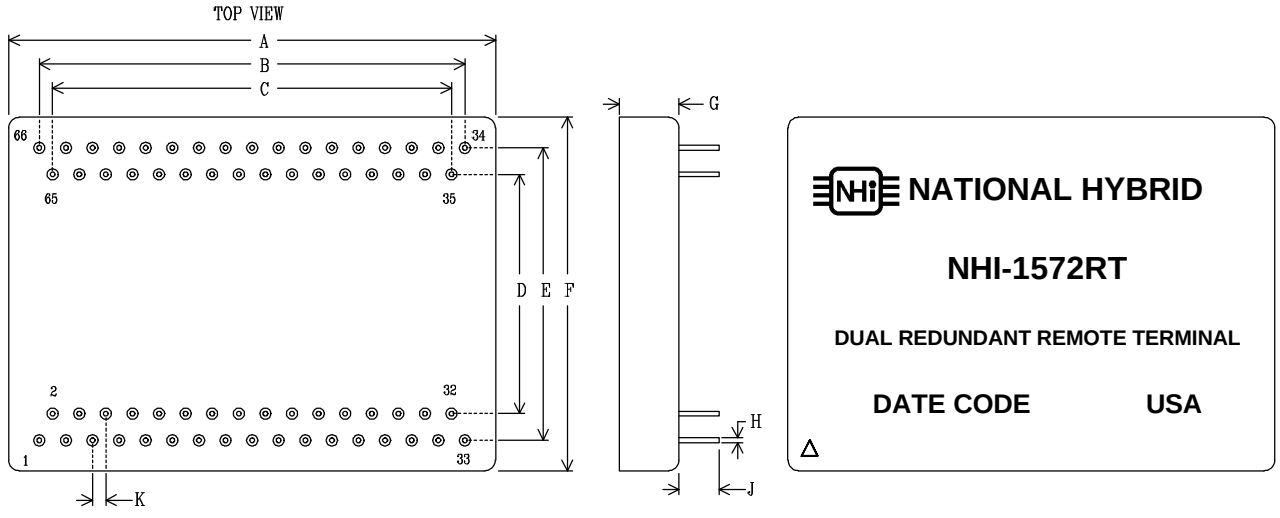


DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ	0.010
B	16 EQ SP @	0.050 = 0.800
C	0.140	MAX
D	0.065	0.010
E	0.400	MIN
F	0.018	0.002
G	0.010	0.002

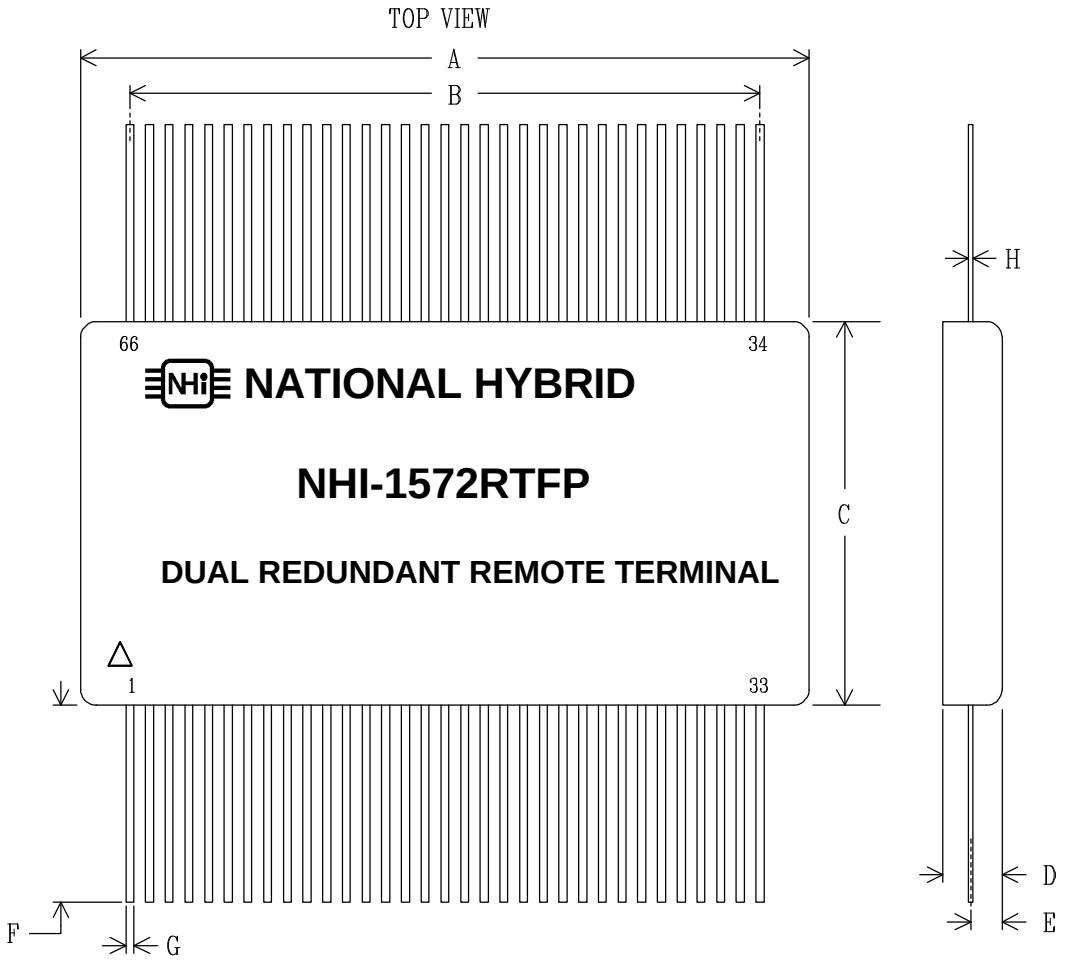
NHI-1562RTFP 68 Pin Quad Flat Package Detail and Marking

Pin Functions

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	TXINH_A	18	H_DAT3	34	BUS_B	51	+5V
2	+5V	19	H_DAT4	35	BUS_B_L	52	DSC_INTPO_L
3	H_ADR1	20	H_DAT5	36	GND	53	MDCDRST
4	H_ADR2	21	H_DAT6	37	I/O_DAT0	54	INTPI_L
5	H_ADR3	22	H_DAT7	38	I/O_DAT1	55	INTACK_L
6	H_ADR4	23	H_DAT8	39	I/O_DAT2	56	CMDS
7	H_ADR5	24	H_DAT9	40	I/O_DAT3	57	PLSCMD
8	H_ADR6	25	H_DAT10	41	I/O_DAT4	58	HWRL_L
9	H_ADR7	26	H_DAT11	42	I/O_DAT5	59	HRD_L
10	H_ADR8	27	H_DAT12	43	I/O_DAT6	60	I/O_RD_L
11	H_ADR9	28	H_DAT13	44	I/O_DAT7	61	I/O_WR_L
12	H_ADR10	29	H_DAT14	45	HCS_L	62	IRQ_L
13	H_ADR11	30	H_DAT15	46	+5V RAM	63	DTACK_L
14	H_ADR12	31	HWRH_L	47	RST_L	64	GND
15	H_DAT0	32	+5V	48	CLK	65	BUS_A_L
16	H_DAT1	33	TXINH_B	49	I/O_ADR1	66	BUS_A
17	H_DAT2			50	I/O_ADR2		



NHI-1572RT 66 Pin Plug-In Package Detail



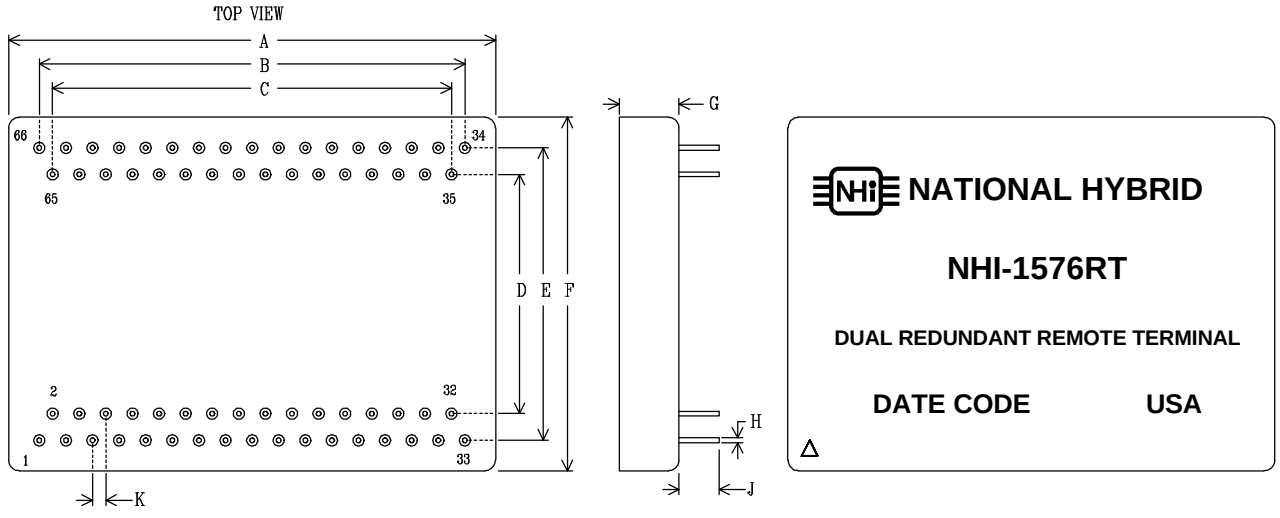
NHI-1572RTFP 66 Pin Flatpack Package Detail

Plug-In Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.830 "**	**0.010 "**
B	**16 EQ SP @**	**0.100 = 1.600 "**
C	**15 EQ SP @**	**0.100 = 1.500 "**
D	**0.900 "**	**0.010 "**
E	**1.100 "**	**0.010 "**
F	**1.330 "**	**0.010 "**
G	**0.225 "**	**MAX**
H	**0.018 " DIA.**	**0.002 "**
J	**0.200 "**	**MIN**

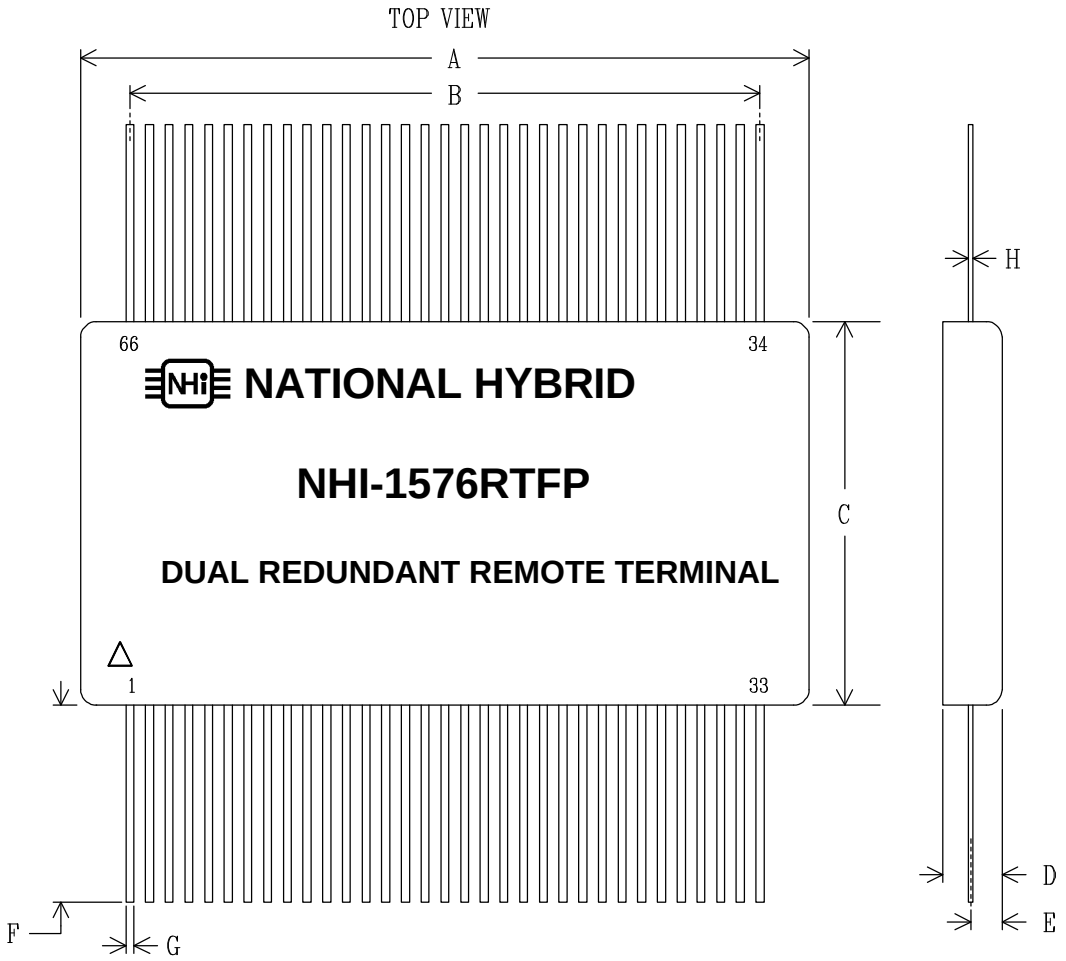
Flatpack Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.850 "**	**0.010 "**
B	**32 EQ SP @**	**0.050 =1.600 "**
C	**0.975 "**	**0.010 "**
D	**0.150 "**	**MAX**
E	**0.085 "**	**0.010 "**
F	**0.500 "**	**MIN**
G	**0.015 "**	**0.002 "**

Pin Functions

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	TXINH_A	18	H_DAT3	34	BUS_B	51	+5V
2	+5V	19	H_DAT4	35	BUS_B_L	52	DSC_INTPO_L
3	H_ADR1	20	H_DAT5	36	GND	53	MDCDRST
4	H_ADR2	21	H_DAT6	37	I/O_DAT0	54	INTPI_L
5	H_ADR3	22	H_DAT7	38	I/O_DAT1	55	INTACK_L
6	H_ADR4	23	H_DAT8	39	I/O_DAT2	56	CMDS
7	H_ADR5	24	H_DAT9	40	I/O_DAT3	57	PLSCMD
8	H_ADR6	25	H_DAT10	41	I/O_DAT4	58	HWRL_L
9	H_ADR7	26	H_DAT11	42	I/O_DAT5	59	HRD_L
10	H_ADR8	27	H_DAT12	43	I/O_DAT6	60	I/O_RD_L
11	H_ADR9	28	H_DAT13	44	I/O_DAT7	61	I/O_WR_L
12	H_ADR10	29	H_DAT14	45	HCS_L	62	IRQ_L
13	H_ADR11	30	H_DAT15	46	SSF_TF	63	DTACK_L
14	H_ADR12	31	HWRH_L	47	RST_L	64	GND
15	H_DAT0	32	+5V	48	CLK	65	BUS_A_L
16	H_DAT1	33	TXINH_B	49	I/O_ADR1	66	BUS_A
17	H_DAT2			50	I/O_ADR2		



NHI-1576RT 66 Pin Plug-In Package Detail



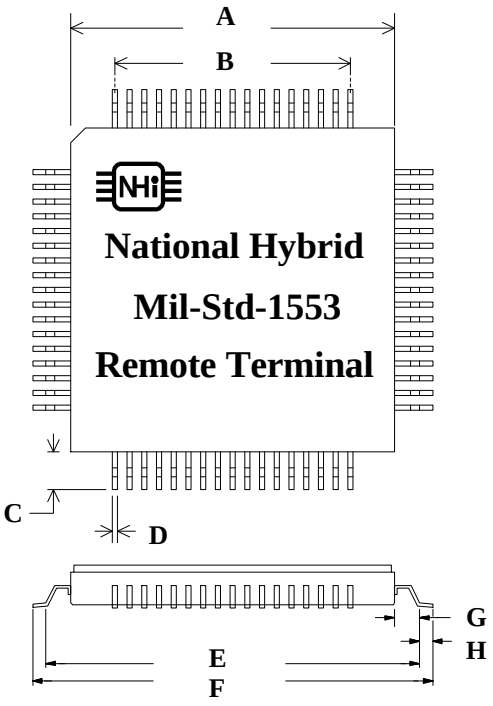
NHI-1576RTFP 66 Pin Flatpack Package Detail

Plug-In Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.830 "**	**0.010 "**
B	**16 EQ SP @**	**0.100 = 1.600 "**
C	**15 EQ SP @**	**0.100 = 1.500 "**
D	**0.900 "**	**0.010 "**
E	**1.100 "**	**0.010 "**
F	**1.330 "**	**0.010 "**
G	**0.225 "**	**MAX**
H	**0.018 " DIA.**	**0.002 "**
J	**0.200 "**	**MIN**

Flatpack Dimensions		
DIM	**TYP (inches)**	**TOL (+/- inches)**
A	**1.850 "**	**0.010 "**
B	**32 EQ SP @**	**0.050 =1.600 "**
C	**0.975 "**	**0.010 "**
D	**0.150 "**	**MAX**
E	**0.085 "**	**0.010 "**
F	**0.500 "**	**MIN**
G	**0.015 "**	**0.002 "**

9.13 FLATPACK GULL WING OPTION

All of the flatpack packages are available with gull wing formed leads. Standard lead forming is per the following diagram.



DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ	0.010
B	16 EQ SP @	0.050 = 0.800
C	0.130	TYP
D	0.018	0.002
E	1.270	MIN
F	1.360	0.015
G	0.085	REF
H	0.045	0.010

9.14 MATING TRANSFORMER CROSS REFERENCE

Device	Power Supply +V	Turns Ratio Direct	Turns Ratio Stub	Technitrol Part Number	DESC SMD
NHI-1553RT	+5V Only	1.00:2.12	1.00:1.50	Q1553-5	5962-9168701
NHI-1554RT	+5V Only	1.00:2.12	1.00:1.50	Q1553-5	5962-9168702
NHI-1561RT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9168703
NHI-1562RT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9168704
NHI-1572RT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9168705
NHI-1576RT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9168706
NHI-1591RT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9168707
NHI-1592RT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9168708

10.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units	Remarks
DC Supply voltage	VCC	-0.3	+7	Volts	
Input voltage	VIN	-0.3	VCC+0.3	Volts	Note 1
DC Input current	IIN	-10	10	Microamps	Note 2
Input zapping	VZAPP	2,000		Volts	Note 3
Latch-up trigger current	ILATCH		200	Milliamps	Note 4
Thermal resistance	TJ		15	Deg. C/W	
Storage temperature	TSTG	-65	150	Deg.C	
Lead temperature	TL	300		Deg. C	

Note 1: VCC referenced to ground
Note 2: Does not include current through internal 64K ohm pull-up/down resistors.
Note 3: As defined for ESDS in Method 3015 0f MIL-STD-883.
Note 4: The latch-up triggering current is the maximum current that will not cause latch-up on an I/O BUFFER.

OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	4.5	+5.5	Volts
Supply current	ICC			
0% TX duty-cycle			90	Milliamps
100% TX duty-cycle			675	Milliamps
Output level on bus	Vpp	7.1	9	Volts
Output level on Stub	Vpp	20	27	Volts
Ambient operating temperature range	TA	-55	+125	Deg. C

I/O TYPES	DESCRIPTION
1	Bi-directional 3-state buffer with 64K ohm pull-up
2	Bi-directional 3-state buffer with 64K ohm pull-up
3	Output Buffer
4	Output Buffer
5	Open-drain Output Buffer
6	Input Buffer with 64K ohm pull-up
7	Input Buffer with 64K ohm pull-down
8	Input Buffer

Signal Name	I/O	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
H_DAT(15:0)	1	DSC_INTPO_L CMDS	3	DTACK_L IRQ_L	5	CLK10	7
I/O_DAT(7:0) I/O_ADR(2:1)	2	MDCDRST PLSCMD I/O_RD_L I/O_WR_L	4	H_ADR(12:1) HRD_L HWRL_L HWRH_L HCS_L RST_L INTPI_L INTACK_L SSF_TF	6	TXINH_A TXINH_B	8

I/O ELECTRICAL CHARACTERISTICS

Parameter	I/O Type	Condition	Min	Max	Units
Low-level input voltage	1,2,6,7,8			0.8	Volts
High-level input voltage	1,2,6,7,8		2		Volts
Low-level output voltage	1	IOL < 8.0 ma		0.4	Volts
	2	IOL < 4.0 ma		0.4	Volts
	3	IOL < 4.0 ma		0.4	Volts
	4	IOL < 6.0 ma		0.4	Volts
	5	IOL < 12.0 ma		0.4	Volts
High-level output voltage	1	IOH > -8.0 ma	2.4		Volts
	2	IOH > -4.0 ma	2.4		Volts
	3	IOH > -4.0 ma	2.4		Volts
	4	IOH > -6.0 ma	2.4		Volts
Input Cap.				10	PF

11.0 TIMING DIAGRAMS

The following diagrams and notes describe the timing of the address, data, and control lines.

11.1 NOTES

1. The address is latched by the NHI-RT on the high-to-low transition of the *HCS line. TADS, TADH, and TASLC are referenced to the high-to-low transition of *HCS.

2. TACK is a function of the contending access performed by the NHI-RT (see host access table).

3. The low-to-high transition of *HRD or I/O *RD terminates the read cycle.

4. The *DTACK line is tri-stated after delay TACKH. Its rise time is a function of the internal 5K ohm pull-up resistor and the external load.

5. While *INTACK is low, *INTPO will be affected by changes in *IRQ.

6. In order to support edge triggered interrupt requests, *IRQ is returned high TINAIRQH ns after *INTACK goes low. If the FIFO is not empty, *IRQ will go low TINAIRQL ns after *INTACK returns high.

7. After *INTACK goes low, the NHI-RT waits TPR ns to allow for the propagation of *INTPO and *INTPI through the daisy chain.

8. The minimum propagation time, TPR, through the daisy chain can be extended by delaying the *HRD signal by any amount, TPRE.

9. If the falling edge of *HRD occurs less than TPR ns after *INTACK, ITACK starts TPR ns after *INTACK, otherwise, ITACK starts after the falling edge of *HRD.

11.2 HOST READ, WRITE, and READ-MODIFY-WRITE TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TADS	ADDRESS SETUP TIME	0	-	ns
TADH	ADDRESS HOLD TIME	200	-	ns
TASLC	ADDRESS STROBE LOW TO COMMAND LOW	0	-	ns
TACKWH	DATA ACKNOWLEDGE LOW TO WRITE HIGH	0	-	ns
TWASH	*HWRL, *HWRH HIGH TO *HCS HIGH	0	-	ns
TACKH	END OF CYCLE TO DATA ACKNOWLEDGE HIGH	0	30	ns
TACKL(1)	NO CONTENTION	0	500	ns
TACKL(2)	WITH CONTENTION	0	800	ns
TACKL(3)	WORST CASE, ONCE AT START OF MESSAGE	0	2.8	us
TDS	DATA SETUP TIME	0	-	ns
TDH	DATA HOLD TIME	0	-	ns
TACKRH	DATA ACKNOWLEDGE LOW TO READ HIGH	0	-	ns
TRDLZ	*HRD LOW TO DATA LOW Z	0	20	ns
TRDHDHZ	*HRD HIGH TO DATA HIGH Z	0	30	ns
TRDHWL	*HRD HIGH TO WRITE LOW	30	-	ns

11.3 I/O READ and TERMINAL ADDRESS READ TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TVARL	VALID ADDRESS TO READ LOW	50	-	ns
TRHVA	ADDRESS VALID AFTER READ HIGH	50	-	ns
TIORW	I/O *RD PULSE WIDTH	190	210	ns
TRHDHZ	I/O *RD HIGH TO DATA HIGH Z	0	200	ns
TRHCML	I/O *RD HIGH TO CMDS LOW	100	-	ns
TCMHRL	CMDS HIGH TO I/O *RD LOW	100	-	ns
TIODHZDL	I/O DATA BUS HIGH Z TO DATA ON BUS	100	-	ns
TRLDS	I/O *RD LOW TO DATA STABLE	-	80	ns
TRHDHZ	I/O *RD HIGH TO DATA IN HIGH Z	0	200	ns
RHIODLZ	I/O *RD HIGH TO DATA BUS IN LOW Z	50	-	ns

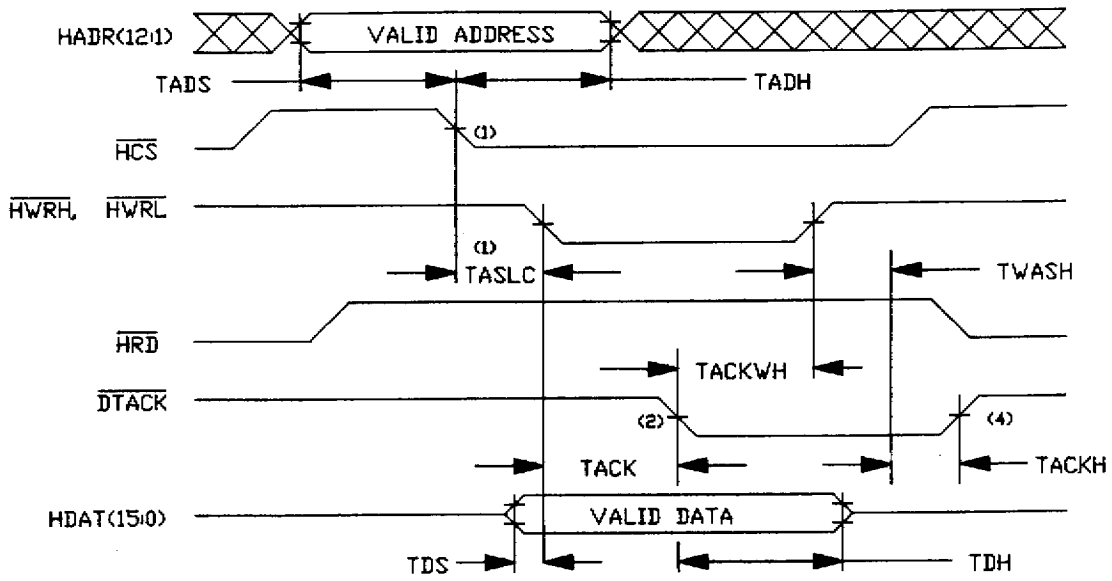
11.4 I/O WRITE and COMMAND WRITE TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TVAWL	VALID ADDRESS TO I/O WRITE LOW	50	-	ns
TWHVA	ADDRESS VALID AFTER I/O WRITE HIGH	50	-	ns
TIOWW	I/O *WR PULSE WIDTH	90	110	ns
TDS	DATA SETUP TIME	25	50	ns
TDH	DATA HOLD TIME	40	80	ns
TCMWW	COMMAND WRITE PULSE WIDTH	290	310	ns
TCMHWL	COMMAND STROBE TO I/O WRITE LOW	40	-	ns
TWHCML	WRITE HIGH TO CMDS LOW	100	-	ns

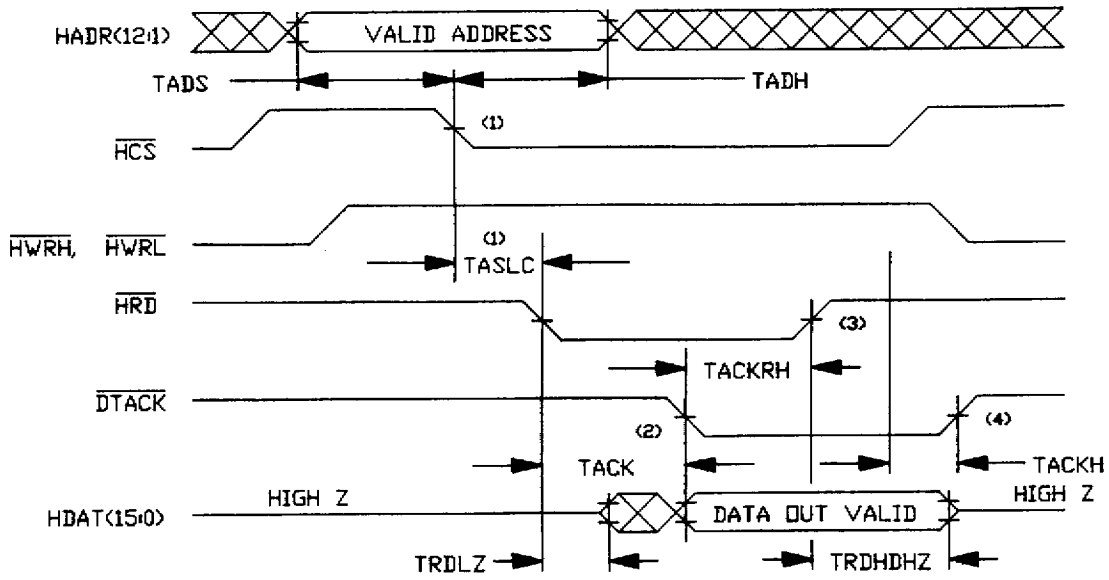
11.5 INTERRUPT ACKNOWLEDGE CYCLE TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TIRQPOH	*IRQ TO *INTPI OUTPUT HIGH	-	20	ns
TPILPOL	*INPI LOW TO *INTPO LOW	-	40	ns
TPIHPOH	*INPI HIGH TO *INTPO HIGH	-	40	ns
TPR	PRIORITY PROPAGATION TIME	400	500	ns
TPRE	PROPAGATION TIME EXTENSION	0	-	ns
TINAIRQH	*INTACK LOW TO *IRQ HIGH	0	200	ns
TINAIRQL	*INTACK HIGH TO NEXT *IRQ LOW	0	200	ns
TINAPOL	*INTACK HIGH TO *INTPO LOW	30	40	ns
TRINAH	*HRD HIGH TO *INTACK HIGH	0	-	ns
ITACK	*HRD LOW TO *DTACK LOW	300	400	ns
TACKRH	*DTACK LOW TO *HRD HIGH	0	-	ns
TRDLZ	*HRD LOW TO DATA IN LOW Z	0	20	ns
TRDHDHZ	*HRD HIGH TO DATA IN HIGH Z	0	30	ns
TACKH	END OF CYCLE TO *DTACK HIGH	0	30	ns

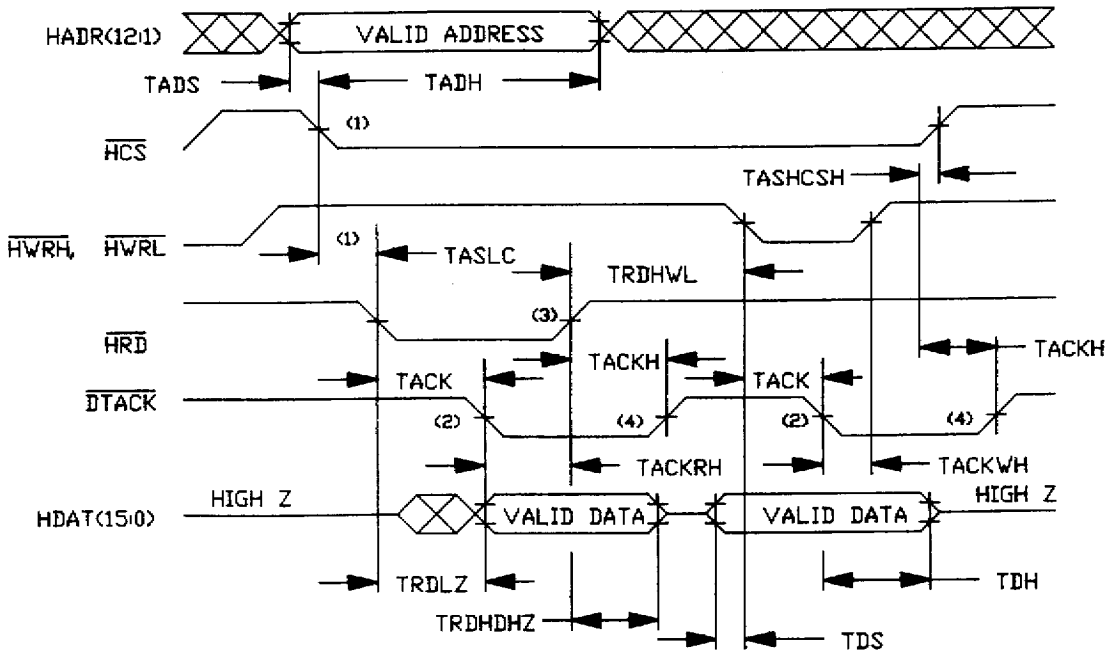
11.6 HOST WRITE CYCLE



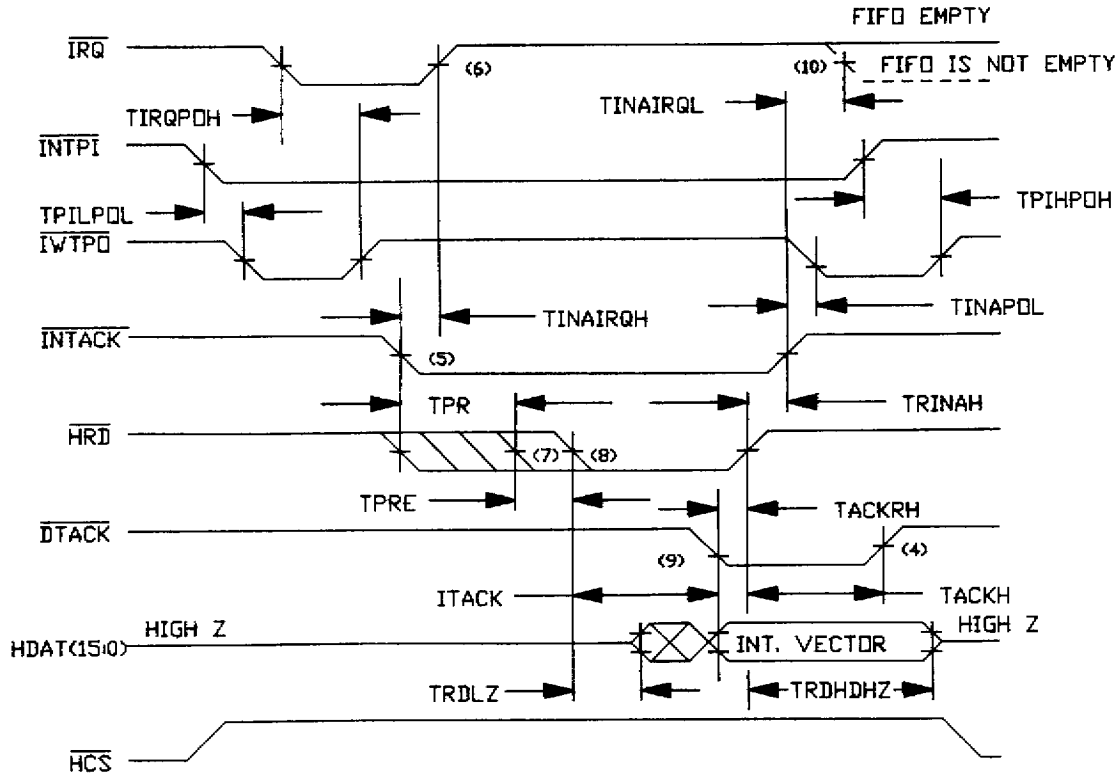
11.7 HOST READ CYCLE



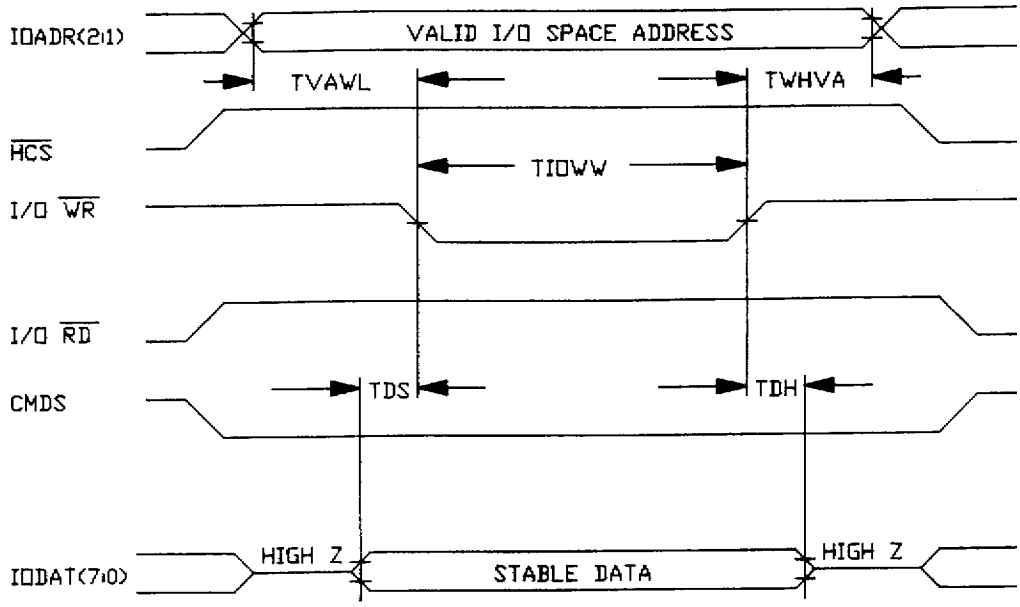
11.8 HOST READ-MODIFY-WRITE CYCLE



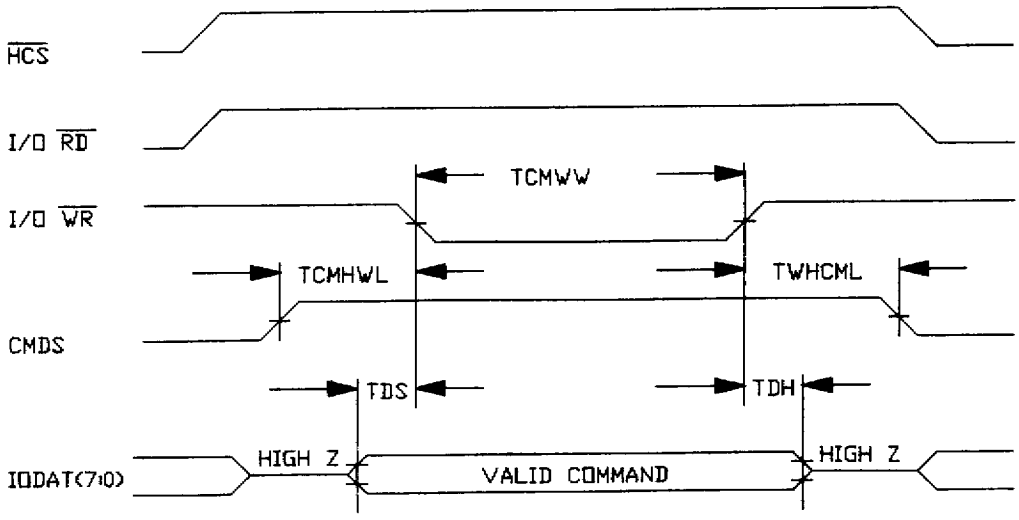
11.9 INTERRUPT ACKNOWLEDGE CYCLE



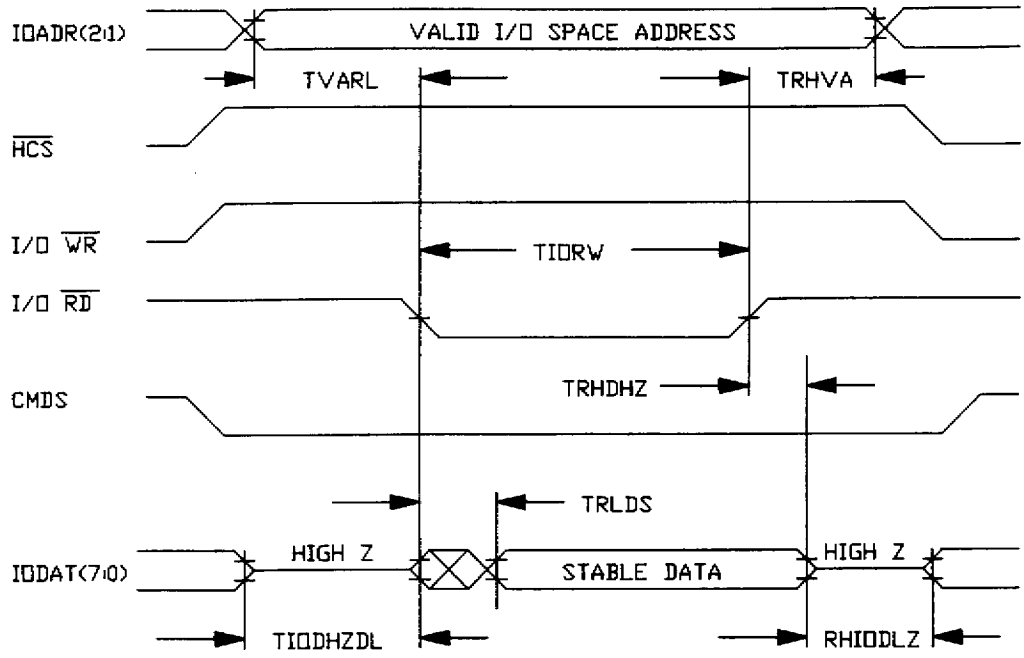
11.10 I/O WRITE CYCLE



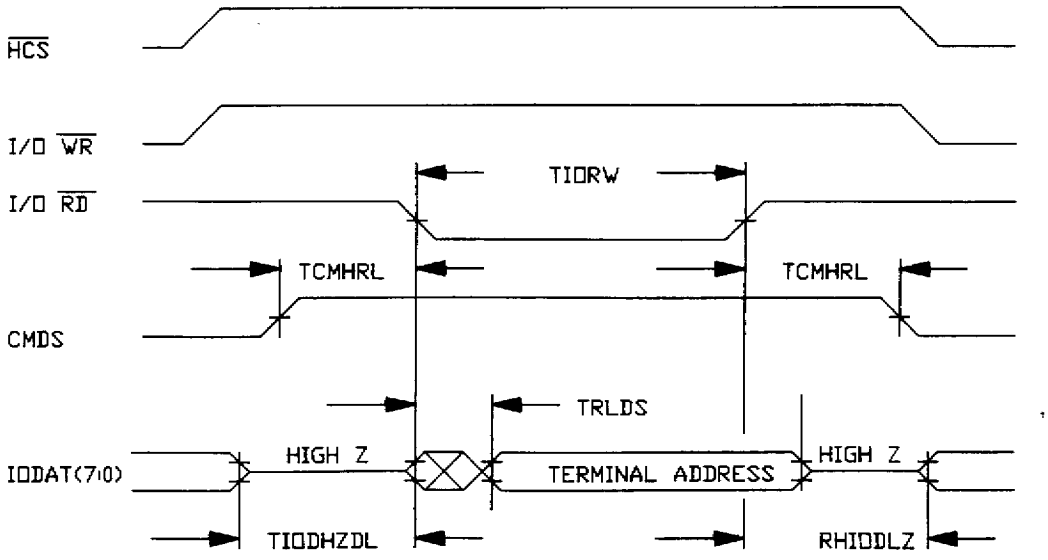
11.11 COMMAND WRITE CYCLE



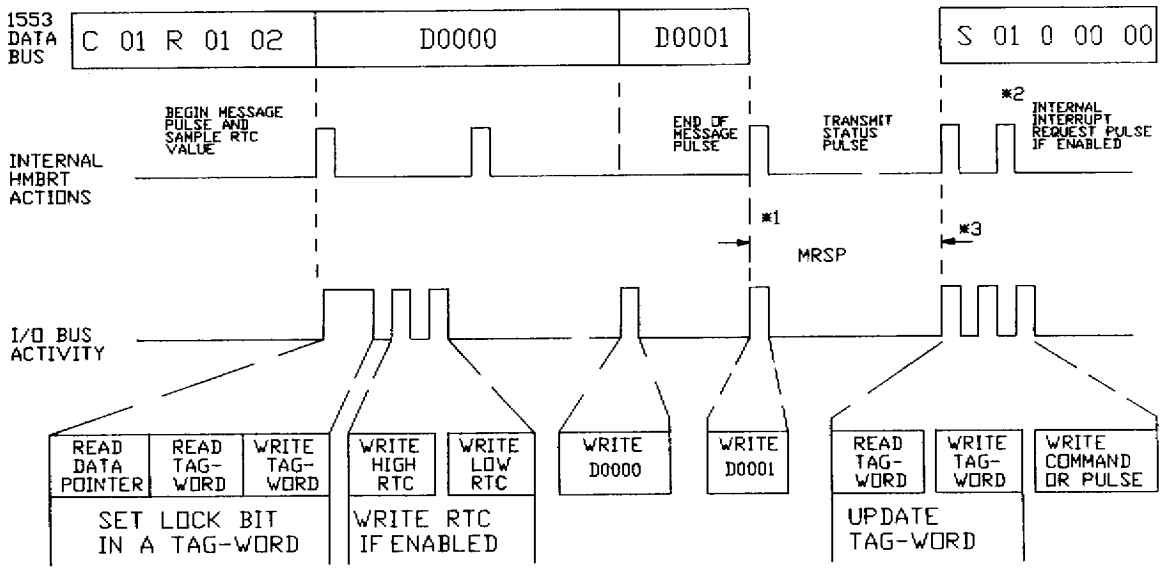
11.12 I/O READ CYCLE



11.13 TERMINAL ADDRESS READ CYCLE



11.14 RECEIVE COMMAND

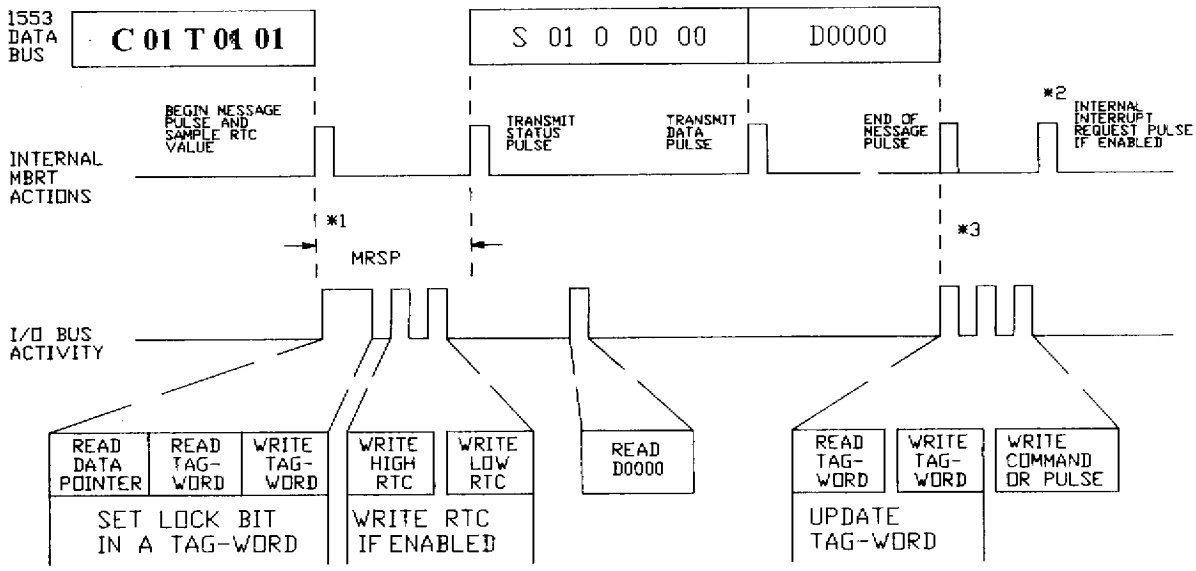


***1 Status Response has a minimum delay of 6.5 uS.**

***2 Internal Interrupt Request Pulse will enter the FIFO immediately if the associated level in not masked, AND, the IRQ_L signal will be activated if IRE bit is set in the control word.**

***3 The exact timing of COMMAND WRITE and IRQ_L activation depends on Host Bus Activity.**

11.15 TRANSMIT COMMAND

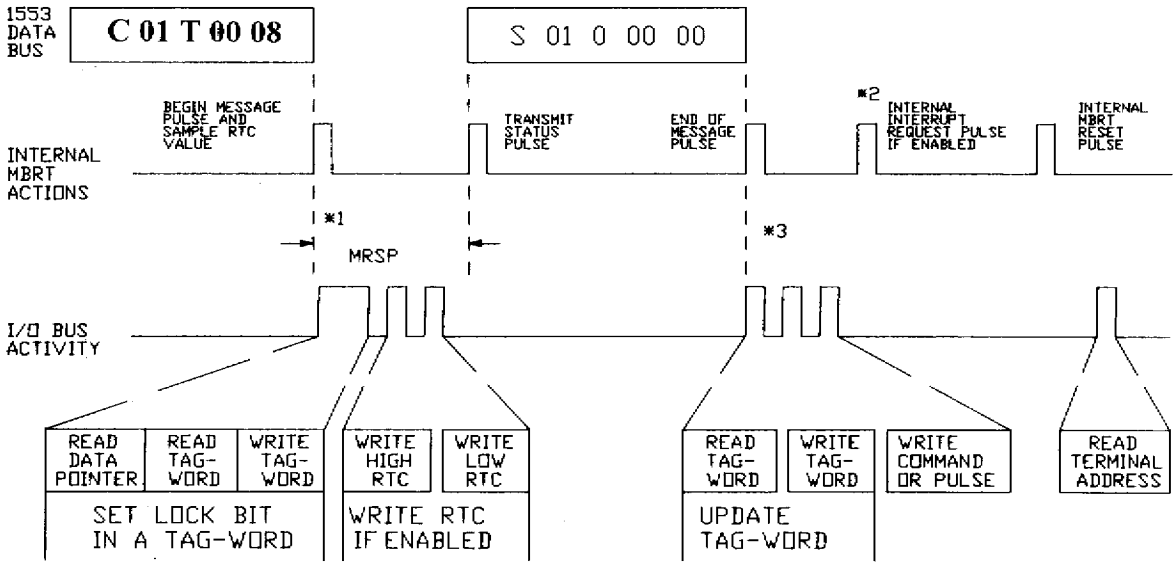


***1 Status Response has a minimum delay of 6.5 uS.**

***2 Internal Interrupt Request Pulse will enter the FIFO immediately if the associated level in not masked, AND, the IRQ_L signal will be activated if IRE bit is set in the control word.**

***3 The exact timing of COMMAND WRITE and IRQ_L activation depends on Host Bus Activity.**

11.16 REMOTE TERMINAL RESET MODE COMMAND



***1 Status Response has a minimum delay of 6.5 uS.**

***2 Internal Interrupt Request Pulse will enter the FIFO immediately if the associated level in not masked, AND, the IRQ_L signal will be activated if IRE bit is set in the control word.**

***3 The exact timing of COMMAND WRITE and IRQ_L activation depends on Host Bus Activity.**

12.0 NHI-1591RT Series Addendum (NHI-1561RT with Additional Configuration Register)

The NHI-1591RT is a drop in replacement to the popular NHI-1561RT Dual Redundant Remote Terminal with the addition of the following features. All new features are enabled via the lower byte (D07-D00) of the Configuration Register at Address 9. In order to maintain the value of bits D15-D08, use a Read-Modify-Write sequence when accessing this register. This will also guarantee software compatibility between the NHI-1561RT and the NHI-1582ET.

Address 9 Configuration Register

D15-D08	D07	D06	D05	D04	D03	D02	D01	D00
Reserved	DBC Ena	Mode 2	Must be Set to logic "0"	Mode 4 Mode 5	Mode 8	TTAG Control	Ext RTC Ena	Bcst Data Block

Configuration 9 Bit Descriptions:

Bit	Bit Value	Description
D15-D08	Reserved	Do not change contents!

D07		Enables response to DBC, Selected Transmitter Shutdown, and Override Transmitter Shutdown Mode Commands.
	0	Specifies that the RT will ignore these mode commands and not respond.
	1	Specifies that the RT will respond to these mode commands according to the pointer word. If the pointer word is zero, the mode command is illegal and the Message Error Bit will be set in the Status Word. (The DBC Bit in the Status Word will always be set to Zero.

D06		Specifies the function of Mode Command 2
	0	Defines mode command 2 as transmit status word according to MIL-STD-1553B.
	1	Defines mode command 2 as a general mode command that can be illegalized if its pointer word is zero.

D04		Specifies the function of Mode Commands 4&5
	0	Defines Mode Command 4 as Transmitter Shutdown according to MIL-STD-1553B.
	1	Defines mode command 4 as a general mode command that can be illegalized if its pointer word is zero.

D04		Specifies the function of Mode Commands 4&5
	0	Defines Mode Command 5 as Override Transmitter Shutdown according to MIL-STD-1553B.
	1	Defines Mode Command 5 as a general mode command that can be illegalized it its pointer word is zero.

D03		Specifies the function of Mode Command 8
	0	Defines Mode Command 8 as a Reset Remote Terminal according to MIL-STD-1553B.
	1	Defines Mode Command 8 as a general mode command that can be illegalized it its pointer word is zero.

D02		Activates Time Tag Transmit/Don't Transmit option. This option is configured by bits 0 and 14 in the corresponding subaddress pointer word as follows:

D02	PTR BIT 14 (RTCENA)	PTR BIT 0	FUNCTION
X	0	X	No time tag
0	1	X	Time tag and transmit Time Tag words (Global - All subaddresses)
1	1	0	Time tag and don't transmit Time Tag words
1	1	1	Time tag and transmit Time Tag words per subaddress.

D01		Enable External Clock for RTC: **Not available on all device types. Please consult factory for additional information.
	0	Default value. Must remain set to zero for the NHI-1591RT. NHI-1591RT does not have input pin for the external clock.
	1	Disables internal Real Time Clock. Enables external clock source for Real Time Clock.

D00		Seperate Broadcast Data Block Enable:
	0	Both Receive and Broadcast Receive messages use the same data tables. Bit 13 of the Tag Word is used to flag a broadcast message.
	1	Specifies that seperate Broadcast Data Blocks will be provided for each broadcast receive subaddress. The pointer table will be increased by 32 additional pointers to accomodate the broadcast data tables.

Additional Features: Minimum response time is reduced to meet the 1553A specification for a 7 uSec maximum response time. (Parity mid bit to Status Sync mid bit zero crossing.)

Overwrite bit in the tag word (bit 5) will function as an overread bit for transmit subaddresses.

NHI-1553RT FP / 883

Reliability Grade

- **883 = Fully Compliant with MIL-PRF-38534**
- **M = Screened to MIL-PRF-38534, -55 to +125 °C**
- **T = Industrial, Tested -55°C to +125°C**
- **Blank = Commercial, -25 to +85 °C**

Package Style

- **Blank = Plug-In**
- **FP = Flatpack**
- **GW = Gull Wing Lead Forming (See page 51)**

- **53RT = Mil-Std-1553, Dual Redundant, Remote Terminal, Separate Vcc for Internal RAM, Hybrid Transceivers**
- **54RT = Mil-Std-1553, Dual Redundant, Remote Terminal, Separate Input Pin for SSFLAG/TFLAG, Hybrid Transceivers**
- **61RT = Mil-Std-1553, Dual Redundant, Remote Terminal, Multichip, Ceramic, Monolithic Transceivers**
- **62RT = MacAir, Dual Redundant, Remote Terminal, Multichip, Ceramic, Universal Monolithic Transceiver Interface**
- **72RT = Same as 53RT except Monolithic Transceivers**
- **75RT = Remote Terminal Protocol, 4K Words SRAM, No Transceivers**
- **76RT = Same as 54RT except Monolithic Transceivers**
- **91RT = Same as 61RT with Seperate Pointer Table for Broadcast Data.**
- **92RT = Same as 62RT with Seperate Pointer Table for Broadcast Data.**

**** SMD Listing: DESC Drawing# 5962-91687**
See QML-38534 for NHI's Manufacturer Qualification Under Mil-H-38534