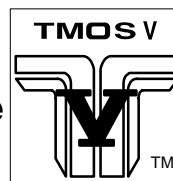


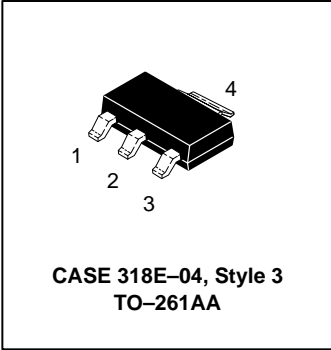
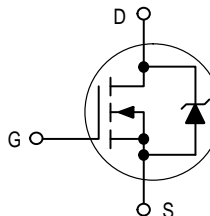
Designer's™ Data Sheet
TMOS V™
SOT-223 for Surface Mount
N-Channel Enhancement-Mode Silicon Gate



MMFT3055VL

TMOS POWER FET
1.5 AMPERES
60 VOLTS
R_{DS(on)} = 0.140 OHM

TMOS V is a new technology designed to achieve an on-resistance area product about one-half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E-FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



New Features of TMOS V

- On-resistance Area Product about One-half that of Standard MOSFETs with New Low Voltage, Low R_{DS(on)} Technology
- Faster Switching than E-FET Predecessors

Features Common to TMOS V and TMOS E-FETS

- Avalanche Energy Specified
- I_{DSS} and V_{DS(on)} Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET
- Available in 12 mm Tape & Reel
Use MMFT3055VLT1 to order the 7 inch/1000 unit reel
Use MMFT3055VLT3 to order the 13 inch/4000 unit reel

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 1.0 MΩ)	V _{DGR}	60	Vdc
Gate-to-Source Voltage – Continuous – Non-repetitive (t _p ≤ 10 ms)	V _{GS} V _{GSM}	± 15 ± 20	Vdc Vpk
Drain Current – Continuous – Continuous @ 100°C – Single Pulse (t _p ≤ 10 μs)	I _D I _D I _{DM}	1.5 1.2 5.0	Adc Adc Apk
Total PD @ T _A = 25°C mounted on 1" sq. Drain pad on FR-4 bd material Total PD @ T _A = 25°C mounted on 0.70" sq. Drain pad on FR-4 bd material Total PD @ T _A = 25°C mounted on min. Drain pad on FR-4 bd material Derate above 25°C	P _D	2.1 1.7 0.94 6.3	Watts mW/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 25 Vdc, V _{GS} = 5.0 Vdc, Peak I _L = 3.4 Apk, L = 10 mH, R _G = 25 Ω)	E _{AS}	58	mJ
Thermal Resistance – Junction to Ambient on 1" sq. Drain pad on FR-4 bd material – Junction to Ambient on 0.70" sq. Drain pad on FR-4 bd material – Junction to Ambient on min. Drain pad on FR-4 bd material	R _{θJA} R _{θJA} R _{θJA}	70 88 159	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design. E-FET, Designer's, and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

MMFT3055VL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60	—	—	Vdc
		—	65	—	mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	—	—	10	μAdc
		—	—	100	
Gate-Body Leakage Current (V _{GS} = ± 15 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0	1.5	2.0	Vdc
		—	3.7	—	mV/°C
Static Drain-to-Source On-Resistance (V _{GS} = 5.0 Vdc, I _D = 0.75 Adc)	R _{DS(on)}	—	0.125	0.14	Ohm
Drain-to-Source On-Voltage (V _{GS} = 5.0 Vdc, I _D = 1.5 Adc) (V _{GS} = 5.0 Vdc, I _D = 0.75 Adc, T _J = 150°C)	V _{DS(on)}	—	—	0.25	Vdc
		—	—	0.24	
Forward Transconductance (V _{DS} = 8.0 Vdc, I _D = 1.5 Adc)	g _{FS}	1.0	3.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	350	pF
Output Capacitance		C _{oss}	—	110	
Transfer Capacitance		C _{rss}	—	29	
SWITCHING CHARACTERISTICS (2)					
Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 1.5 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω)	t _{d(on)}	—	9.5	ns
Rise Time		t _r	—	18	
Turn-Off Delay Time		t _{d(off)}	—	35	
Fall Time		t _f	—	22	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 1.5 Adc, V _{GS} = 5.0 Vdc)	Q _T	—	9.0	nC
		Q ₁	—	1.0	
		Q ₂	—	4.0	
		Q ₃	—	3.5	
SOURCE-DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage (1)	(I _S = 1.5 Adc, V _{GS} = 0 Vdc) (I _S = 1.5 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	—	0.82	Vdc
			—	0.68	
Reverse Recovery Time	(I _S = 1.5 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	—	41	ns
		t _a	—	29	
		t _b	—	12	
Reverse Recovery Stored Charge		Q _{RR}	—	0.066	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	L _D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

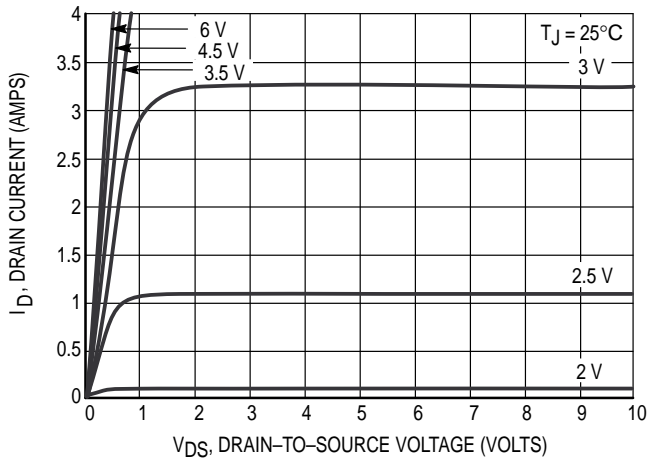


Figure 1. On-Region Characteristics

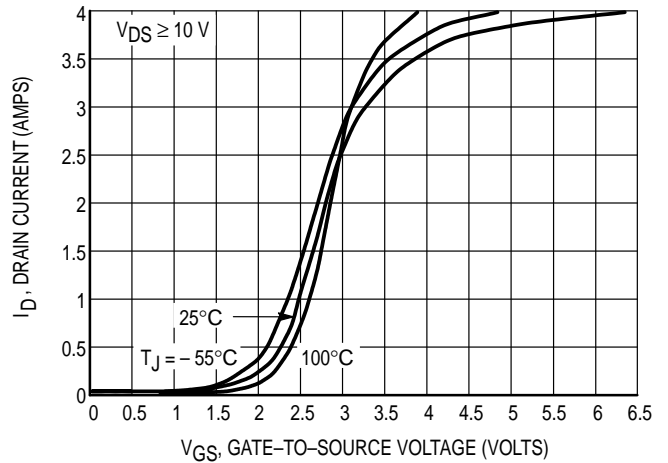


Figure 2. Transfer Characteristics

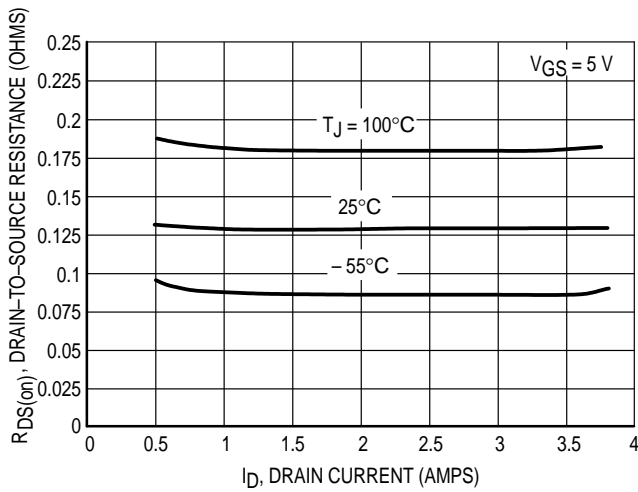


Figure 3. On-Resistance versus Drain Current and Temperature

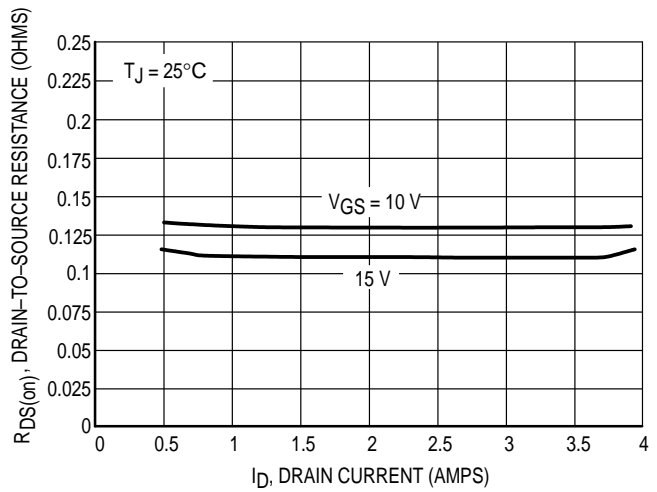


Figure 4. On-Resistance versus Drain Current and Gate Voltage

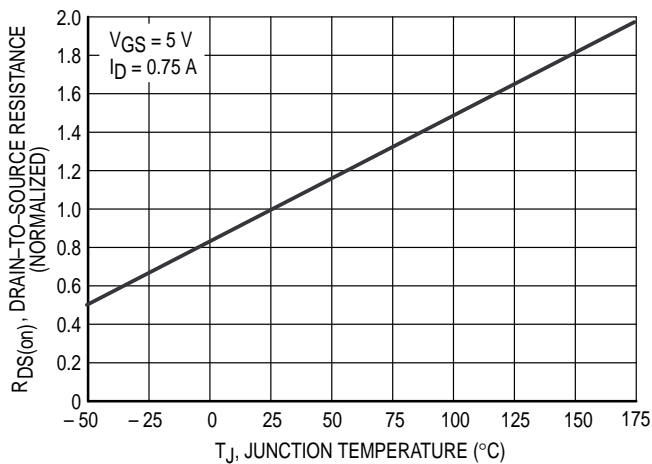


Figure 5. On-Resistance Variation with Temperature

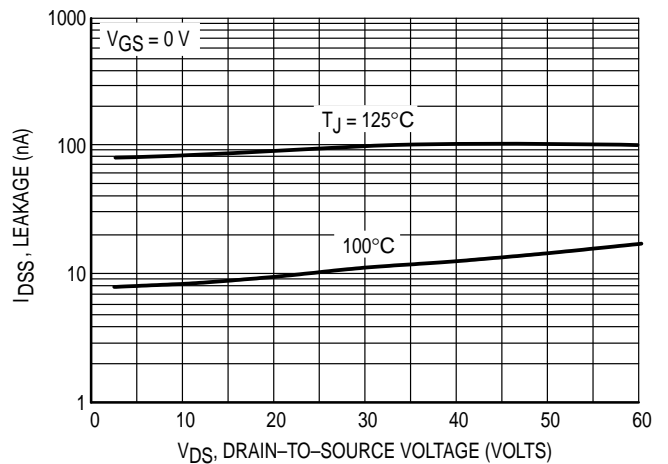


Figure 6. Drain-To-Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP} . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{SGP})$$

$$t_f = Q_2 \times R_G / V_{SGP}$$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{SGP} are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG} / (V_{GG} - V_{SGP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG} / V_{SGP})$$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on-state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by $L di/dt$, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

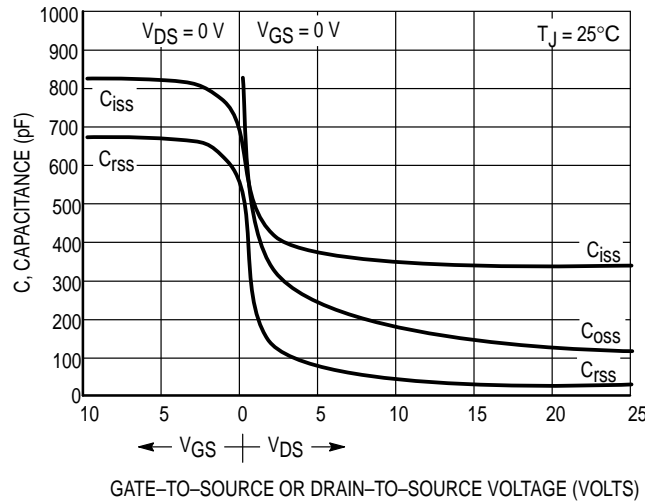


Figure 7. Capacitance Variation

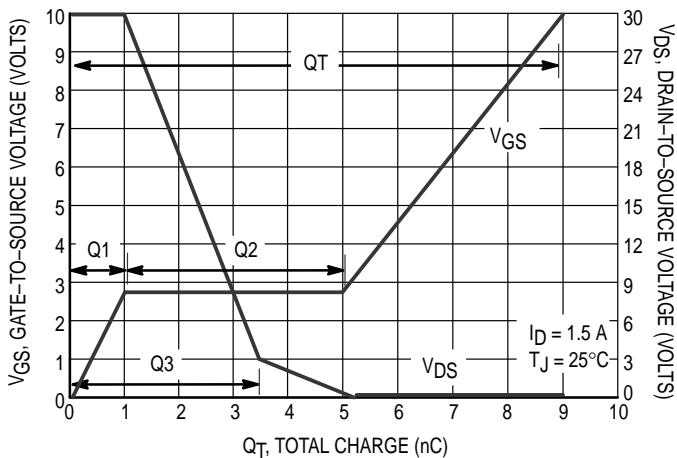


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

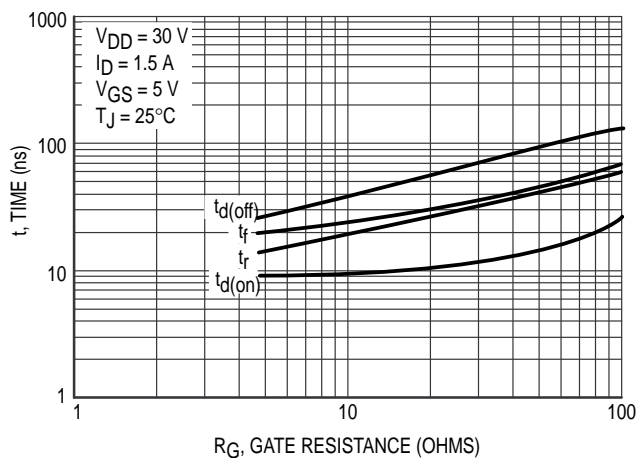


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN-TO-SOURCE DIODE CHARACTERISTICS

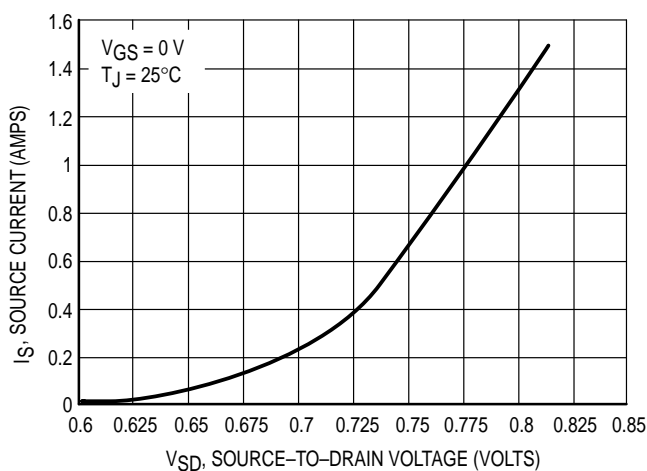


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance—General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r, t_f) do not exceed 10 μs . In addition the total power averaged over a complete switching cycle must not exceed $(T_J(MAX) - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For reli-

able operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

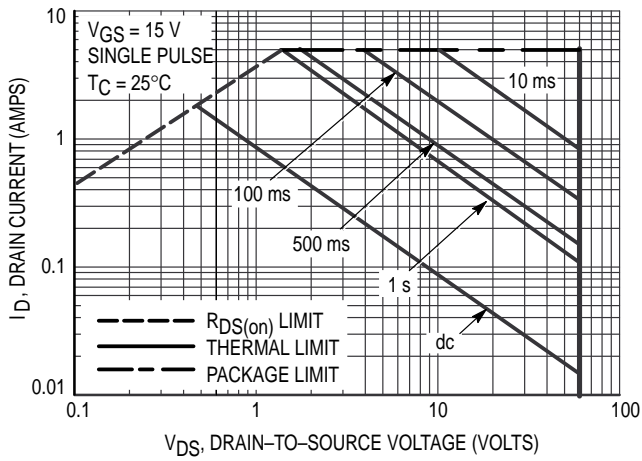


Figure 11. Maximum Rated Forward Biased Safe Operating Area

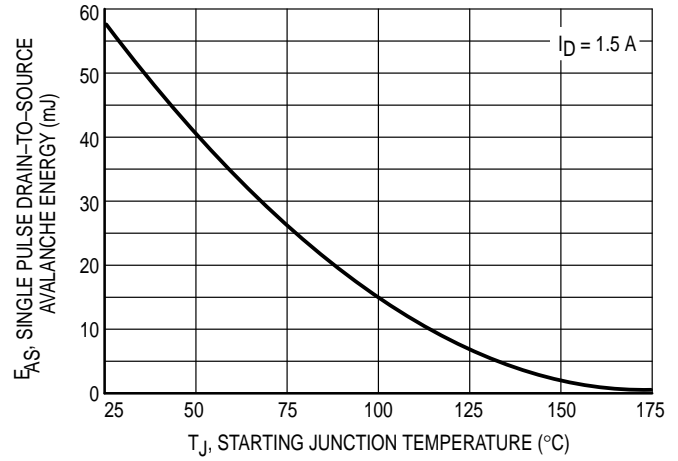


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

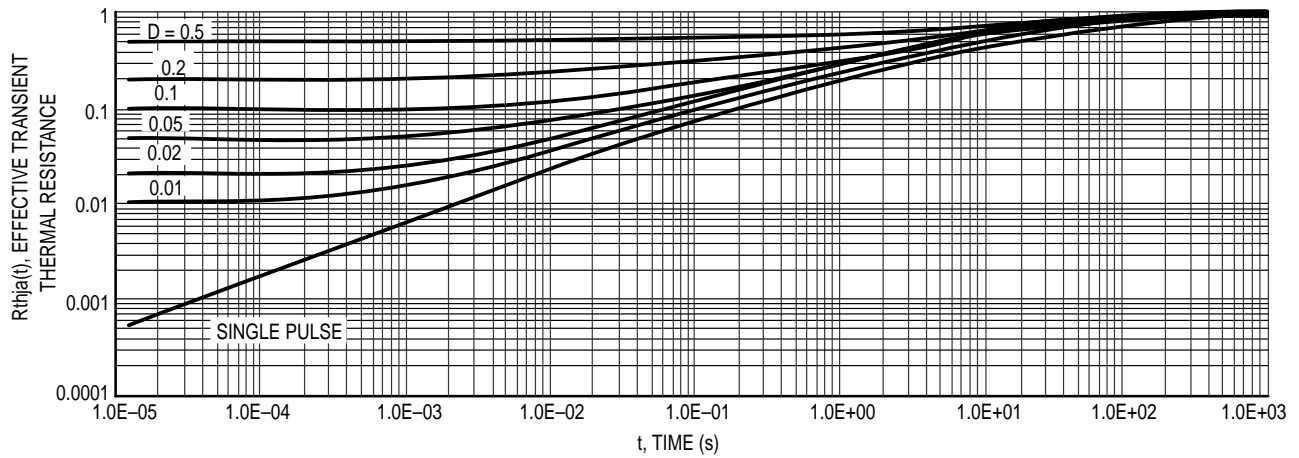


Figure 13. Thermal Response

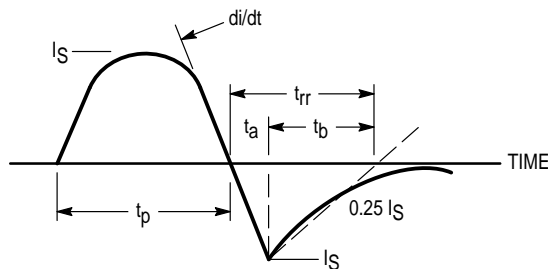


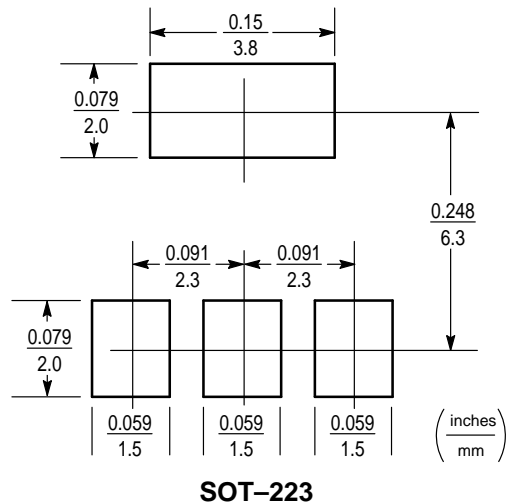
Figure 14. Diode Reverse Recovery Waveform

INFORMATION FOR USING THE SOT-223 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface

between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-223 POWER DISSIPATION

The power dissipation of the SOT-223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SOT-223 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 943 milliwatts.

$$P_D = \frac{175^\circ\text{C} - 25^\circ\text{C}}{159^\circ\text{C/W}} = 943 \text{ milliwatts}$$

The 159°C/W for the SOT-223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 943 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power

dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

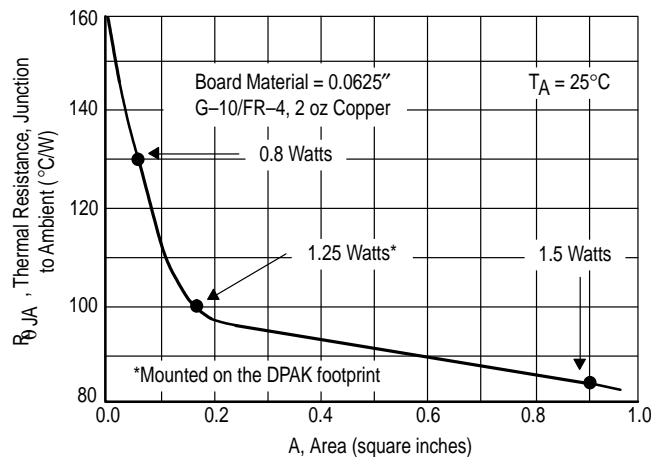


Figure 15. Thermal Resistance versus Drain Pad Area for the SOT-223 Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or

stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT-223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.

- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The

line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

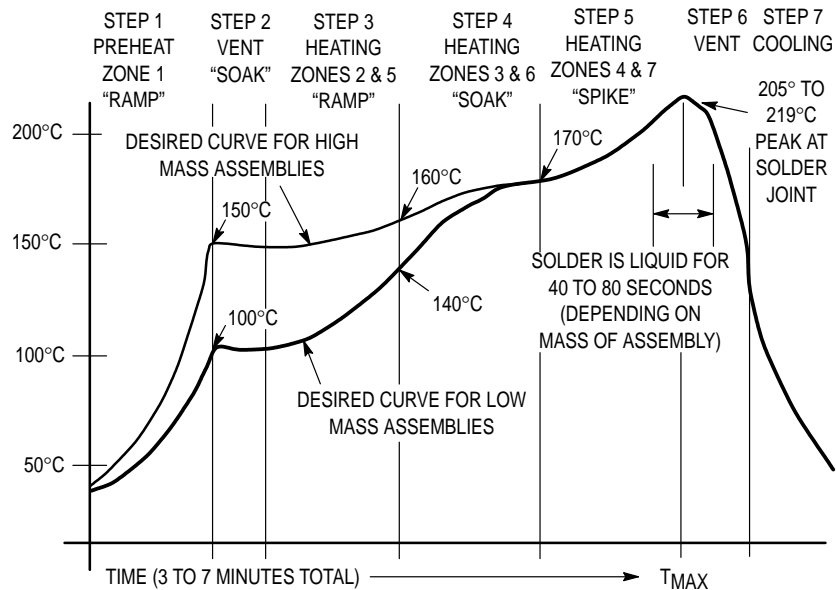
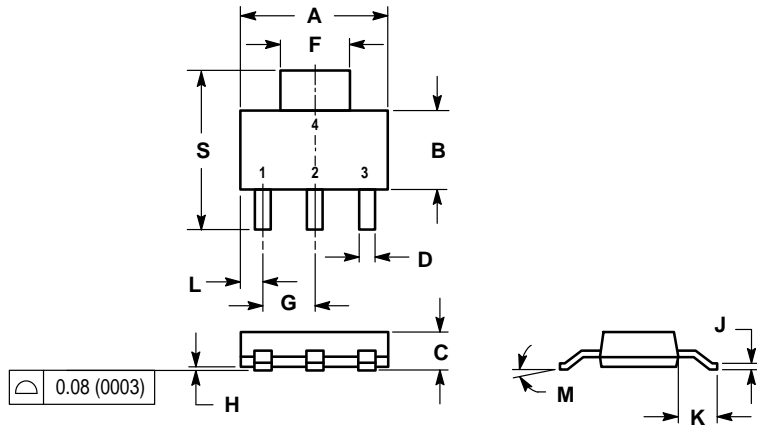


Figure 16. Typical Solder Heating Profile

PACKAGE DIMENSIONS




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0°	10°	0°	10°
S	0.264	0.287	6.70	7.30

- STYLE 3:
- PIN 1: GATE
 - 2: DRAIN
 - 3: SOURCE
 - 4: DRAIN

CASE 318E-04
ISSUE H

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