

# Video Signal Driver for DVD Player Monolithic IC MM1568

## Outline

This IC is a video signal driver that supports 6-ch progressive, and was developed for use in DVD players. It contains a low pass filter that attenuates the noise element during DA conversion, and a 6dB amp and 75ΩX3-line driver (component circuit is 2-line).

It also has a SAG correction pin for reducing output coupling capacitance, and reinforced output pin ESD protection element allows reduction of external ESD protection diodes.

## Features

- (1)Has SAG correction pin.
- (2)3-line drive possible with 75Ω driver.
- (3)Built-in fourth low pass filter.  
 Frequency response: 6.75MHz ±1dB / 27MHz – 27dB min.  
 13.5MHz ±1dB / 54MHz – 24dB min.
- (4)Built-in 6dB amp.
- (5)Built-in power save function.
- (6)S/N=80dB typ.(Y/C mix:74dB typ.)
- (7)For aerial discharge, ±15kV ESD protection withstand pressure (IEC standard)
- (8)Component circuit control pin allows support for RGB signals.

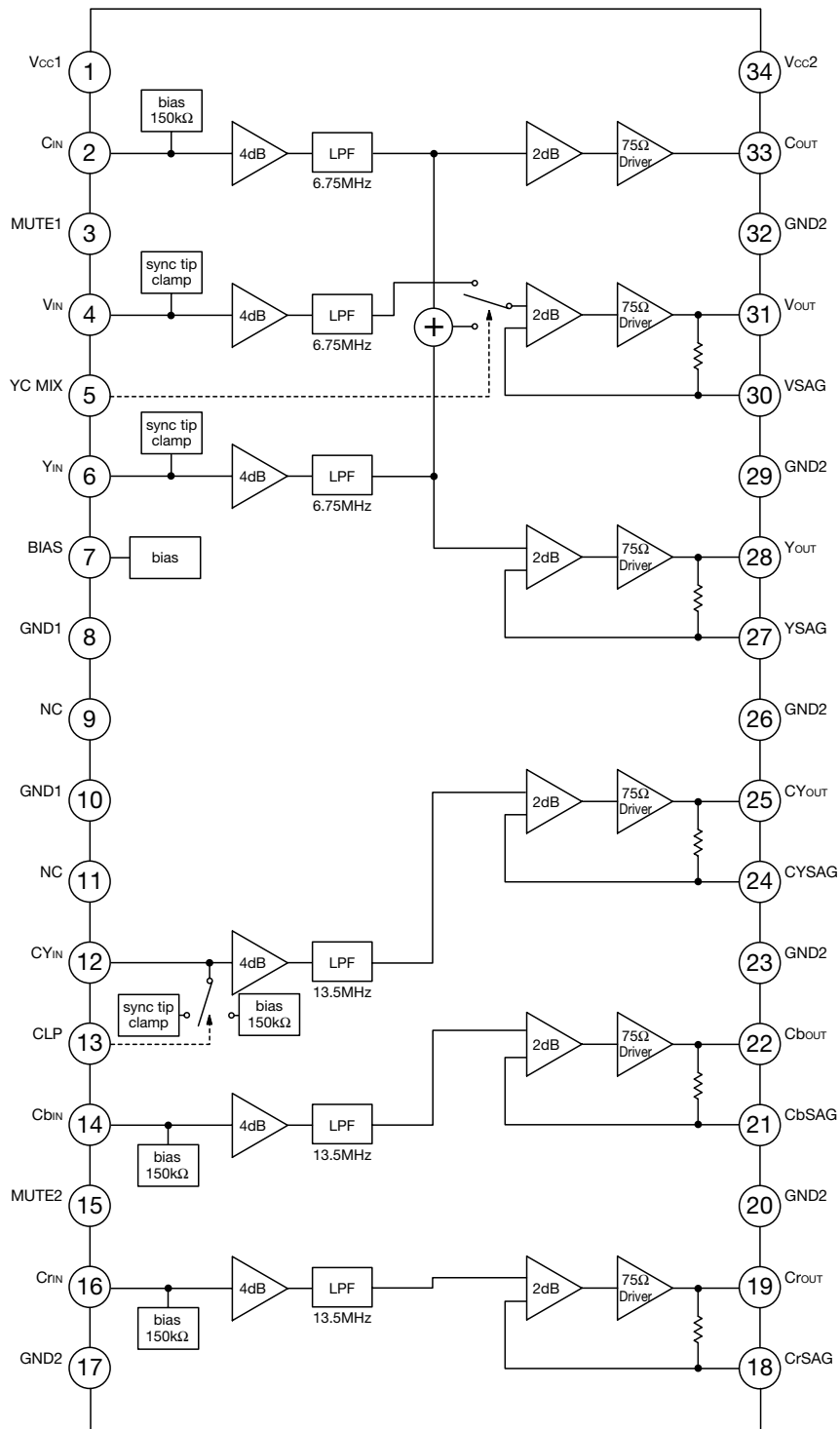
## Package

SSOP-34A

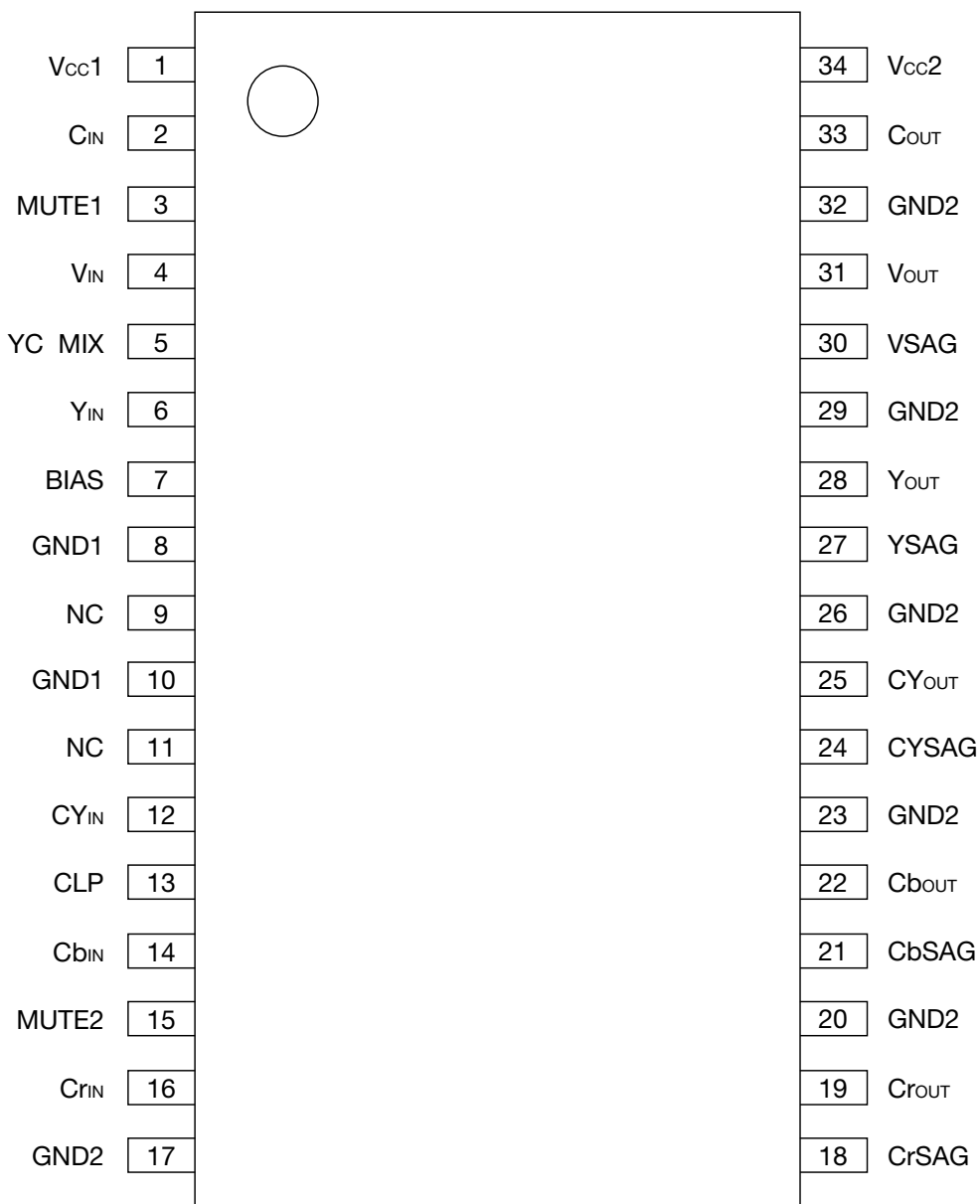
## Applications

- (1)DVD players that support progressive video
- (2)Digital STB
- (3)Other digital video equipment

Block diagram



Pin Assignment



SSOP-34A

1	Vcc1	18	CrSAG
2	CIN	19	CrOUT
3	MUTE1	20	GND2
4	VIN	21	CbSAG
5	YC MIX	22	CbOUT
6	YIN	23	GND2
7	BIAS	24	CYSAG
8	GND1	25	CYOUT
9	NC	26	GND2
10	GND1	27	YSAG
11	NC	28	YOUT
12	CYIN	29	GND2
13	CLP	30	VSAG
14	Cbin	31	VOUT
15	MUTE2	32	GND2
16	CrIN	33	COUT
17	GND2	34	Vcc2

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
1 34	V <sub>CC1</sub> V <sub>CC2</sub>	V <sub>CC</sub>	
2	C <sub>IN</sub>	Croma input	
3 15	MUTE1 MUTE2	Mute Select  Using of Mute and POWER-SAVING	
4 6	V <sub>IN</sub> Y <sub>IN</sub>	Video input (Composite or Y)  Input clamp: Sync tip	
5	YC MIX	YC MIX select	

Pin Description

Pin No.	Pin name	Function	Internal equivalent circuit diagram
7	BIAS	Bias	
8	GND1	GND	
10	GND1		
17	GND2		
20	GND2		
23	GND2		
26	GND2		
29	GND2		
32	GND2		
9	NC	NC	
11	NC	NC	
12	CY <sub>IN</sub>	Luminance input  The input can select Sync tip clamp or Bias.	
13	CLP	Input clamp select	
14	Cb <sub>IN</sub>	Component input	
16	Cr <sub>IN</sub>		

**Pin Description**

Pin No.	Pin name	Function	Internal equivalent circuit diagram
18 21 24 27 30	Crout Cbout CYout Yout Vout	Signal output	
19 22 25 28 31	CrSAG CbSAG CYSAG YSAG VSAG	SAG correction	
33	Cout	Croma output	

**Absolute Maximam Ratings (Ta=25°C)**

Item	Symbol	Rating	Unit
Storage temparature	T <sub>STG</sub>	-65 ~ +150	°C
Operating temparature	T <sub>OPR</sub>	-40 ~ +85	°C
Supply Voltage	V <sub>CC max.</sub>	7	V
Power dissipation *1	P <sub>d</sub>	1.4	W

note \*1 Board mounting power dissipation. Board size 100mmX100mmX1.6mm

**Recommended Operating Conditions**

Item	Symbol	Rating	Unit
Operating temparature	T <sub>OPR</sub>	-40 ~ +85	°C
Operating Voltage	V <sub>CCOP</sub>	4.5 ~ 5.5	V

**Electrical Characteristics** (Unless otherwise specified, Ta=25°C, Vcc=5V)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Consumption current	Icc1	No signal	74	97	126	mA
	Icc2	No signal Mute1:ON	36	51	66	mA
	Icc3	No signal Mute2:ON	39	55	71	mA
	Icc4	No signal Mute1 and Mute2:ON	1	3	5	mA
Croma input	V <sub>CIN</sub>		1.9	2.4	2.9	V
Composite video input	V <sub>VIN</sub>		1.15	1.4	1.65	V
Luminance input	V <sub>YIN, CYIN</sub>		1.15	1.4	1.65	V
Component input	V <sub>CbIN, CrIN</sub>		1.9	2.4	2.9	V
Croma outoput	V <sub>COUt</sub>			2.4		V
Composite video output	V <sub>VOUt</sub>			1.1		V
Luminance output	V <sub>YOuT, CYOuT</sub>			1.1		V
Component output	V <sub>CbOuT, CrOuT</sub>			2.4		V
Control terminal Input current	H I <sub>IHm</sub> *2				350	μA
	L I <sub>ILm</sub> *2				35	μA
Control terminal input voltage	H V <sub>thHm</sub> *2		2.1			V
	L V <sub>thLm</sub> *2				0.7	V
Input impedance	Z <sub>CIN, CbIN, CrIN</sub>		100	150	200	kΩ
Voltage gain	G <sub>1,2,3,5,6</sub> *3	SIN wave:1V f=100kHz	5.7	6.0	6.3	dB
	G <sub>2,1,4,7,8</sub> *3	SIN wave:1V f=100kHz	5.7	6.0	6.3	dB
Frequency characteristic	f <sub>1~5</sub> *3	SIN wave:1V 6.75MHz/100kHz	-1.0	0	1.0	dB
	f <sub>2~5</sub> *3	SIN wave:1V 27MHz/100kHz		-40	-27	dB
	f <sub>3</sub> *3	SIN wave:1V 13.5MHz/100kHz	0	1.0	2.0	dB
	f <sub>4,7,8</sub> *3	SIN wave:0.7V 13.5MHz/100kHz	0	1.0	2.0	dB
	f <sub>5,6~8</sub> *3	SIN wave:1V 54MHz/100kHz		-40	-24	dB
Differential gain	DG <sub>1~3</sub> *3	Staircase signal 1V		0.6	1.0	%
Differential phase	DP <sub>1~3</sub> *3	Staircase signal 1V		0.6	1.0	°
Output dynamic range	DR <sub>n</sub> *3	SIN wave:100kHz THD=1.0%	2.6	3.0		V
Crosstalk	CT <sub>n</sub> *3	f=4.43MHz, 1V		-60	-55	dB
S/N	SN <sub>1,4~5</sub> *3	BW:100k ~ 6MHz		-80		dB
	SN <sub>2~3</sub> *3	BW:100k ~ 6MHz at MIX OUT		-74		dB
	SN <sub>3,6~8</sub> *3			-80		dB
Group delay	t <sub>1GD1~5</sub> *3	at 100kHz		50		ns
	t <sub>2GD6~8</sub> *3	at 100kHz (Component)		30		ns
Group delay deviation	Δt <sub>1GDn</sub> *3	to 3.58MHz		4		ns
	Δt <sub>2GDn</sub> *3	to 4.43MHz		7		ns
	Δt <sub>3GD1~5</sub> *3	to 6MHz		12		ns
	Δt <sub>4GD6~8</sub> *3	to 6MHz (Component)		4		ns
	Δt <sub>5GD6~8</sub> *3	to 12MHz (Component)		12		ns

note \*2 The subscript number "m" is the terminal of right table.

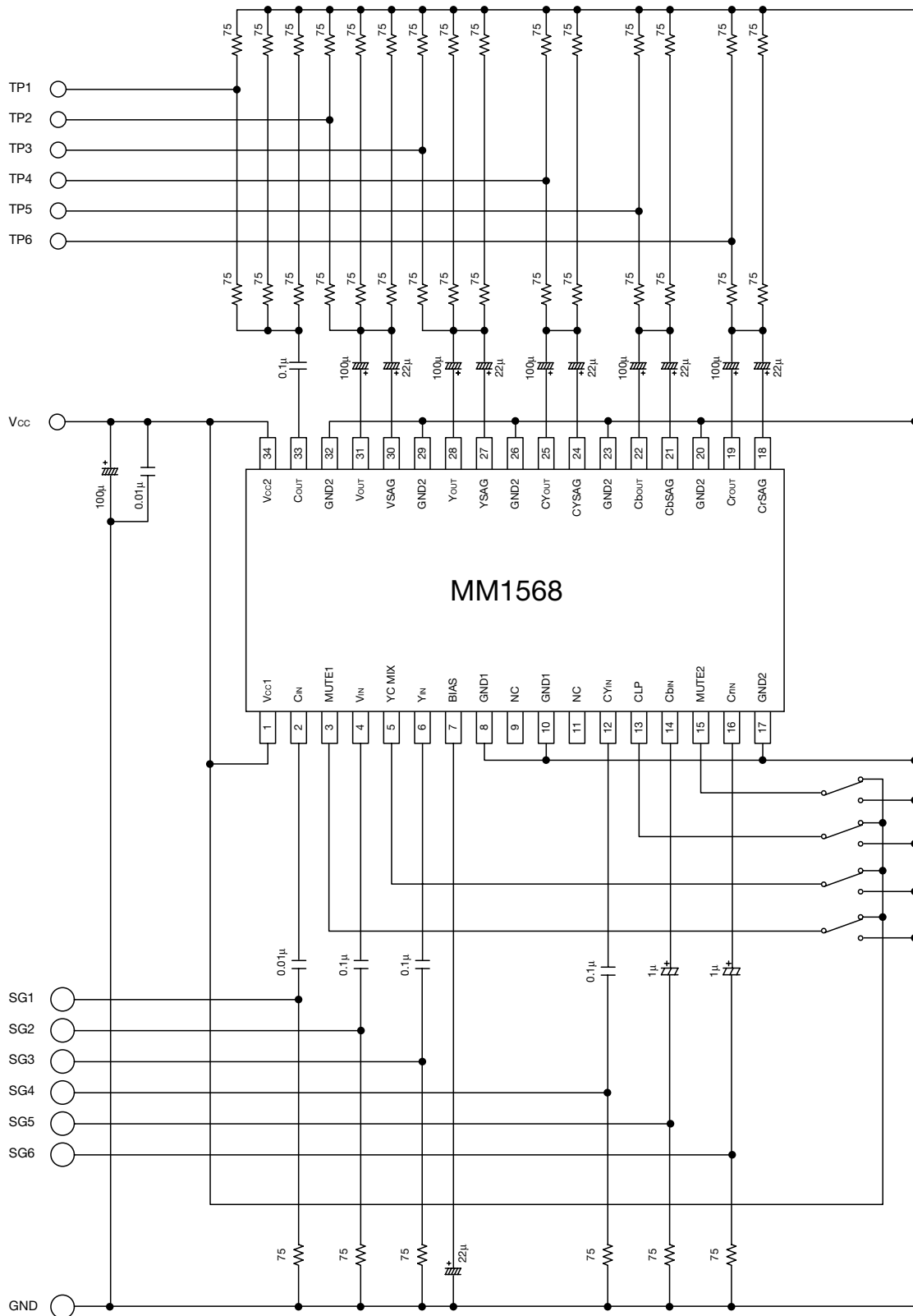
m	Terminal
1	MUTE1
2	MUTE2
3	YC MIX
4	CLP

note \*3 The subscript number "n" is the combination of under table.

n	Input	Output
1	C <sub>IN</sub>	V <sub>OUT</sub>
2	V <sub>IN</sub>	
3	Y <sub>IN</sub>	
4	C <sub>IN</sub>	C <sub>OUT</sub>

n	Input	Output
5	Y <sub>IN</sub>	Y <sub>OUT</sub>
6	CY <sub>IN</sub>	CY <sub>OUT</sub>
7	Cb <sub>IN</sub>	Cb <sub>OUT</sub>
8	Cr <sub>IN</sub>	Cr <sub>OUT</sub>

Test Circuit



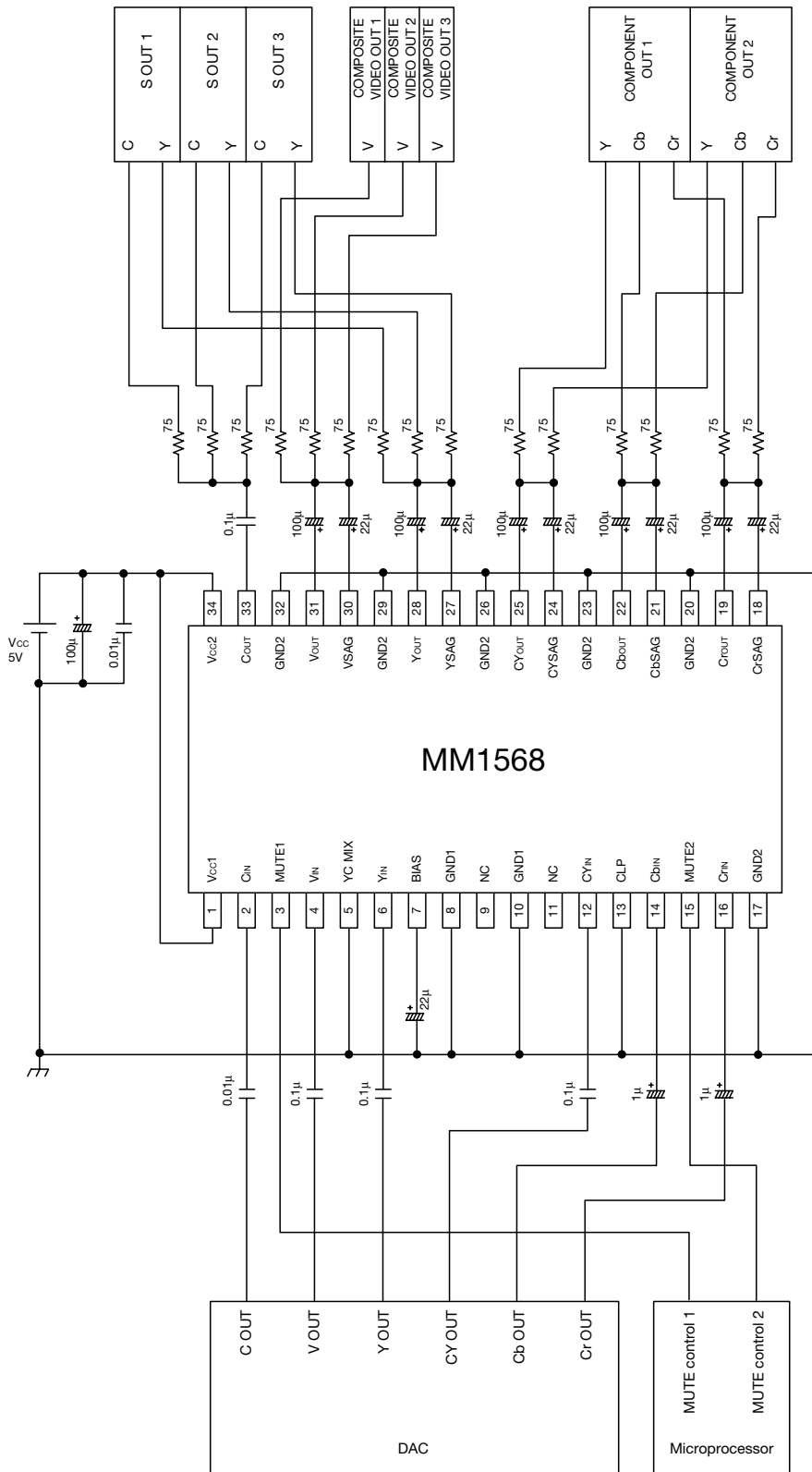


**Switch Control Table**

Input Select	Output Terminal	Control Terminal			
		MUTE1	YC MIX	MUTE2	CLP
MUTE	C <sub>OUT</sub>	Low	*	*	*
C <sub>IN</sub>		High	*	*	*
MUTE	V <sub>OUT</sub>	Low	*	*	*
Y <sub>IN</sub> +C <sub>IN</sub>		High	Low	*	*
V <sub>IN</sub>			High	*	*
MUTE	Y <sub>OUT</sub>	Low	*	*	*
Y <sub>IN</sub>		High	*	*	*
MUTE	C <sub>YOUT</sub>	*	*	Low	*
C <sub>YIN</sub> (Clamp)		*	*	High	Low
C <sub>YIN</sub> (Bias)		*	*		High
MUTE	C <sub>bOUT</sub>	*	*	Low	*
C <sub>bIN</sub>		*	*	High	*
MUTE	C <sub>rOUT</sub>	*	*	Low	*
C <sub>rIN</sub>		*	*	High	*

\* : Don't care

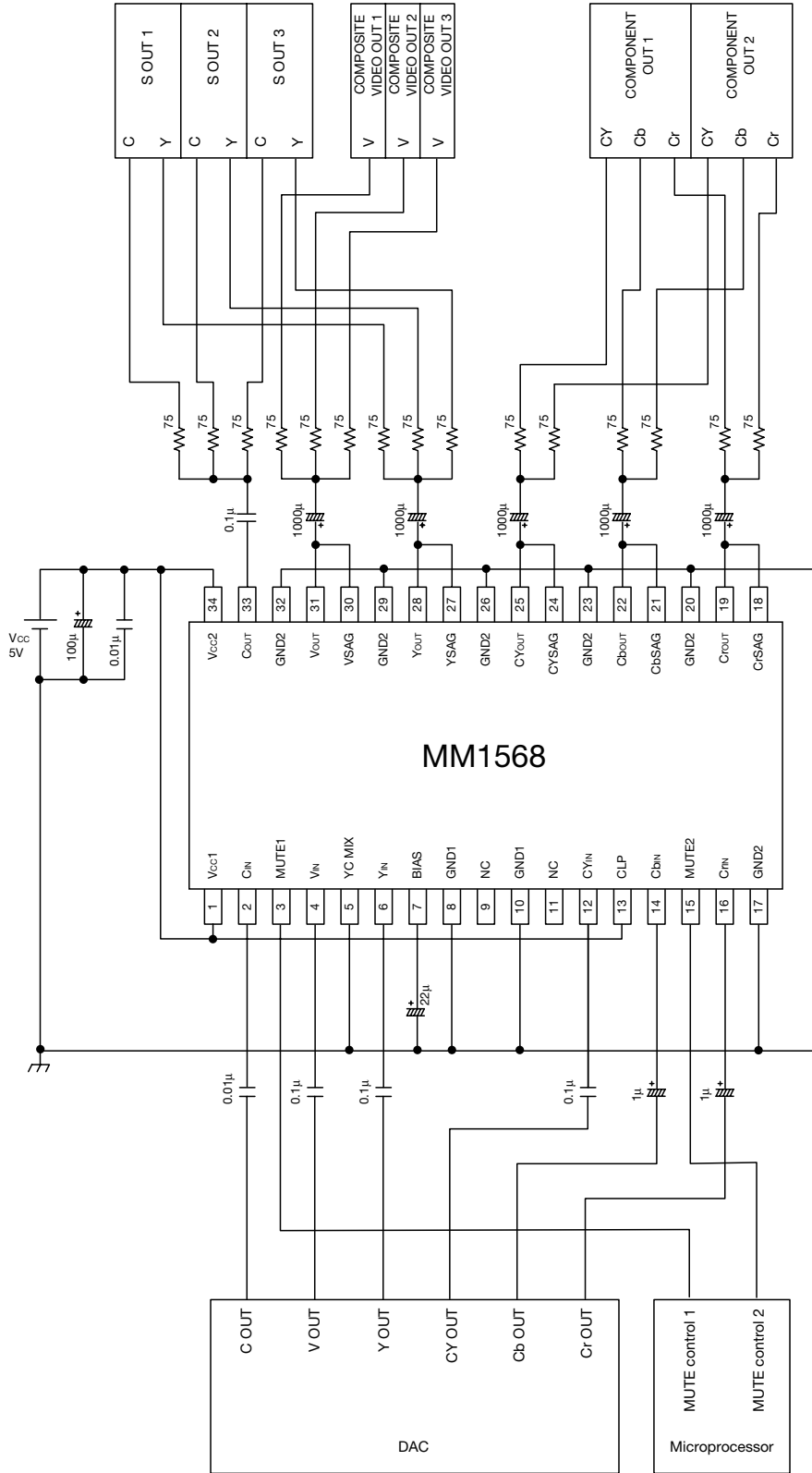
Application Circuit 1



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (34PIN).

Application Circuit 2

■ At unused the SAG correction function



(note) : Please arrange power supply bypass capacitor near the Vcc2 terminal (34PIN).