MH16M40AJD -6

Proto-2

FAST PAGE MODE (16,777,216-WORD BY 40-BIT) DYNAMIC RAM

DESCRIPTION

The MH16M40AJD is a 16M word by 40-bit dynamic RAM module and consists of 10 industry standard 16M X 4 dynamic RAMs in a TSOP package.

The ICs are mounted on both sides of two small PC boards (Ceracom) with the flash gold plating and form a convenient 69-pin WDIP package.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH16M40AJD-6	60	15	30	15	110	2500

- **Utilizes industry standard 16M X 4 DRAMs in TSOP package**
- **Low stand-by power dissipation**
  13mW (Max) ..... CMOS Input level
- **Low operating power dissipation**
  MH16M40AJD - 6 ..... 3242 mW (Max)

- **Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh**
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- **Early-write mode and $\overline{OE}$ to control output buffer impedance**
- **All inputs, output TTL compatible and low capacitance**
- **4096 refresh cycles every 64ms (A_0 - A_{12}) (CbR only)**
- **Includes (0.22uF x 12) decoupling capacitors**
- **5.0V ± 5% Vcc**
- **3.3V Vdd by onboard mounted regulators**
- **TTL input converted to LVTTL by onboard mounted level shifters.**

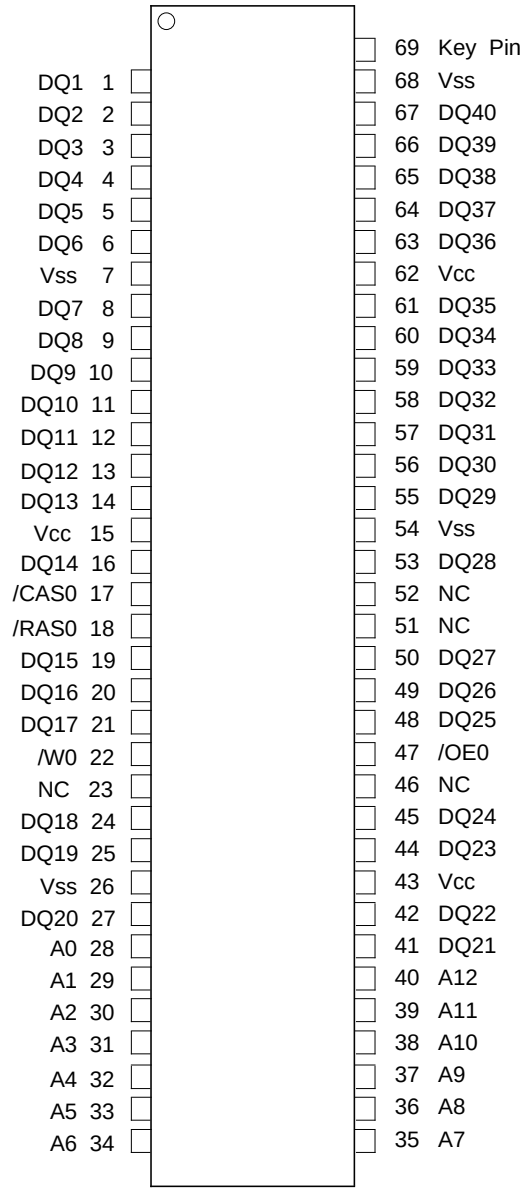
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin Name	Function
A_0-A_{12}	Address Inputs
DQ1-DQ40	Data Inputs / Outputs
$\overline{RAS}$ 0	Row Address Strobe Input
$\overline{CAS}$ 0	Column Address Strobe Input
$\overline{W}$ 0	Write Control Input
$\overline{OE}$ 0	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



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FUNCTION

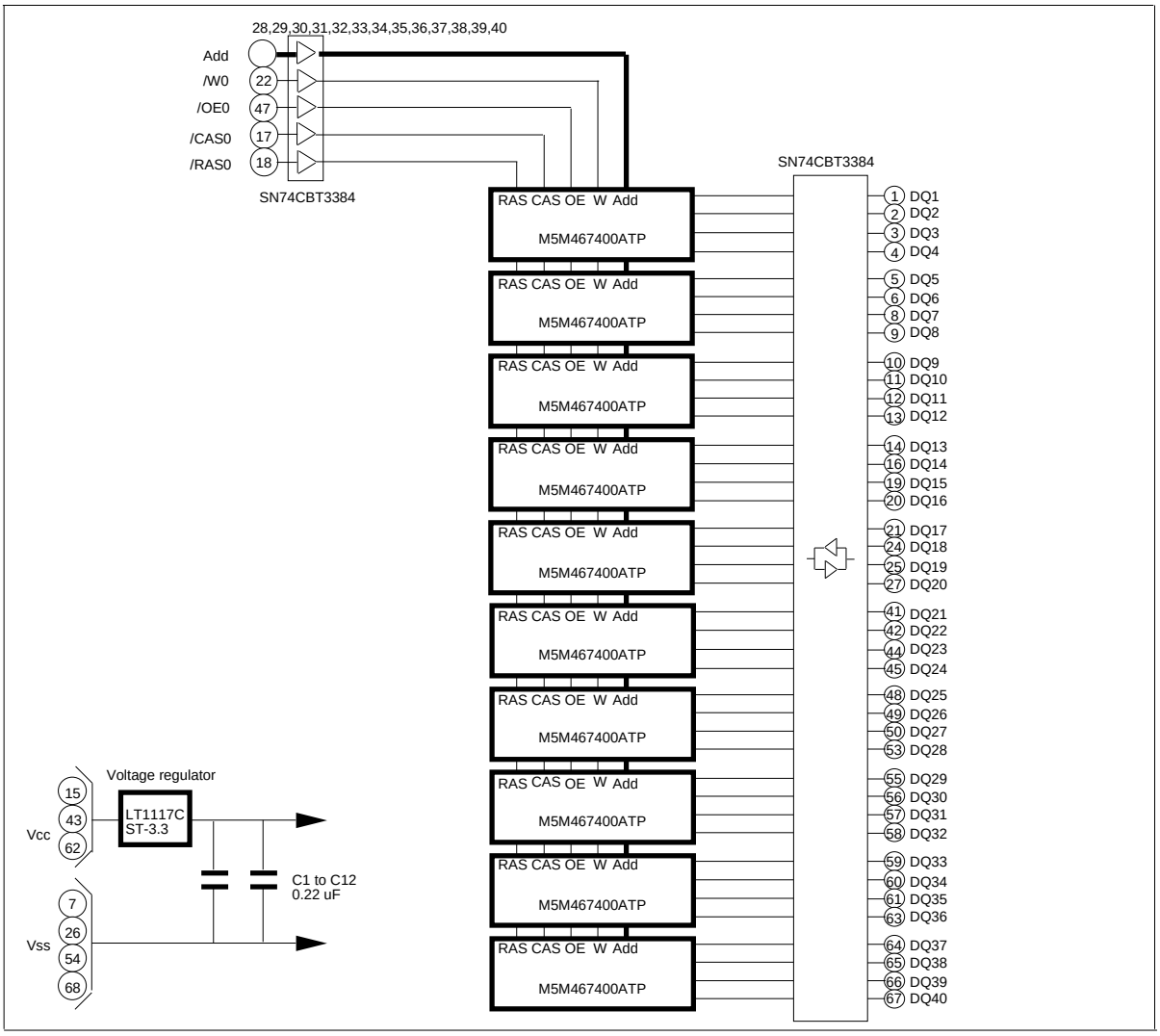
The MH16M40AJD provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{CAS}$ before $\overline{RAS}$ refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
Hidden refresh	ACT	ACT	NAC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5 ~ 7	V
VI	Input voltage		-0.5 ~ 6	V
V0	Output voltage		-0.5 ~ 6	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	15	W
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-40 ~ 100	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.75	5	5.25	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		5.5	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=5V ± 5%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH}=-2mA	2.4		3.6	V
V_{OL}	Low-level output voltage	I_{OL}=2mA	0		0.4	V
I_{OZ}	Off-state output current	Q floating 0V ≦ V_{OUT} ≦ 3.6V	-10		10	uA
I_I	Input current	0V ≦ V_{IN} ≦ 5.25V, Other inputs pins=0V	-5		5	uA
$I_{CC1\ (AV)}$	Average supply current from Vcc operating (Note 3,4)	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			900	mA
I_{CC2}	Supply current from Vcc , stand-by	$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			10	mA
		$\overline{RAS}$= $\overline{CAS}$ ≧ Vcc -0.2			5.4	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	RAS=V_{IL}, CAS cycling t_{PC}=min. output open			800	mA
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			1200	mA

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc4 (AV) and Icc6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta=0 ~ 70°C , Vcc=5V ± 5%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I\ (A)}$	Input capacitance, address inputs	V_I=Vss f=1MHz Vi=25mVrms			20	pF
$C_{I\ (\overline{OE})}$	Input capacitance, $\overline{OE}$ input				20	pF
$C_{I\ (\overline{W})}$	Input capacitance, write control input				20	pF
$C_{I\ (\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				20	pF
$C_{I\ (\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				20	pF
$C_{I/O}$	Input/Output capacitance, data ports				20	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C , Vcc=5V ± 5%, Vss=0V, unless otherwise noted , see notes 5,12,13)

Symbol	Parameter		Limits -6 Min	Limits -6 Max	Unit
t_{CAC}	Access time from $\overline{CAS}$	(Note 6,7)		15	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6,8)		60	ns
t_{AA}	Columu address access time	(Note 6,9)		30	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6,10)		35	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		15	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	15	ns

Note 5: An initial pause of 500 us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{CAS}$ before $\overline{RAS}$ refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to 1TTL loads and 100pF.The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

7: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

8: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

9: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

10: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

11: $t_{OFF(max)}$ and $t_{OEZ\ (max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq$ I ± 10 uAI) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C , Vcc=5V ± 5%, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits -6 Min	Limits -6 Max	Unit
t_{REF}	Refresh cycle time			64	ms
t_{RP}	$\overline{RAS}$ high pulse width		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	20	45	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note15)	15	30	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note17)	0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note17)	0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data	(Note18)	15		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note18)	15		ns
t_T	Transition time	(Note19)	1	50	ns

Note 12: The timing requirements are assumed t_T =5ns.

13: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}$.

15: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

16: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

17: Either t_{DZC} or t_{DZO} must be satisfied.

18: Either t_{CDD} or t_{ODD} must be satisfied.

19: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
t_{RC}	Read cycle time	110		ns
t_{RAS}	$\overline{RAS}$ iow pulse width	60	10000	ns
t_{CAS}	$\overline{CAS}$ iow pulse width	15	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ iow	60		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ iow	15		ns
t_{RCS}	Read Setup time after $\overline{CAS}$ high	0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ iow (Note 20)	0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ iow (Note 20)	10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ iow	15		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ iow	15		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
t_{WC}	Write cycle time	110		ns
t_{RAS}	$\overline{RAS}$ iow pulse width	60	10000	ns
t_{CAS}	$\overline{CAS}$ iow pulse width	15	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ iow	60		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ iow	15		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 22)	0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ iow	10		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ iow	15		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ iow	15		ns
t_{WP}	Write pulse width	10		ns
t_{DS}	Data setup time before $\overline{CAS}$ iow or $\overline{W}$ iow	0		ns
t_{DH}	Data hold time after $\overline{CAS}$ iow or $\overline{W}$ iow	10		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ iow	15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note21)	150		ns
t_{RAS}	$\overline{RAS}$ low pulse width	95	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	50	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	95		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	50		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note22)	30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note22)	75		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note22)	45		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		ns
t_{WP}	Write pulse width	10		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		ns
t_{DH}	Data hold time after $\overline{W}$ low	10		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		ns

Note 21: t_{RWC} **is specified as** $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

22: t_{WCS}, t_{CWD}, t_{RWD} **and** t_{AWD} **and,** t_{CPWD} **are specified as reference points only. If** $t_{WCS} \geqq t_{WCS(min)}$ **the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If** $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ **and** $t_{CPWD} \geqq t_{CPWD(min)}$ **(for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to** V_{IH} **) is indeterminate.**

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	75		ns
t_{RAS}	$\overline{RAS}$ iow pulse width for read write cycle (Note24)	100	102400	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note25)	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ iow (Note22)	35		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: $t_{RAS(min)}$ **is specified as two cycles of $\overline{CAS}$ input are performed.**

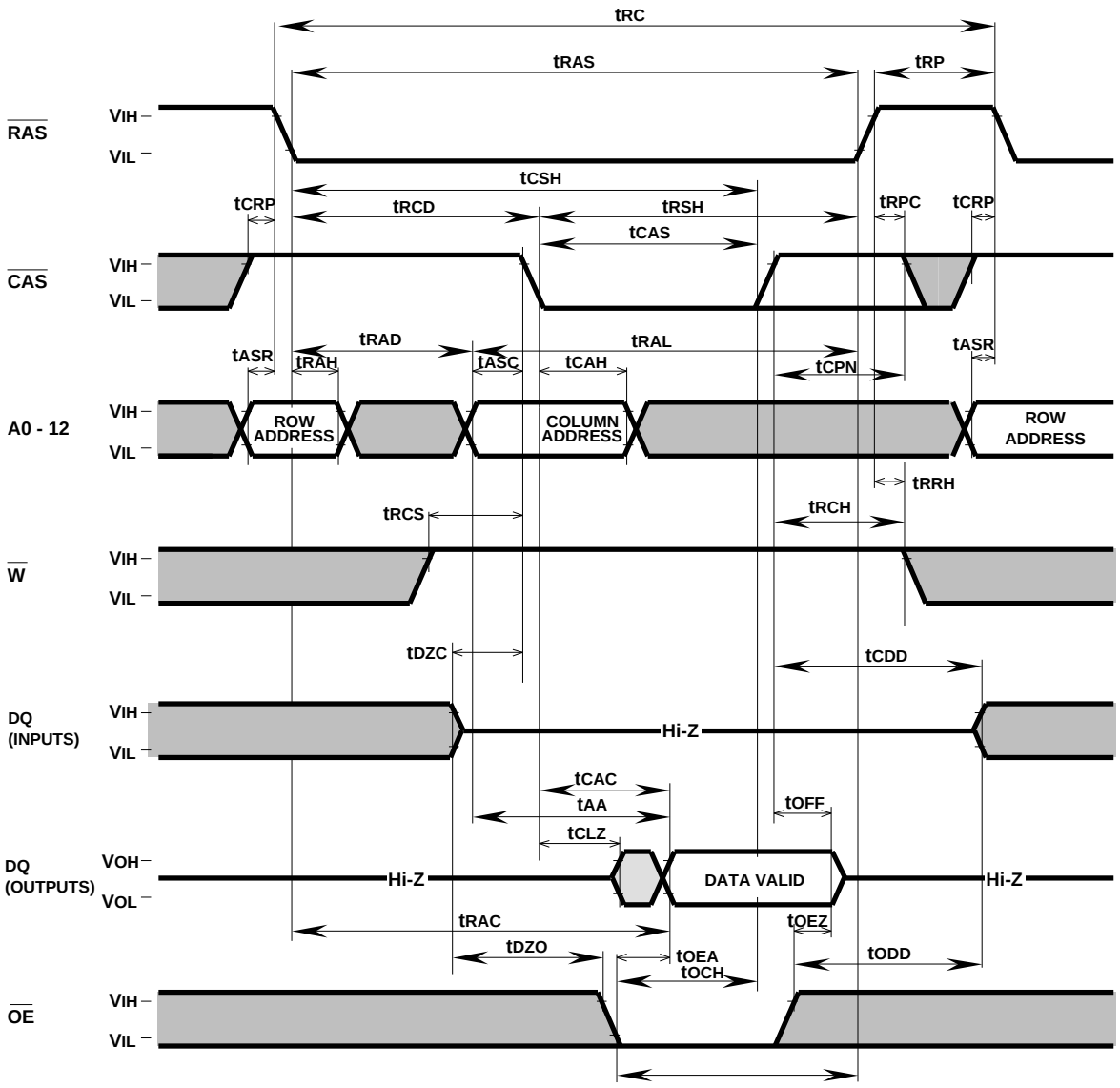
25: $t_{CP(max)}$ **is specified as a reference point only. If tCP** $\geqq$ **tCP(max),access time is controlled exclusively by tCAC.**

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits		Unit
		-6		
		Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

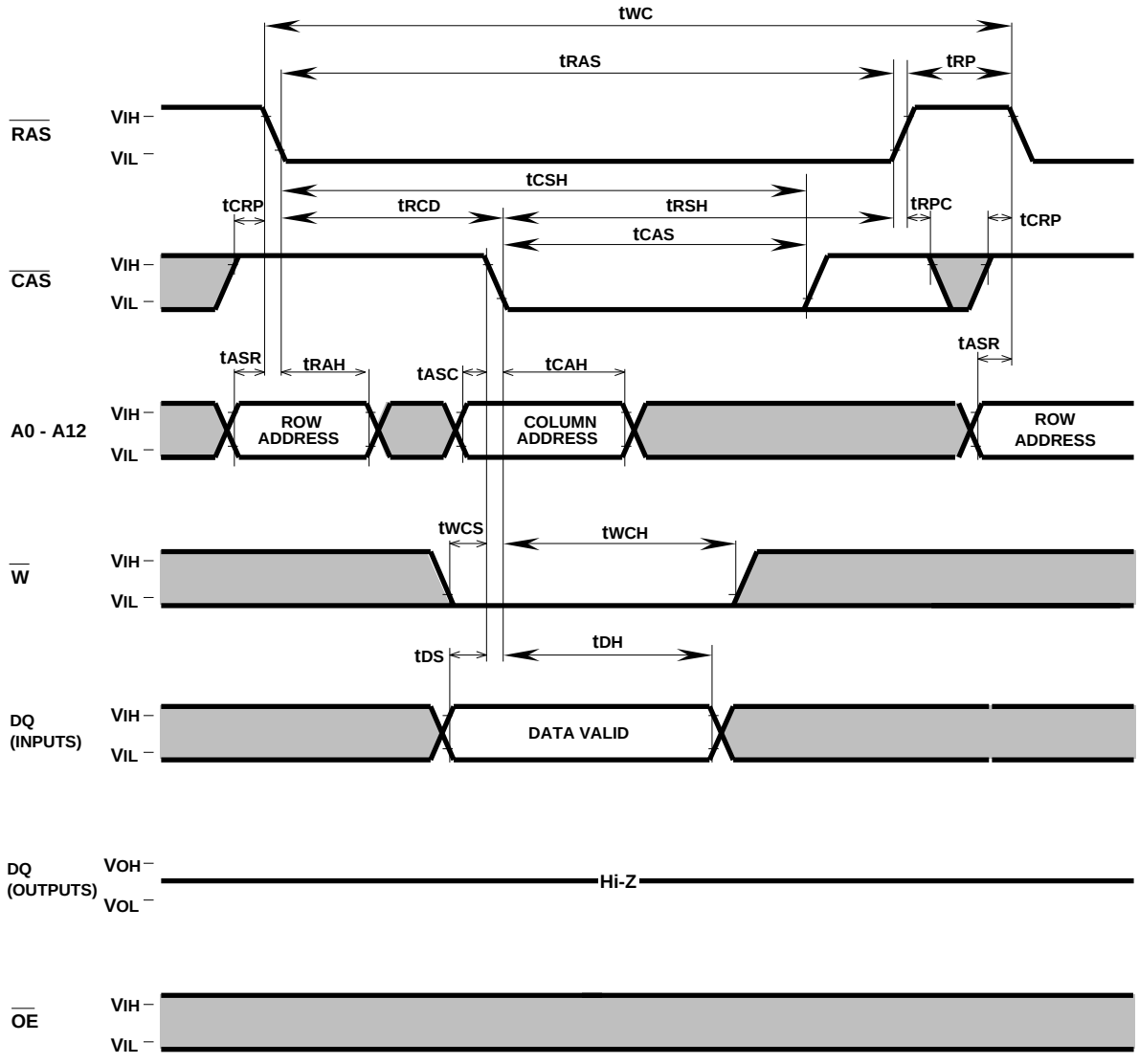
Timing Diagrams (Note 27)
Read Cycle



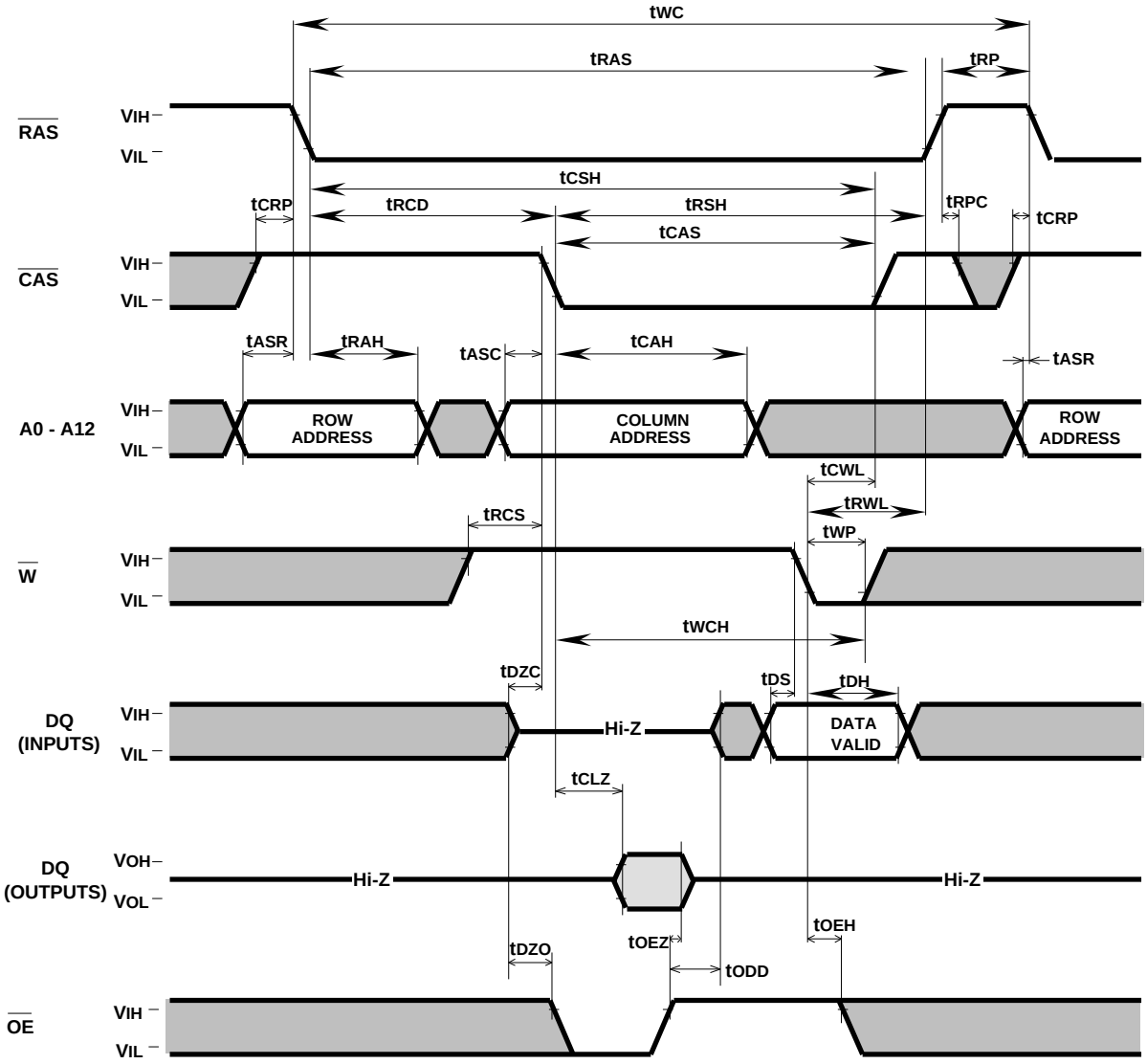
Note 27

Indicates the don't care input.
VIH(min) ≦ VIN ≦ VIH(max) or
VIL(min) ≦ VIN ≦ VIL(max)
Indicates the invalid output.

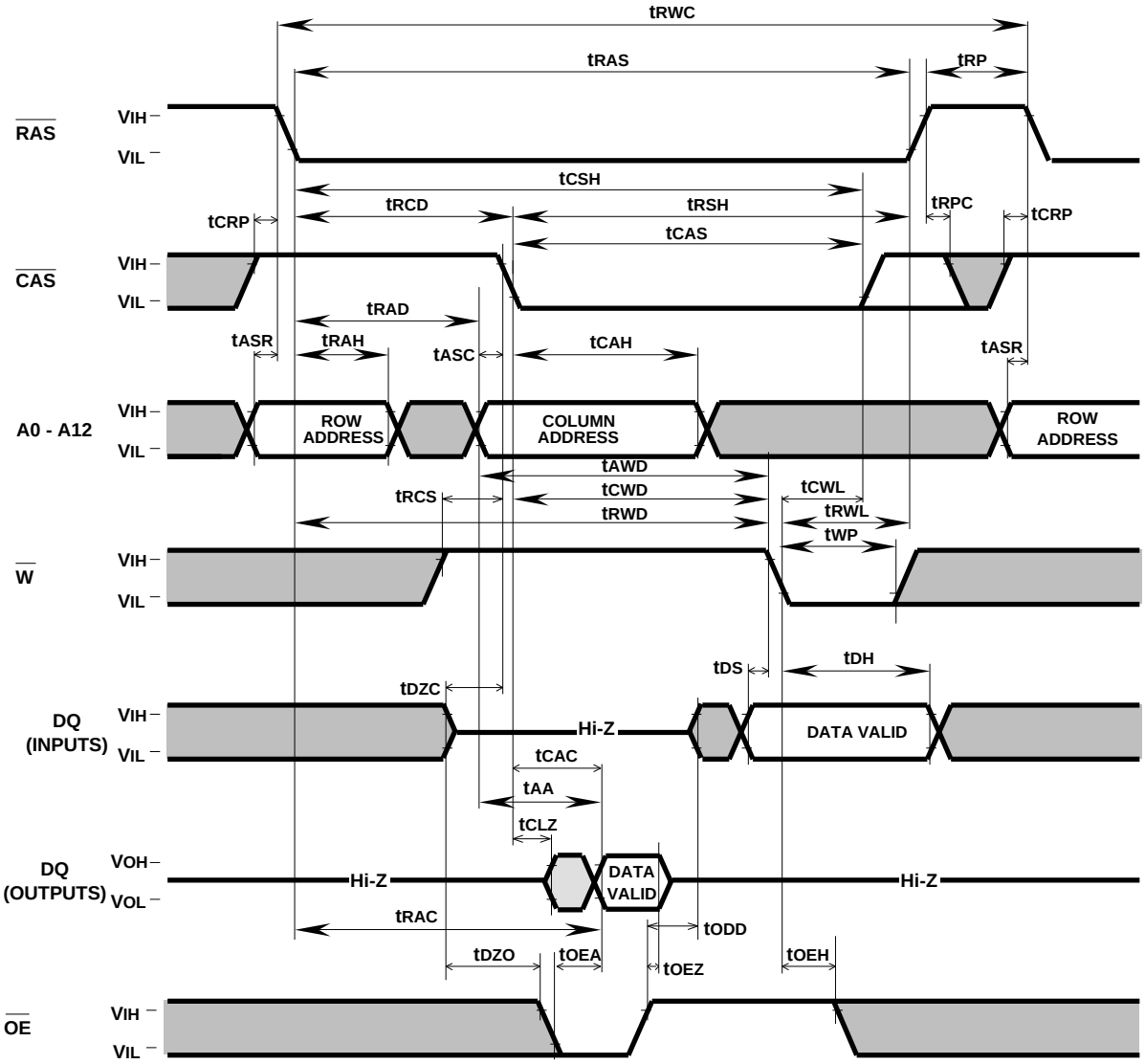
Write Cycle (Early write)



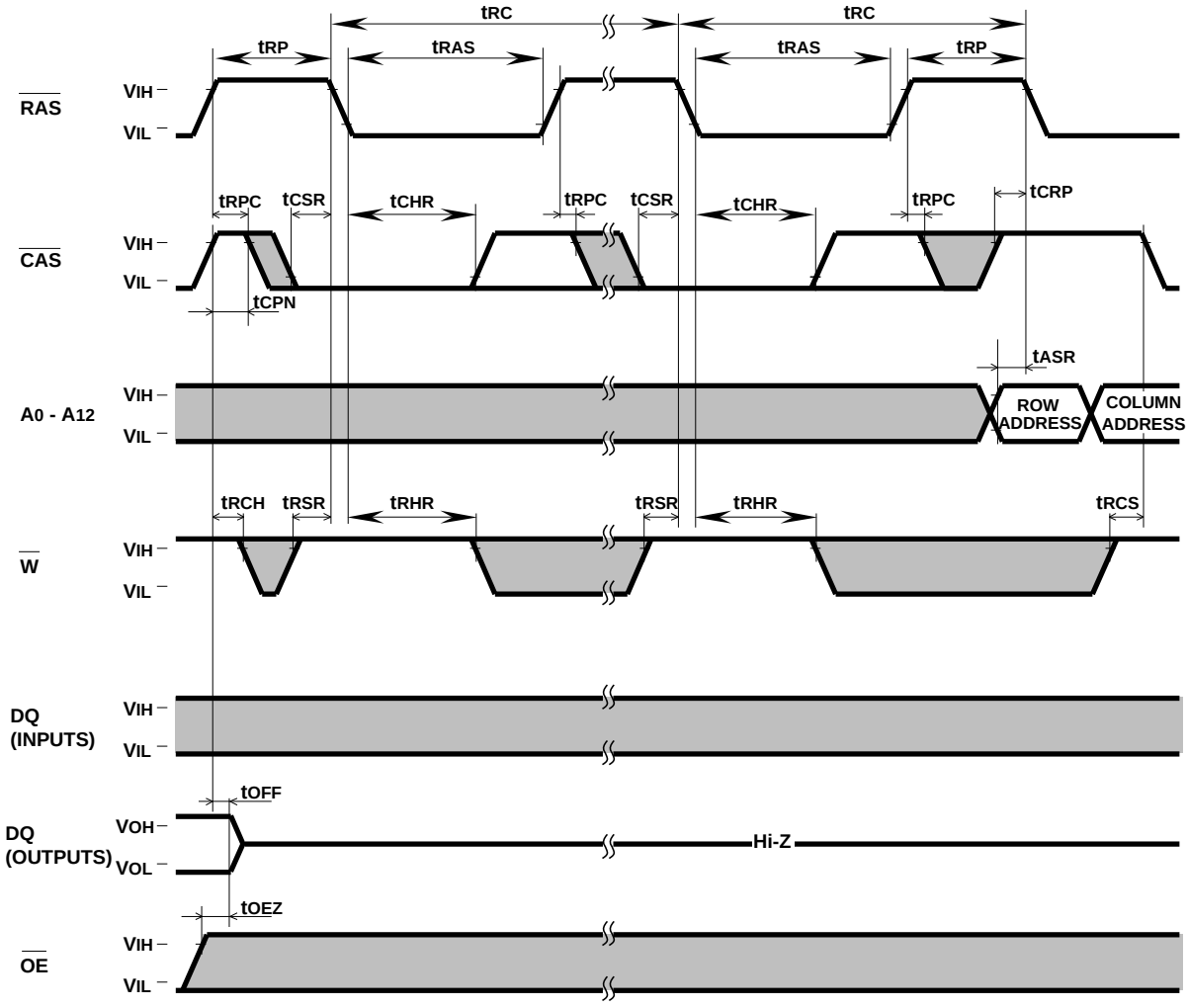
Write Cycle (Delayed write)



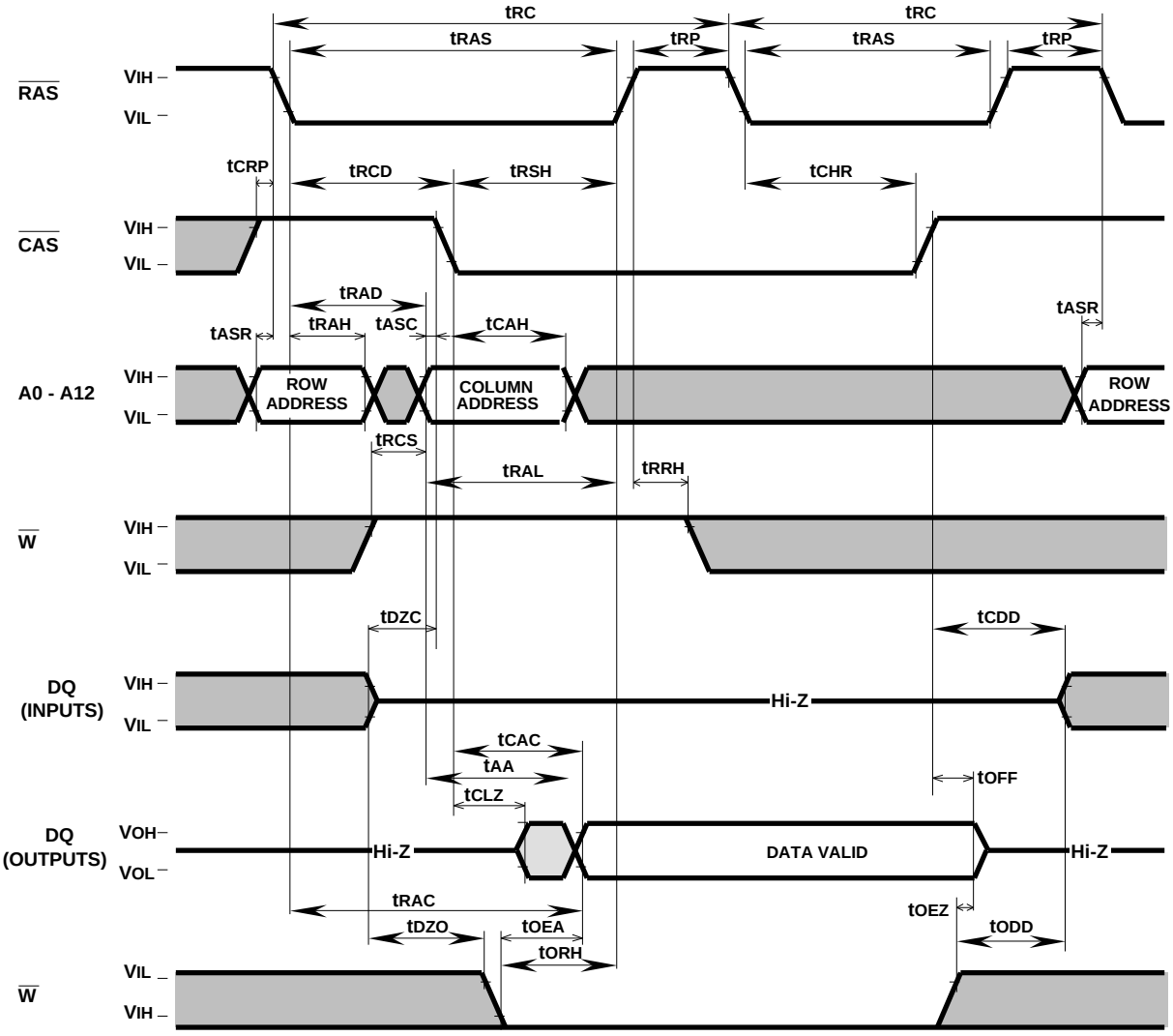
Read-Write, Read-Modify-Write Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

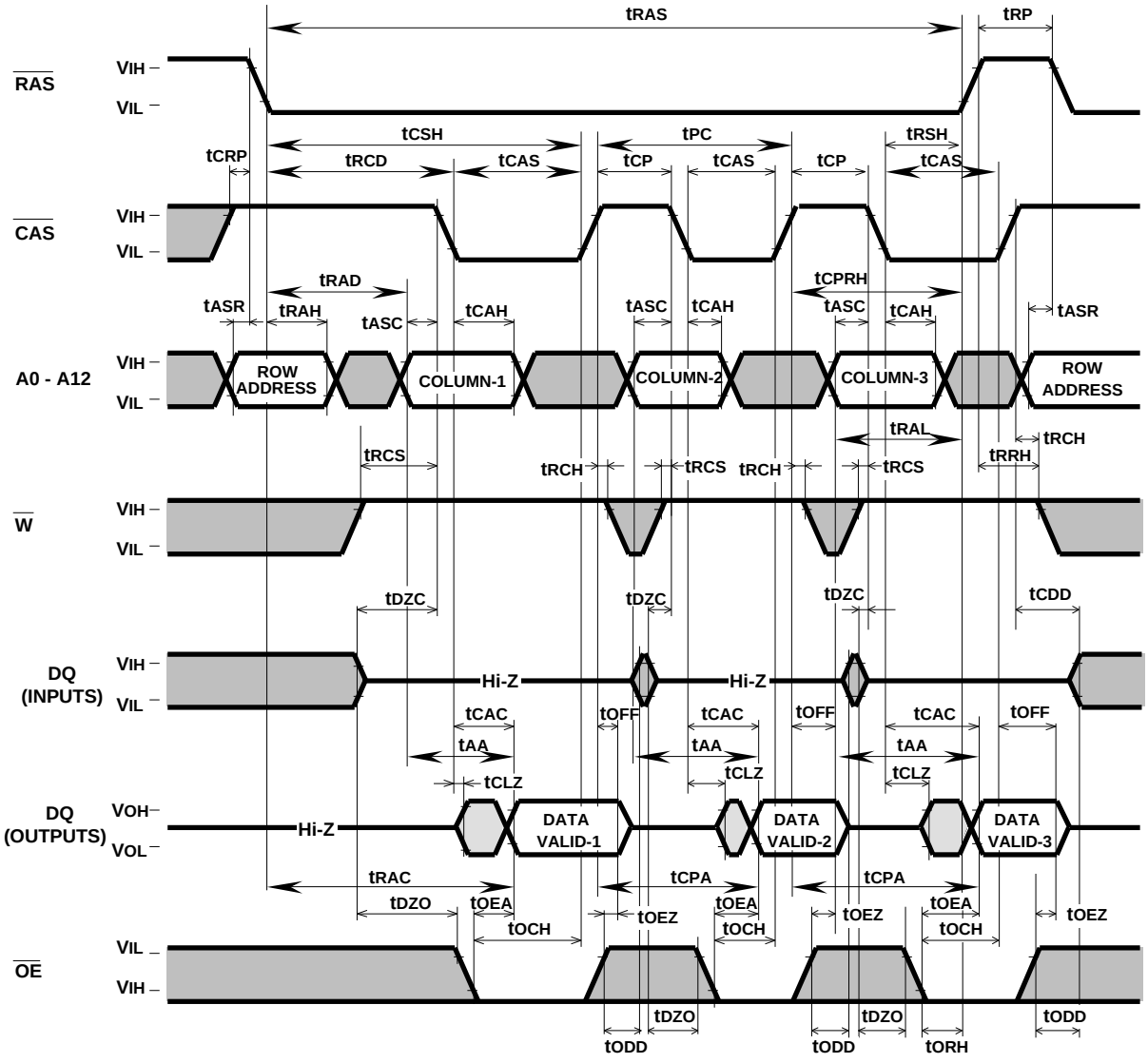


Hidden Refresh Cycle (Read) **(Note 28)**

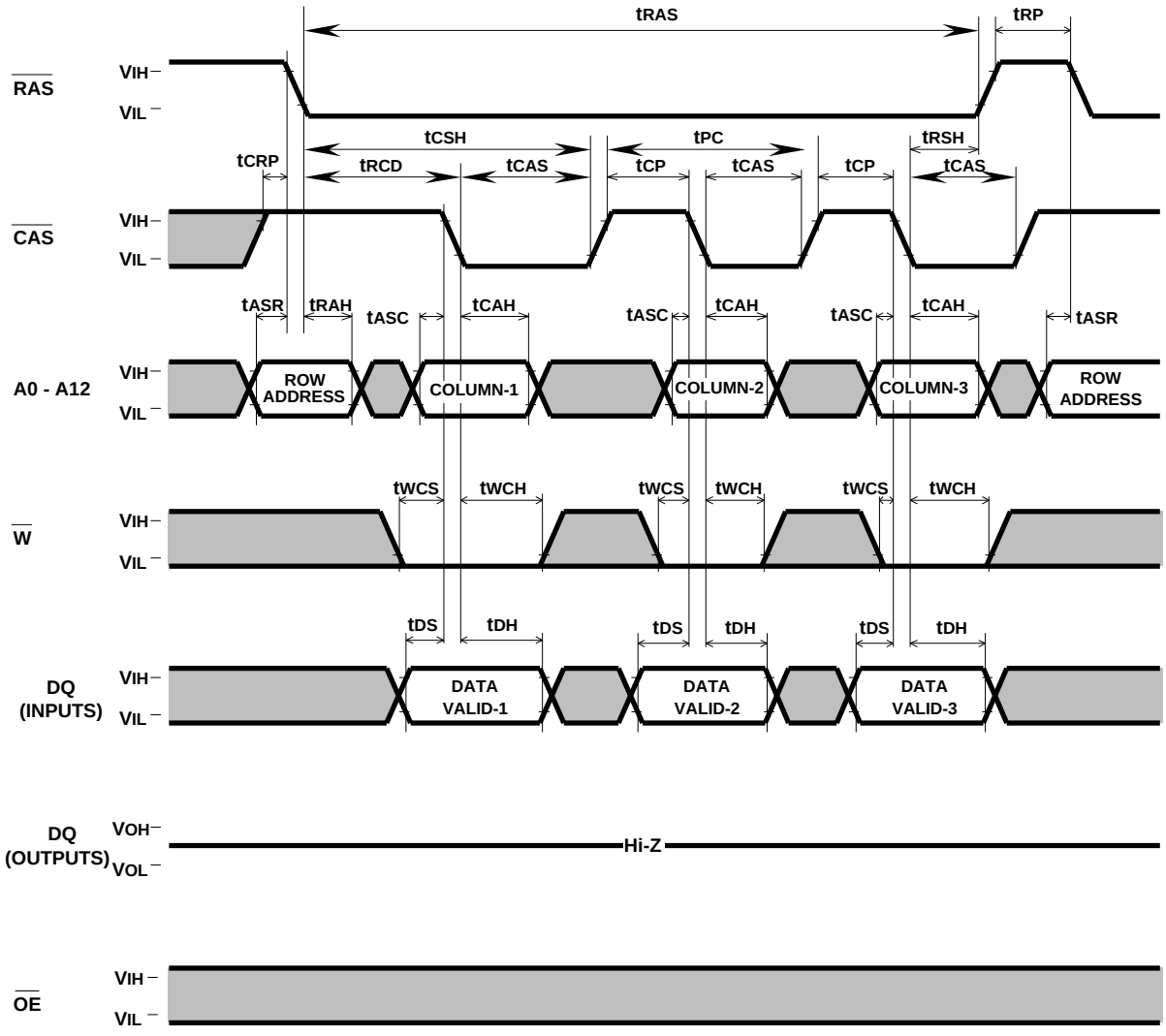


Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

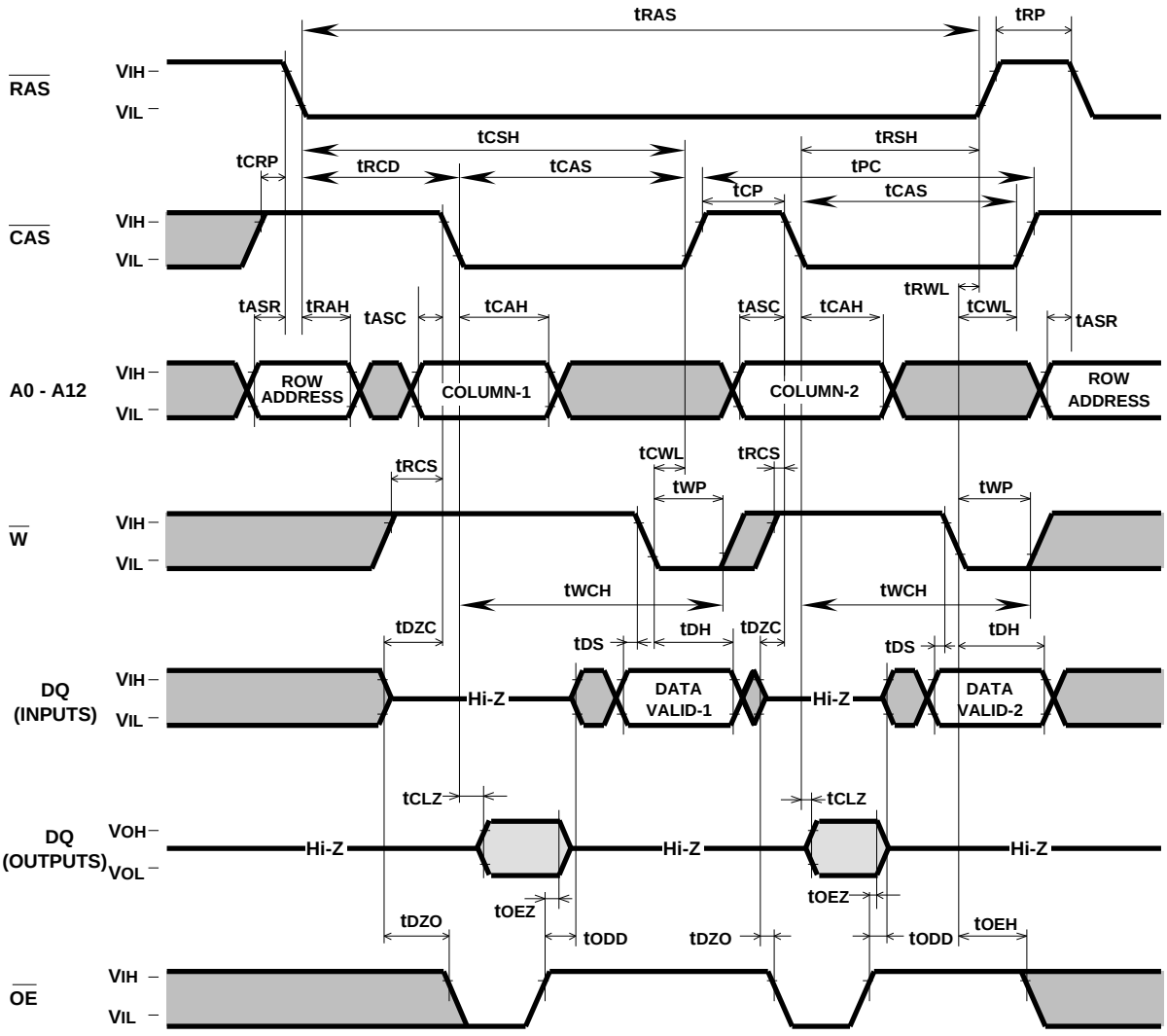
Fast Page Mode Read Cycle



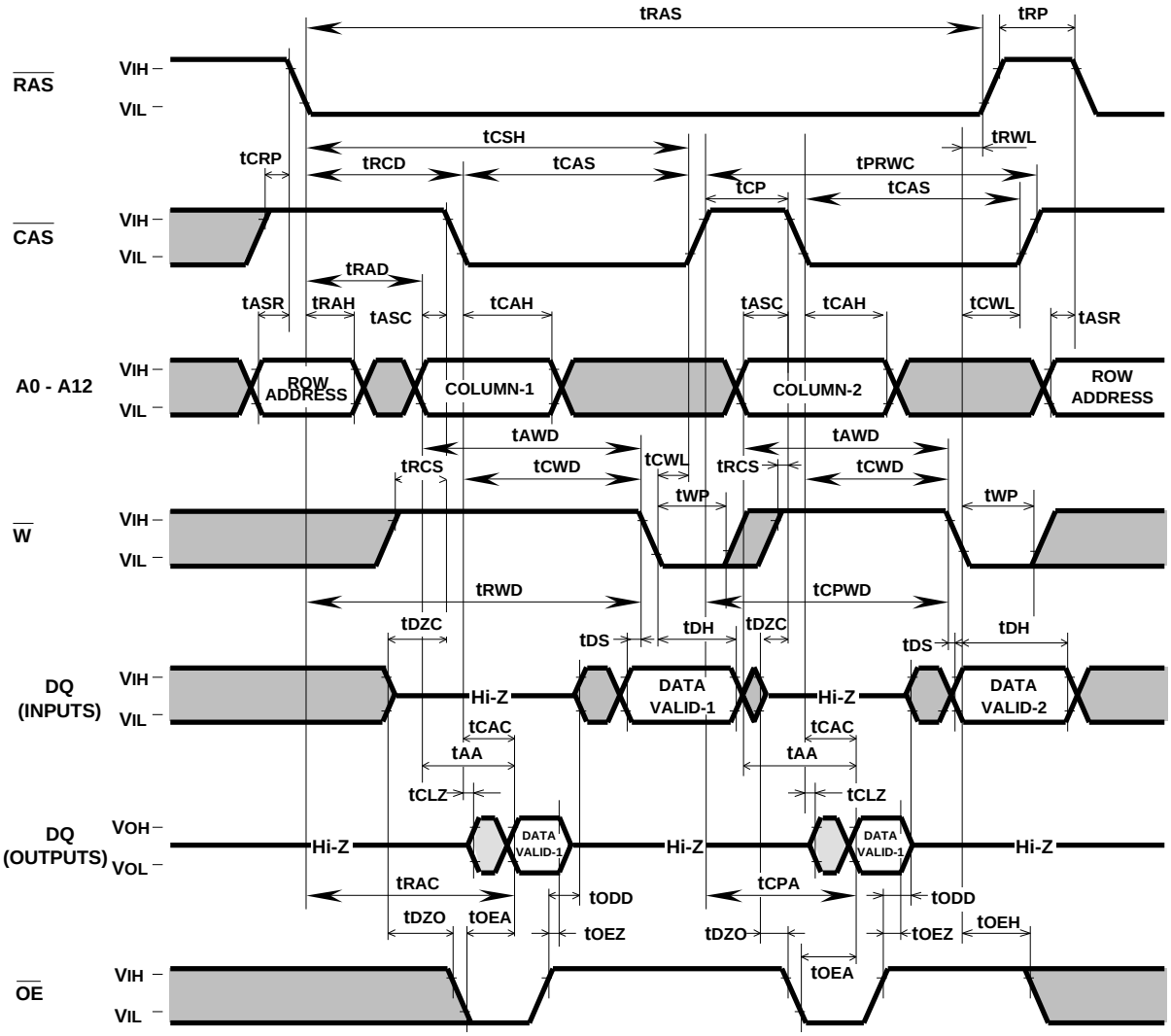
Fast Page Mode Write Cycle (Early Write)



Fast-Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write,Read-Modify-Write Cycle



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