



# M5M5Y416CWG -85HI

## 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

### FUNCTION

The M5M5Y416CWG is organized as 262144-words by 16-bit. These devices operate on a single +1.65~2.3V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs  $\overline{BC1}$ ,  $\overline{BC2}$ ,  $\overline{S1}$ ,  $S2$ ,  $\overline{W}$  and  $\overline{OE}$ . Each mode is summarized in the function table.

A write operation is executed whenever the low level  $\overline{W}$  overlaps with the low level  $\overline{BC1}$  and/or  $\overline{BC2}$  and the low level  $\overline{S1}$  and the high level  $S2$ . The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting  $\overline{W}$  at a high level and  $\overline{OE}$  at a low level while  $\overline{BC1}$  and/or  $\overline{BC2}$  and  $\overline{S1}$  and  $S2$  are in an active state( $\overline{S1}=L, S2=H$ ).

When setting  $\overline{BC1}$  at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting  $\overline{BC2}$  at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

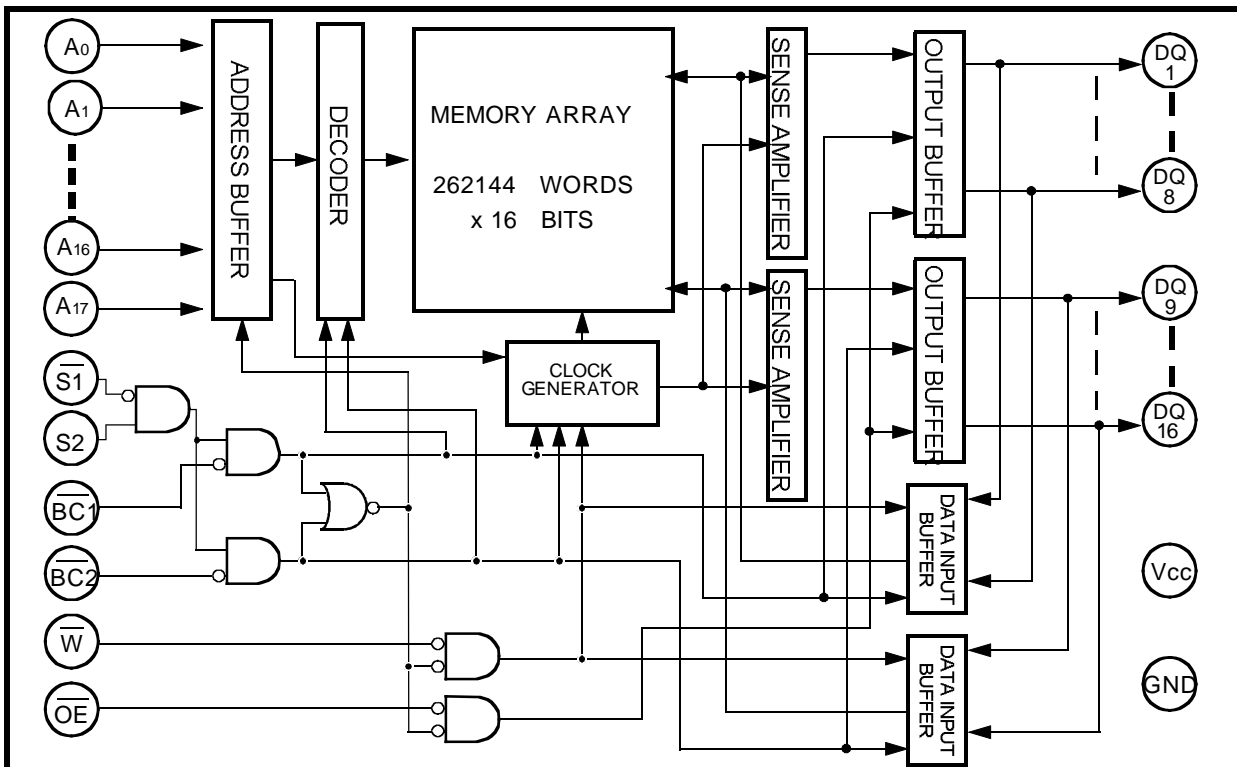
When setting  $\overline{BC1}$  and  $\overline{BC2}$  at a high level or  $\overline{S1}$  at a high level or  $S2$  at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by  $\overline{BC1}$ ,  $\overline{BC2}$  and  $\overline{S1}$ ,  $S2$ .

The power supply current is reduced as low as 0.2 $\mu$ A(25°C, typical), and the memory data can be held at +1.5V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

### FUNCTION TABLE

| $\overline{S1}$ | $S2$ | $\overline{BC1}$ | $\overline{BC2}$ | $\overline{W}$ | $\overline{OE}$ | Mode          | DQ1~8  | DQ9~16 | I <sub>cc</sub> |
|-----------------|------|------------------|------------------|----------------|-----------------|---------------|--------|--------|-----------------|
| H               | L    | X                | X                | X              | X               | Non selection | High-Z | High-Z | Standby         |
| L               | L    | X                | X                | X              | X               | Non selection | High-Z | High-Z | Standby         |
| H               | H    | X                | X                | X              | X               | Non selection | High-Z | High-Z | Standby         |
| X               | X    | H                | H                | X              | X               | Non selection | High-Z | High-Z | Standby         |
| L               | H    | L                | H                | L              | X               | Write         | Din    | High-Z | Active          |
| L               | H    | L                | H                | H              | L               | Read          | Dout   | High-Z | Active          |
| L               | H    | L                | H                | H              | H               | ————          | High-Z | High-Z | Active          |
| L               | H    | H                | L                | L              | X               | Write         | High-Z | Din    | Active          |
| L               | H    | H                | L                | H              | L               | Read          | High-Z | Dout   | Active          |
| L               | H    | H                | L                | H              | H               | ————          | High-Z | High-Z | Active          |
| L               | H    | L                | L                | L              | X               | Write         | Din    | Din    | Active          |
| L               | H    | L                | L                | H              | L               | Read          | Dout   | Dout   | Active          |
| L               | H    | L                | L                | H              | H               | ————          | High-Z | High-Z | Active          |

### BLOCK DIAGRAM



**M5M5Y416CWG -85HI**

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

**ABSOLUTE MAXIMUM RATINGS**

| Symbol           | Parameter             | Conditions           | Ratings                                   | Units |
|------------------|-----------------------|----------------------|---|-------|
| V <sub>CC</sub>  | Supply voltage        | With respect to GND  | -0.5* ~ +2.7                              | V     |
| V <sub>I</sub>   | Input voltage         | With respect to GND  | -0.2* ~ V <sub>CC</sub> + 0.2 (max. 2.7V) |       |
| V <sub>O</sub>   | Output voltage        | With respect to GND  | 0 ~ V <sub>CC</sub>                       |       |
| P <sub>d</sub>   | Power dissipation     | T <sub>a</sub> =25°C | 700                                       | mW    |
| T <sub>a</sub>   | Operating temperature | I-version            | - 40 ~ +85                                | °C    |
| T <sub>stg</sub> | Storage temperature   |                      | - 65 ~ +150                               | °C    |

\* -0.7V in case of AC (Pulse width ≤ 30ns)

**DC ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub>=1.65~ 2.3V, unless otherwise noted)

| Symbol           | Parameter                                  | Conditions   | Limits                |     |                       | Units |    |
|------------------|--|--|-----------------------|-----|-----------------------|-------|----|
|                  |  |  | Min                   | Typ | Max                   |       |    |
| V <sub>IH</sub>  | High-level input voltage                   |  | 0.7 x V <sub>CC</sub> |     | V <sub>CC</sub> +0.2V | V     |    |
| V <sub>IL</sub>  | Low-level input voltage                    |  | -0.2*                 |     | 0.4                   |       |    |
| V <sub>OH</sub>  | High-level output voltage                  | I <sub>OH</sub> = -0.1mA   | 1.3                   |     |                       |       |    |
| V <sub>OL</sub>  | Low-level output voltage                   | I <sub>OL</sub> =0.1mA   |                       |     | 0.2                   | μA    |    |
| I <sub>I</sub>   | Input leakage current                      | V <sub>I</sub> =0 ~ V <sub>CC</sub>  |                       |     | ±1                    |       |    |
| I <sub>O</sub>   | Output leakage current                     | $\overline{BC1}$ and $\overline{BC2}$ =V <sub>IH</sub> or $\overline{S1}$ =V <sub>IH</sub> or S <sub>2</sub> =V <sub>IL</sub> or $\overline{OE}$ =V <sub>IH</sub> , V <sub>I/O</sub> =0 ~ V <sub>CC</sub>  |                       |     | ±1                    | mA    |    |
| I <sub>CC1</sub> | Active supply current<br>(AC, MOS level)   | $\overline{BC1}$ and $\overline{BC2}$ ≤ 0.2V, $\overline{S1}$ ≤ 0.2V, S <sub>2</sub> ≥ V <sub>CC</sub> -0.2V<br>other inputs ≤ 0.2V or ≥ V <sub>CC</sub> -0.2V<br>Output - open (duty 100%)  | f = 10MHz             | -   | 18                    |       | 30 |
|                  |  |  | f = 1MHz              | -   | 1.5                   |       | 3  |
| I <sub>CC2</sub> | Active supply current<br>(AC, TTL level)   | $\overline{BC1}$ and $\overline{BC2}$ =V <sub>IL</sub> , $\overline{S1}$ =V <sub>IL</sub> , S <sub>2</sub> =V <sub>IH</sub><br>other pins =V <sub>IH</sub> or V <sub>IL</sub><br>Output - open (duty 100%)   | f = 10MHz             | -   | 18                    |       | 30 |
|                  |  |  | f = 1MHz              | -   | 1.5                   | 3     |    |
| I <sub>CC3</sub> | Stand by supply current<br>(AC, MOS level) | (1) $\overline{S1}$ ≥ V <sub>CC</sub> - 0.2V,<br>S <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V,<br>other inputs = 0 ~ V <sub>CC</sub><br>(2) S <sub>2</sub> ≤ 0.2V,<br>other inputs = 0 ~ V <sub>CC</sub><br>(3) $\overline{BC1}$ and $\overline{BC2}$ ≥ V <sub>CC</sub> - 0.2V<br>$\overline{S1}$ ≤ 0.2V, S <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V<br>other inputs = 0 ~ V <sub>CC</sub> | ~ +25°C               | -   | 0.2                   | 1     |    |
|                  |  |  | ~ +40°C               | -   | 0.4                   | 2     |    |
|                  |  |  | ~ +70°C               | -   | -                     | 8     |    |
|                  |  |  | ~ +85°C               | -   | -                     | 15    |    |
| I <sub>CC4</sub> | Stand by supply current<br>(AC, TTL level) | $\overline{BC1}$ and $\overline{BC2}$ =V <sub>IH</sub> or $\overline{S1}$ =V <sub>IH</sub> or S <sub>2</sub> =V <sub>IL</sub><br>Other inputs=0 ~ V <sub>CC</sub>  | -                     | -   | 0.5                   | mA    |    |

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

\* -0.7V in case of AC (Pulse width ≤ 30ns)

Note 2: Typical parameter indicates the value for the center of distribution at 2.0V, and not 100% tested.

**CAPACITANCE**(V<sub>CC</sub>=1.65 ~ 2.3V, unless otherwise noted)

| Symbol         | Parameter          | Conditions   | Limits |     |     | Units |
|----------------|--------------------|--|--------|-----|-----|-------|
|                |                    |  | Min    | Typ | Max |       |
| C <sub>I</sub> | Input capacitance  | V <sub>I</sub> =GND, V <sub>I</sub> =25mVrms, f=1MHz |        |     | 10  | pF    |
| C <sub>O</sub> | Output capacitance | V <sub>O</sub> =GND, V <sub>O</sub> =25mVrms, f=1MHz |        |     | 10  |       |



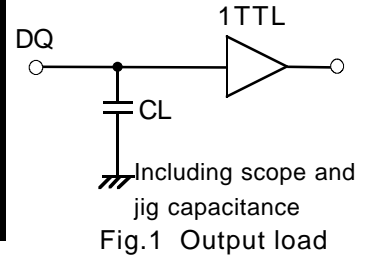
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4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub>=1.65 ~ 2.3V, unless otherwise noted)

### (1) TEST CONDITIONS

|                               |   |
|-------------------------------|---|
| Supply voltage                | 1.65~2.3V   |
| Input pulse                   | V <sub>IH</sub> =0.7 x V <sub>CC</sub> +0.2V, V <sub>IL</sub> =0.2V   |
| Input rise time and fall time | 5ns   |
| Reference level               | V <sub>OH</sub> =V <sub>OL</sub> =0.9V <small>Transition is measured ±200mV from steady state voltage.(for ten, tdis)</small> |
| Output loads                  | Fig.1, CL=30pF<br>CL=5pF (for ten, tdis)  |



### (2) READ CYCLE

| Symbol                | Parameter                                       | Limits |     | Units |
|-----------------------|---|--------|-----|-------|
|                       |   | 85HI   |     |       |
|                       |   | Min    | Max |       |
| t <sub>CR</sub>       | Read cycle time                                 | 85     |     | ns    |
| t <sub>a(A)</sub>     | Address access time                             |        | 85  | ns    |
| t <sub>a(S1)</sub>    | Chip select 1 access time                       |        | 85  | ns    |
| t <sub>a(S2)</sub>    | Chip select 2 access time                       |        | 85  | ns    |
| t <sub>a(BC1)</sub>   | Byte control 1 access time                      |        | 85  | ns    |
| t <sub>a(BC2)</sub>   | Byte control 2 access time                      |        | 85  | ns    |
| t <sub>a(OE)</sub>    | Output enable access time                       |        | 45  | ns    |
| t <sub>dis(S1)</sub>  | Output disable time after $\overline{S1}$ high  |        | 30  | ns    |
| t <sub>dis(S2)</sub>  | Output disable time after S2 low                |        | 30  | ns    |
| t <sub>dis(BC1)</sub> | Output disable time after $\overline{BC1}$ high |        | 30  | ns    |
| t <sub>dis(BC2)</sub> | Output disable time after $\overline{BC2}$ high |        | 30  | ns    |
| t <sub>dis(OE)</sub>  | Output disable time after $\overline{OE}$ high  |        | 30  | ns    |
| t <sub>en(S1)</sub>   | Output enable time after $\overline{S1}$ low    | 10     |     | ns    |
| t <sub>en(S2)</sub>   | Output enable time after S2 high                | 10     |     | ns    |
| t <sub>dis(BC1)</sub> | Output enable time after $\overline{BC1}$ low   | 10     |     | ns    |
| t <sub>dis(BC2)</sub> | Output enable time after $\overline{BC2}$ low   | 10     |     | ns    |
| t <sub>en(OE)</sub>   | Output enable time after $\overline{OE}$ low    | 5      |     | ns    |
| t <sub>v(A)</sub>     | Data valid time after address                   | 10     |     | ns    |

### (3) WRITE CYCLE

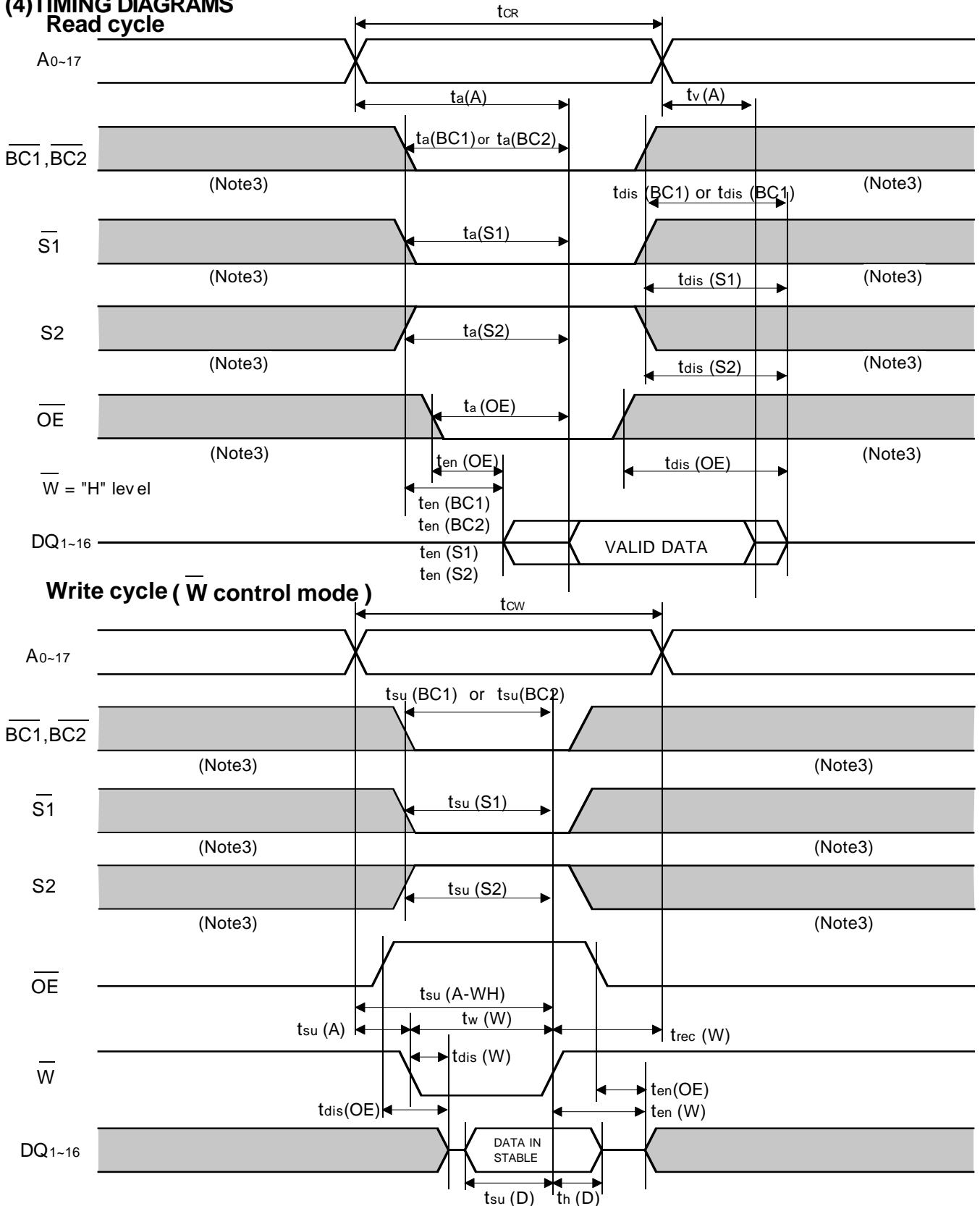
| Symbol                | Parameter   | Limits |     | Units |
|-----------------------|---|--------|-----|-------|
|                       |   | 85HI   |     |       |
|                       |   | Min    | Max |       |
| t <sub>cw</sub>       | Write cycle time                                  | 85     |     | ns    |
| t <sub>w(W)</sub>     | Write pulse width                                 | 60     |     | ns    |
| t <sub>su(A)</sub>    | Address setup time                                | 0      |     | ns    |
| t <sub>su(A-WH)</sub> | Address setup time with respect to $\overline{W}$ | 70     |     | ns    |
| t <sub>su(BC1)</sub>  | Byte control 1 setup time                         | 70     |     | ns    |
| t <sub>su(BC2)</sub>  | Byte control 2 setup time                         | 70     |     | ns    |
| t <sub>su(S1)</sub>   | Chip select 1 setup time                          | 70     |     | ns    |
| t <sub>su(S2)</sub>   | Chip select 2 setup time                          | 70     |     | ns    |
| t <sub>su(D)</sub>    | Data setup time                                   | 35     |     | ns    |
| t <sub>h(D)</sub>     | Data hold time                                    | 0      |     | ns    |
| t <sub>rec(W)</sub>   | Write recovery time                               | 0      |     | ns    |
| t <sub>dis(W)</sub>   | Output disable time from $\overline{W}$ low       |        | 30  | ns    |
| t <sub>dis(OE)</sub>  | Output disable time from $\overline{OE}$ high     |        | 30  | ns    |
| t <sub>en(W)</sub>    | Output enable time from $\overline{W}$ high       | 5      |     | ns    |
| t <sub>en(OE)</sub>   | Output enable time from $\overline{OE}$ low       | 5      |     | ns    |



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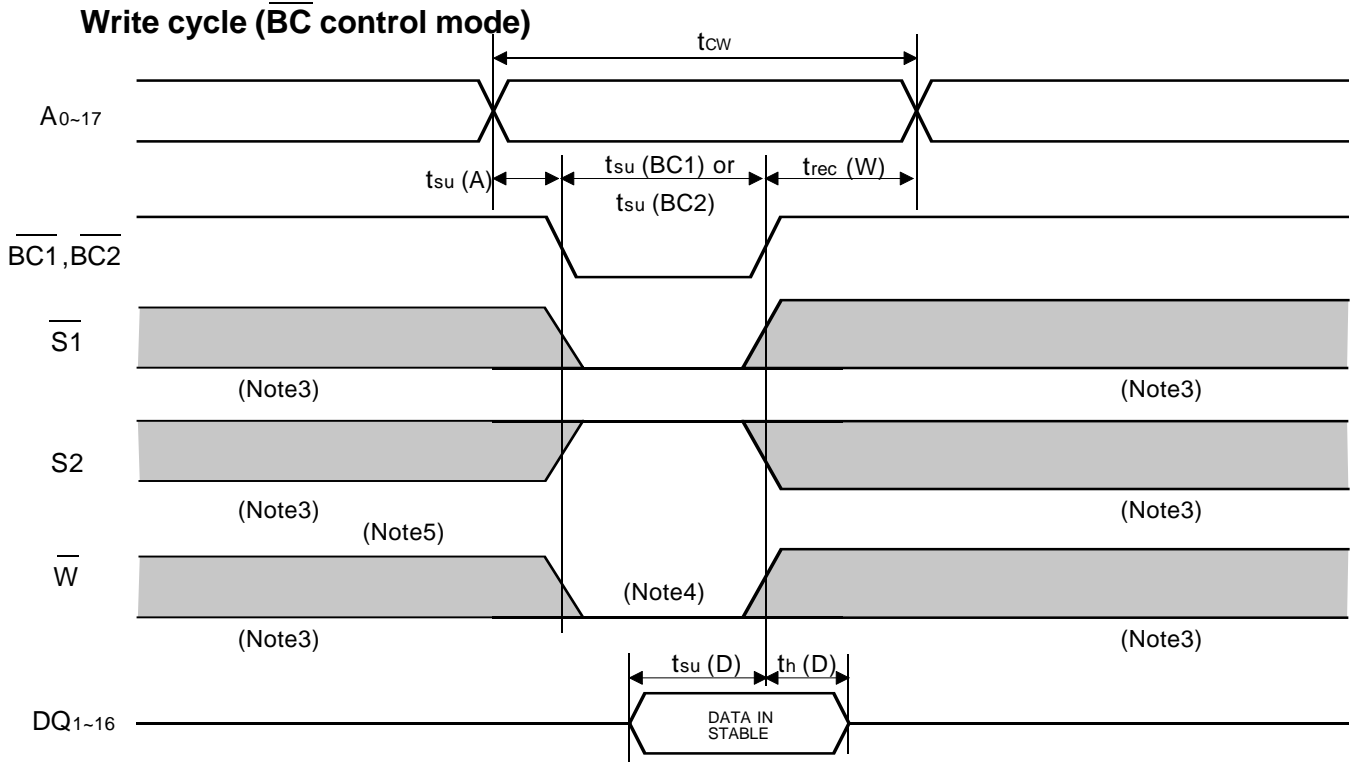
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## (4)TIMING DIAGRAMS



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Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during  $\overline{S1}$  low, S2 high overlaps  $\overline{BC1}$  and/or  $\overline{BC2}$  low and  $\overline{W}$  low.

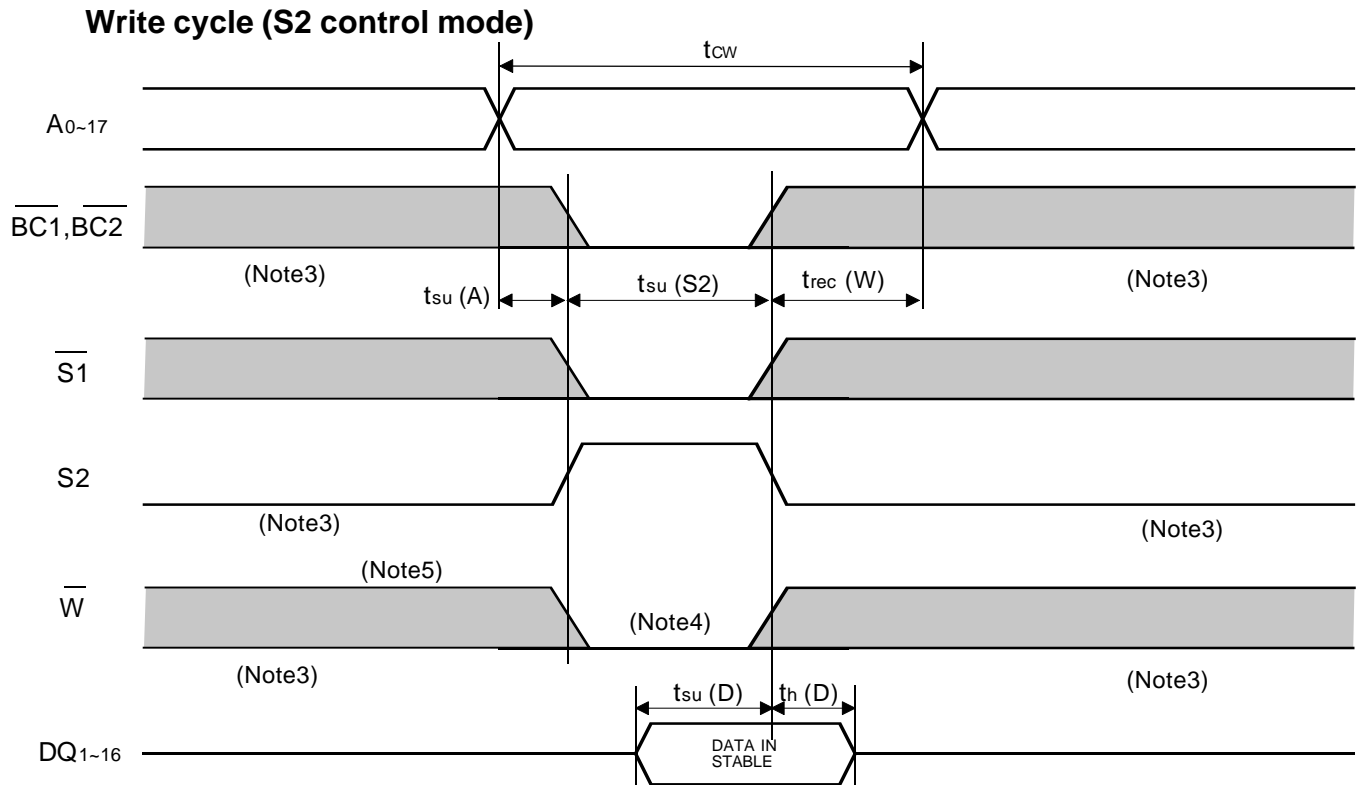
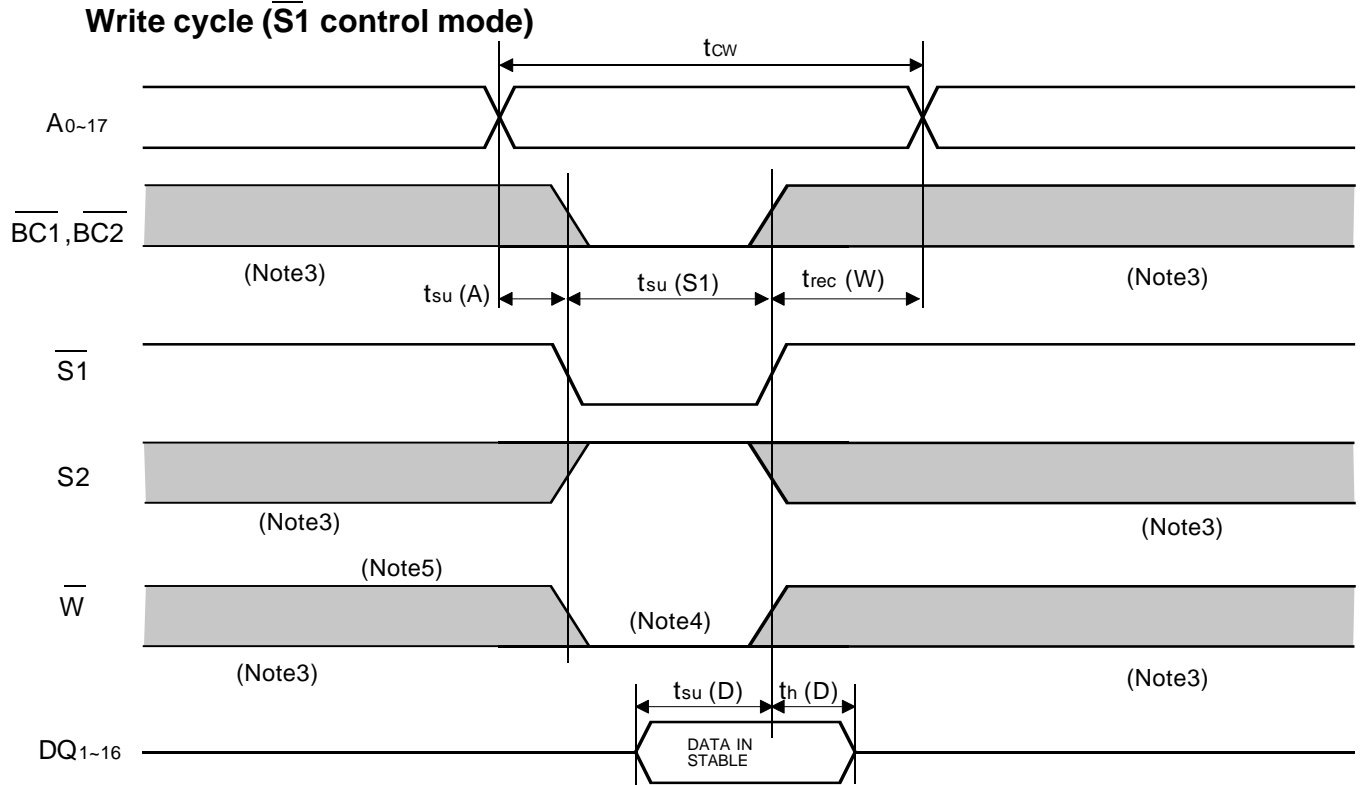
Note 5: When the falling edge of  $\overline{W}$  is simultaneously or prior to the falling edge of  $\overline{BC1}$  and/or  $\overline{BC2}$  or the falling edge of  $\overline{S1}$  or rising edge of S2, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.



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## POWER DOWN CHARACTERISTICS

### (1) ELECTRICAL CHARACTERISTICS

| Symbol               | Parameter  | Test conditions  | Limits              |              |     | Units |    |
|----------------------|--|--|---------------------|--------------|-----|-------|----|
|                      |  |  | Min                 | Typ          | Max |       |    |
| V <sub>CC</sub> (PD) | Power down supply voltage                              |  | 1.5                 |              |     | V     |    |
| V <sub>I</sub> (BC)  | Byte control input $\overline{BC1}$ & $\overline{BC2}$ | $1.65V \leq V_{CC}(PD)$  | $0.7 \times V_{CC}$ |              |     | V     |    |
|                      |  | $1.5V \leq V_{CC}(PD) \leq 1.65V$  |                     | $V_{CC}(PD)$ |     |       |    |
| V <sub>I</sub> (S1)  | Chip select input $\overline{S1}$                      | $1.65V \leq V_{CC}(PD)$  | $0.7 \times V_{CC}$ |              |     | V     |    |
|                      |  | $1.5V \leq V_{CC}(PD) \leq 1.65V$  |                     | $V_{CC}(PD)$ |     |       |    |
| V <sub>I</sub> (S2)  | Chip select input S2                                   |  |                     |              | 0.2 | V     |    |
| I <sub>CC</sub> (PD) | Power down supply current                              | $V_{CC}=1.5V$<br>(1) $\overline{S1} \geq V_{CC} - 0.2V$ ,<br>other inputs = 0 - V <sub>CC</sub><br>(2) $S2 \leq 0.2V$ ,<br>other inputs = 0 - V <sub>CC</sub><br>(3) $\overline{BC1}$ and $\overline{BC2} \geq V_{CC} - 0.2V$<br>$\overline{S1} \leq 0.2V$ , $S2 \geq V_{CC} - 0.2V$<br>other inputs = 0 - V <sub>CC</sub> | ~ +25°C             | -            | 0.1 | 0.7   | μA |
|                      |  |  | ~ +40°C             | -            | 0.2 | 1.5   |    |
|                      |  |  | ~ +70°C             | -            | -   | 5     |    |
|                      |  |  | ~ +85°C             | -            | -   | 10    |    |

Note 2: Typical parameter of I<sub>CC</sub>(PD) indicates the value for the center of distribution at 1.5V, and not 100% tested.

### (2) TIMING REQUIREMENTS

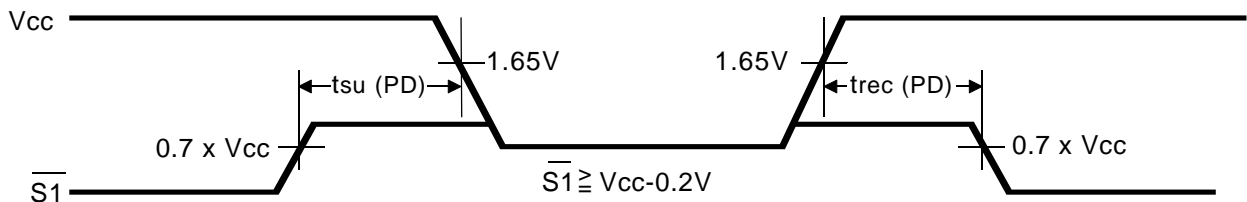
| Symbol                | Parameter                | Test conditions | Limits |     |     | Units |
|-----------------------|--------------------------|-----------------|--------|-----|-----|-------|
|                       |                          |                 | Min    | Typ | Max |       |
| t <sub>su</sub> (PD)  | Power down set up time   |                 | 0      |     |     | ns    |
| t <sub>rec</sub> (PD) | Power down recovery time |                 | 5      |     |     | ms    |

### (3) TIMING DIAGRAM

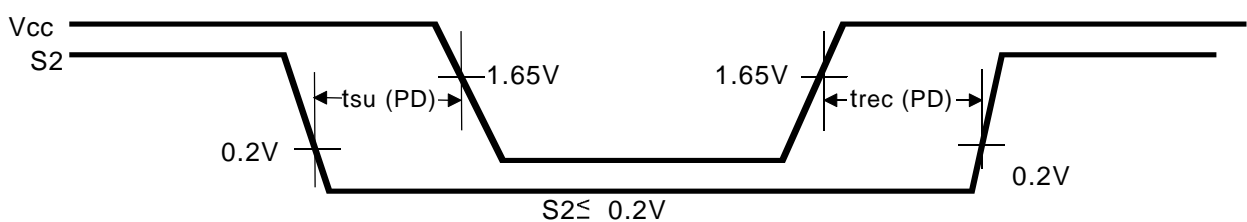
#### BC control mode



#### S1 control mode



#### S2 control mode





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