

MITSUBISHI LSIs
M5M5V108CFP,VP,RV,KV,KR -70H, -10H,
-70X, -10X
1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M5V108CFP,VP,RV,KV,KR are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance quadruple-polysilicon and double metal CMOS technology. The use of thin film transistor (TFT) load cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M5V108CVP,RV,KV,KR are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD). Two types of devices are available. M5M5V108CVP,KV(normal lead bend type package), M5M5V108CRV,KR(reverse lead bend type package).Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

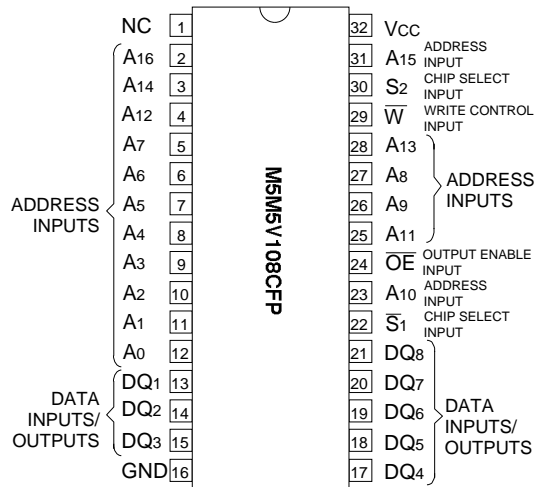
| Type name | Access time (max) | VCC | Power supply current | |
|-----------------------------|-------------------|----------|----------------------|----------------|
| | | | Active (1MHz) (max) | stand-by (max) |
| M5M5V108CFP,VP,RV,KV,KR-70H | 70ns | 2.7~3.6V | 5mA | 12µA |
| M5M5V108CFP,VP,RV,KV,KR-10H | 100ns | | | |
| M5M5V108CFP,VP,RV,KV,KR-70X | 70ns | | | 4.8µA |
| M5M5V108CFP,VP,RV,KV,KR-10X | 100ns | | | |

- Low stand-by current 0.1µA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by S₁,S₂
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- OE prevents data contention in the I/O bus
- Common data I/O
- Package
 - M5M5V108CFP 32pin 525mil SOP
 - M5M5V108CVP,RV 32pin 8 X 20 mm² TSOP
 - M5M5V108CKV,KR 32pin 8 X 13.4 mm² TSOP

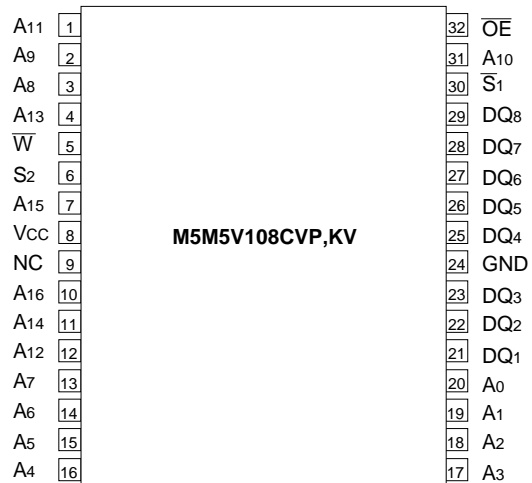
APPLICATION

Small capacity memory units

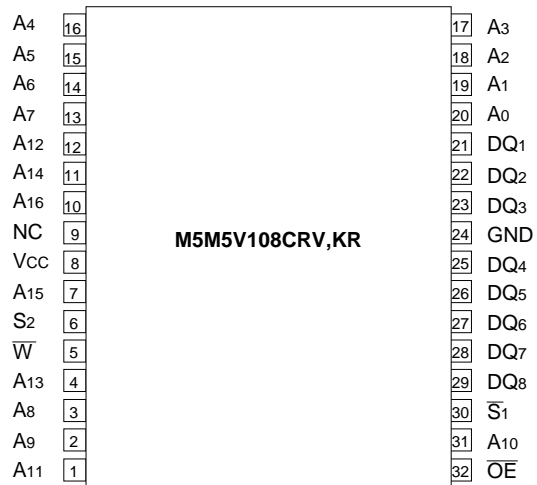
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A



Outline 32P3H-E(VP), 32P3K-B(KV)



Outline 32P3H-F(RV), 32P3K-C(KR)

NC : NO CONNECTION

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FUNCTION

The operation mode of the M5M5V108C series are determined by a combination of the device control inputs \bar{S}_1, S_2, \bar{W} and \bar{OE} . Each mode is summarized in the function table.

A write cycle is executed whenever the low level \bar{W} overlaps with the low level \bar{S}_1 and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \bar{W}, \bar{S}_1 or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input \bar{OE} directly controls the output stage. Setting the \bar{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

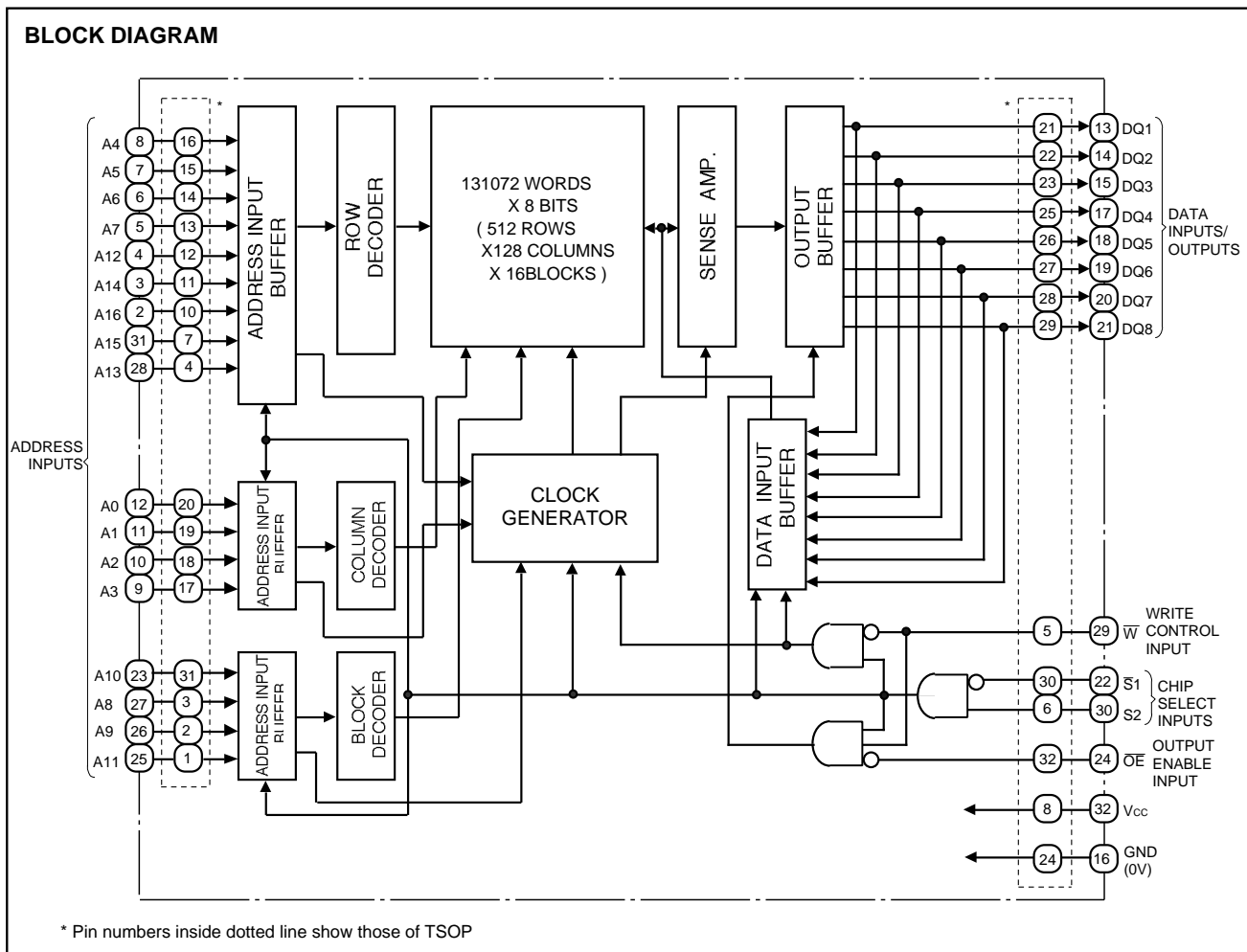
A read cycle is executed by setting \bar{W} at a high level and \bar{OE} at a low level while \bar{S}_1 and S_2 are in an active state ($\bar{S}_1=L, S_2=H$).

When setting \bar{S}_1 at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \bar{S}_1 and S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

| \bar{S}_1 | S_2 | \bar{W} | \bar{OE} | Mode | DQ | I _{cc} |
|-------------|-------|-----------|------------|---------------|----------------|-----------------|
| X | L | X | X | Non selection | High-impedance | Stand-by |
| H | X | X | X | Non selection | High-impedance | Stand-by |
| L | H | L | X | Write | Din | Active |
| L | H | H | L | Read | Dout | Active |
| L | H | H | H | | High-impedance | Active |

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP

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ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|-----------------------|----------------------|---|------|
| V _{CC} | Supply voltage | With respect to GND | - 0.3*~4.6 | V |
| V _I | Input voltage | | - 0.3*~V _{CC} + 0.3 (Max 4.6) | V |
| V _O | Output voltage | | 0~V _{CC} | V |
| P _d | Power dissipation | T _a =25°C | 700 | mW |
| T _{opr} | Operating temperature | | 0~70 | °C |
| T _{stg} | Storage temperature | | - 65~150 | °C |

* -3.0V in case of AC (Pulse width 30ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=2.7~3.6V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|------------------|-----------------------------|---|-----------------------|-------|-----------------------|------|
| | | | Min | Typ | Max | |
| V _{IH} | High-level input voltage | | 2.0 | | V _{CC} + 0.3 | V |
| V _{IL} | Low-level input voltage | | -0.3* | | 0.6 | V |
| V _{OH1} | High-level output voltage 1 | I _{OH} = - 0.5mA | 2.4 | | | V |
| V _{OH2} | High-level output voltage 2 | I _{OH} = - 0.05mA | V _{CC} - 0.5 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 2mA | | | 0.4 | V |
| I _I | Input current | V _I =0~V _{CC} | | | ±1 | µA |
| I _O | Output current in off-state | $\bar{S}_1=V_{IH}$ or $S_2=V_{IL}$ or $\bar{OE}=V_{IH}$ V _{I/O} =0~V _{CC} | | | ±1 | µA |
| I _{CC1} | Active supply current | $\bar{S}_1=V_{IL}, S_2=V_{IH}$, other inputs=V _{IH} or V _{IL} Output-open(duty 100%) | 70ns | | 35 | mA |
| | | | 100ns | | 30 | |
| I _{CC2} | Active supply current | | 1MHz | | 5 | |
| I _{CC3} | Stand-by current | 1) S ₂ 0.2V other inputs=0~V _{CC} 2) \bar{S}_1 V _{CC} -0.2V, S ₂ V _{CC} -0.2V other inputs=0~V _{CC} | -H | ~25°C | 1.2 | µA |
| | | | | ~40°C | 3.6 | |
| | | | | ~70°C | 12 | |
| | | | -X | ~25°C | 0.6 | |
| | | | | ~40°C | 1.8 | |
| | | | | ~70°C | 4.8 | |
| I _{CC4} | Stand-by current | $\bar{S}_1=V_{IH}$ or $S_2=V_{IL}$, other inputs=0~V _{CC} | | | 0.33 | mA |

* -3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (T_a=0~70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------------|--------------------|--|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| C _I | Input capacitance | V _I =GND, V _I =25mVrms, f=1MHz | | | 6 | pF |
| C _O | Output capacitance | V _O =GND, V _O =25mVrms, f=1MHz | | | 10 | pF |

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{CC} = 3V, T_a = 25°C

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AC ELECTRICAL CHARACTERISTICS ($T_a=0\sim 70^{\circ}\text{C}$, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

- V_{CC} 2.7~3.6V
- Input pulse level V_{IH}=2.2V, V_{IL}=0.4V
- Input rise and fall time 5ns
- Reference level V_{OH}=V_{OL}=1.5V
- Output loads Fig.1, C_L=30pF
 C_L=5pF (for t_{en},t_{dis})
- Transition is measured \pm 500mV from steady state voltage. (for t_{en},t_{dis})

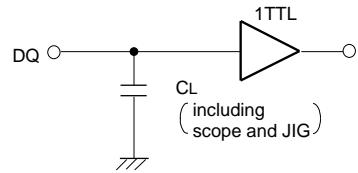


Fig.1 Output load

(2) READ CYCLE

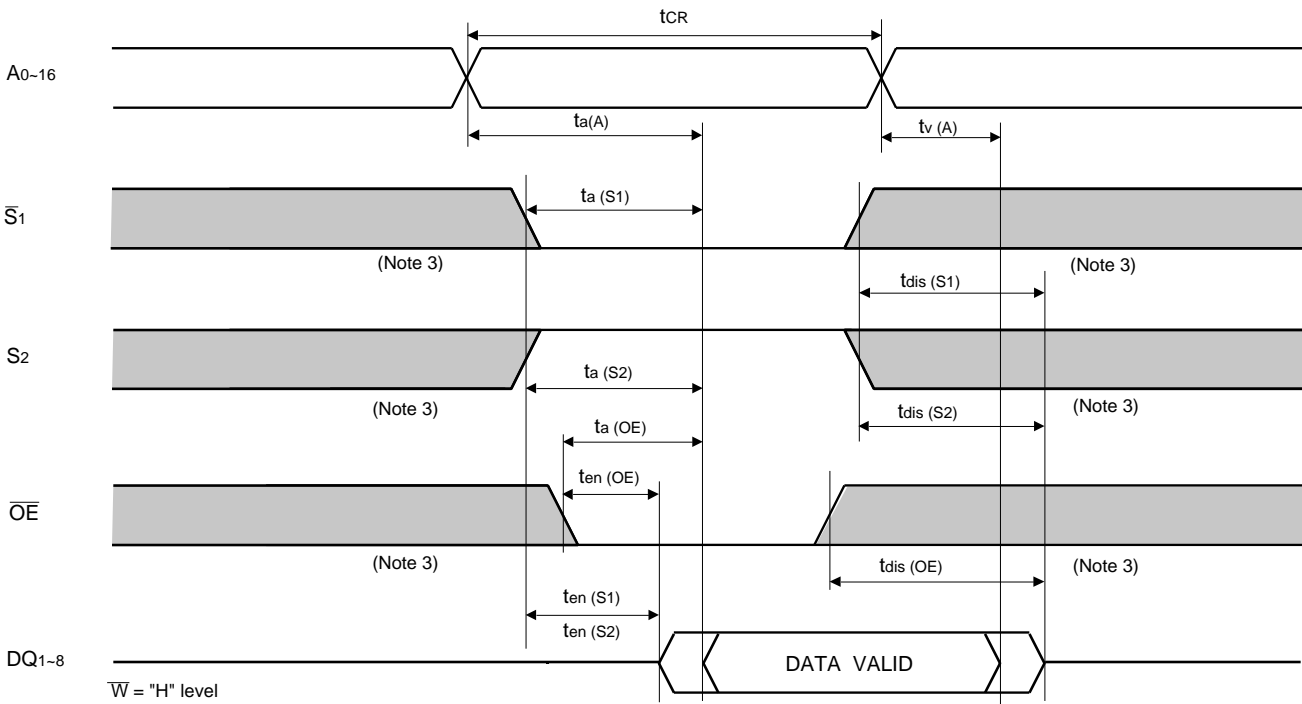
| Symbol | Parameter | Limits | | | | Unit |
|----------------------|--|-----------|-----|-----------|-----|------|
| | | -70H,-70X | | -10H,-10X | | |
| | | Min | Max | Min | Max | |
| t _{CR} | Read cycle time | 70 | | 100 | | ns |
| t _{a(A)} | Address access time | | 70 | | 100 | ns |
| t _{a(S1)} | Chip select 1 access time | | 70 | | 100 | ns |
| t _{a(S2)} | Chip select 2 access time | | 70 | | 100 | ns |
| t _{a(OE)} | Output enable access time | | 35 | | 50 | ns |
| t _{dis(S1)} | Output disable time after \bar{S}_1 high | | 25 | | 35 | ns |
| t _{dis(S2)} | Output disable time after \bar{S}_2 low | | 25 | | 35 | ns |
| t _{dis(OE)} | Output disable time after \bar{OE} high | | 25 | | 35 | ns |
| t _{en(S1)} | Output enable time after \bar{S}_1 low | 10 | | 10 | | ns |
| t _{en(S2)} | Output enable time after S_2 high | 10 | | 10 | | ns |
| t _{en(OE)} | Output enable time after \bar{OE} low | 5 | | 5 | | ns |
| t _{V(A)} | Data valid time after address | 10 | | 10 | | ns |

(3) WRITE CYCLE

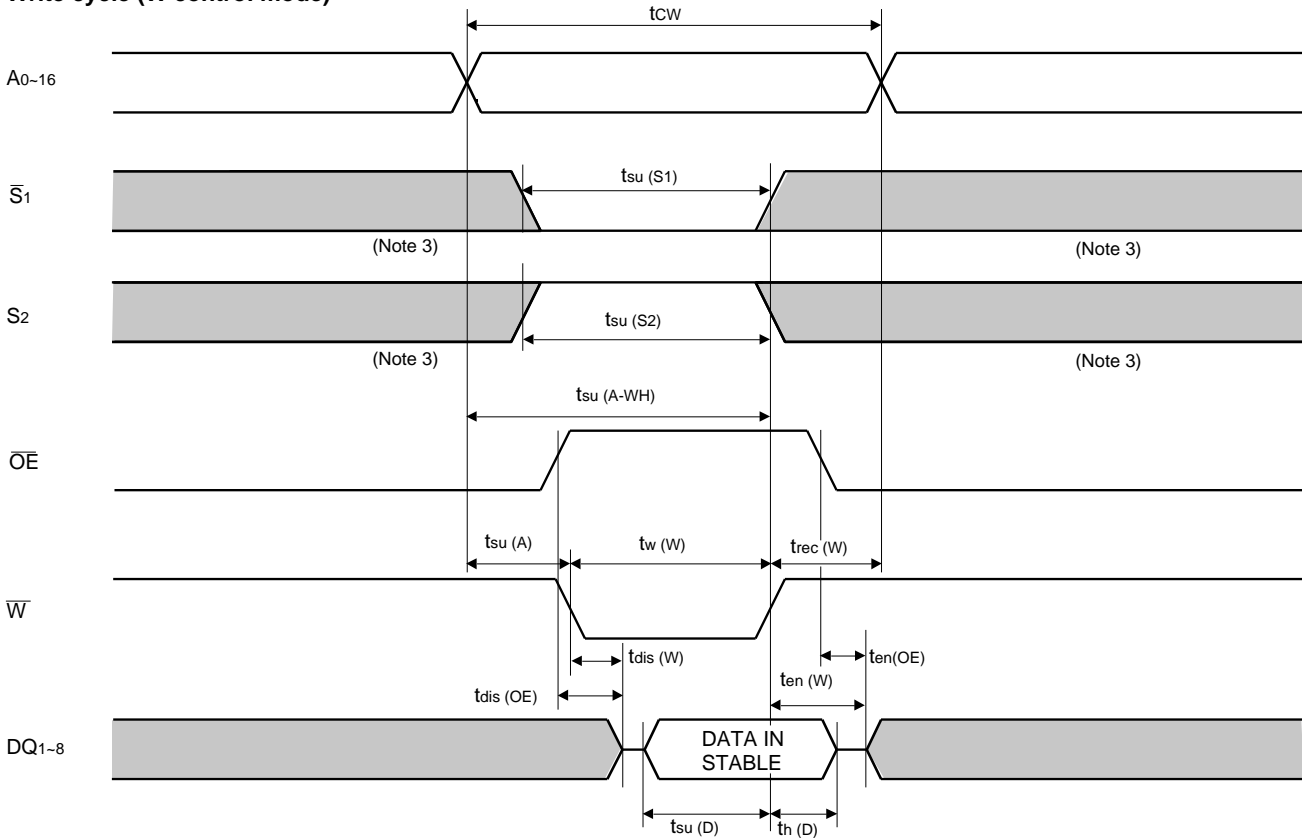
| Symbol | Parameter | Limits | | | | Unit |
|-----------------------|--|-----------|-----|-----------|-----|------|
| | | -70H,-70X | | -10H,-10X | | |
| | | Min | Max | Min | Max | |
| t _{cw} | Write cycle time | 70 | | 100 | | ns |
| t _{w(W)} | Write pulse width | 55 | | 75 | | ns |
| t _{su(A)} | Address setup time | 0 | | 0 | | ns |
| t _{su(A-WH)} | Address setup time with respect to \bar{W} | 65 | | 85 | | ns |
| t _{su(S1)} | Chip select 1 setup time | 65 | | 85 | | ns |
| t _{su(S2)} | Chip select 2 setup time | 65 | | 85 | | ns |
| t _{su(D)} | Data setup time | 30 | | 40 | | ns |
| t _{h(D)} | Data hold time | 0 | | 0 | | ns |
| t _{rec(W)} | Write recovery time | 0 | | 0 | | ns |
| t _{dis(W)} | Output disable time from \bar{W} low | | 25 | | 35 | ns |
| t _{dis(OE)} | Output disable time from \bar{OE} high | | 25 | | 35 | ns |
| t _{en(W)} | Output enable time from \bar{W} high | 5 | | 5 | | ns |
| t _{en(OE)} | Output enable time from \bar{OE} low | 5 | | 5 | | ns |

(4) TIMING DIAGRAMS

Read cycle

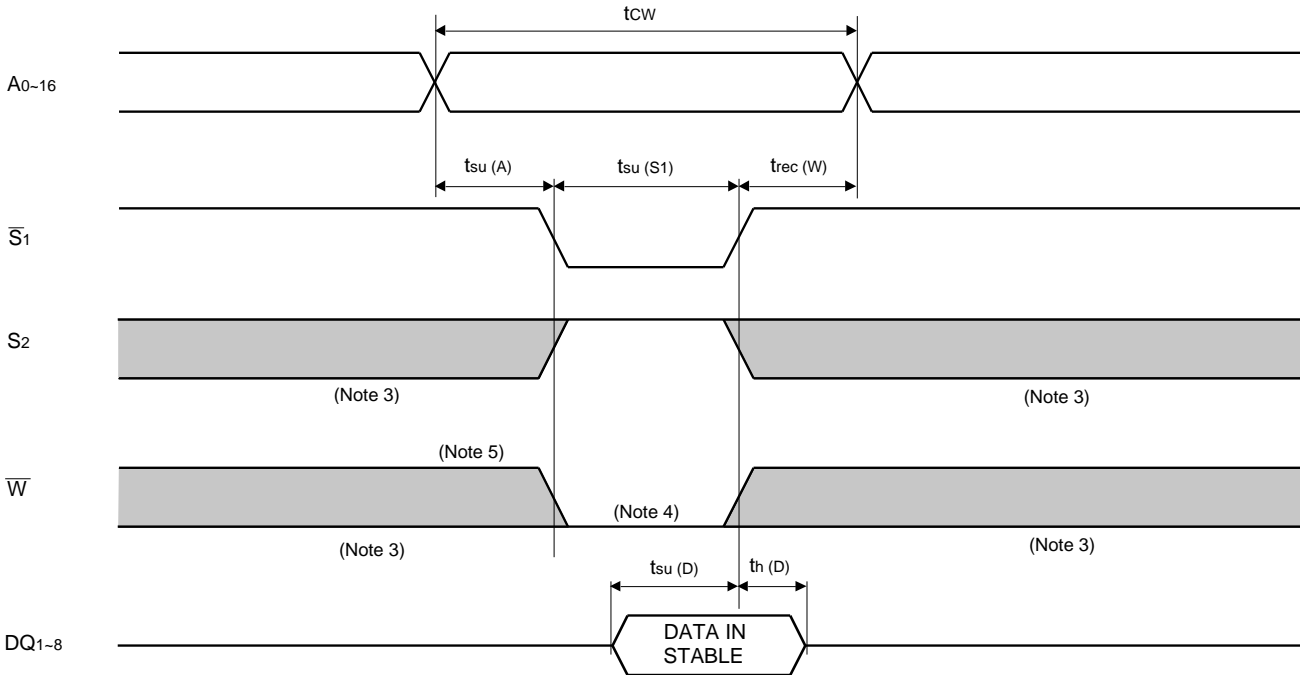


Write cycle (\bar{W} control mode)

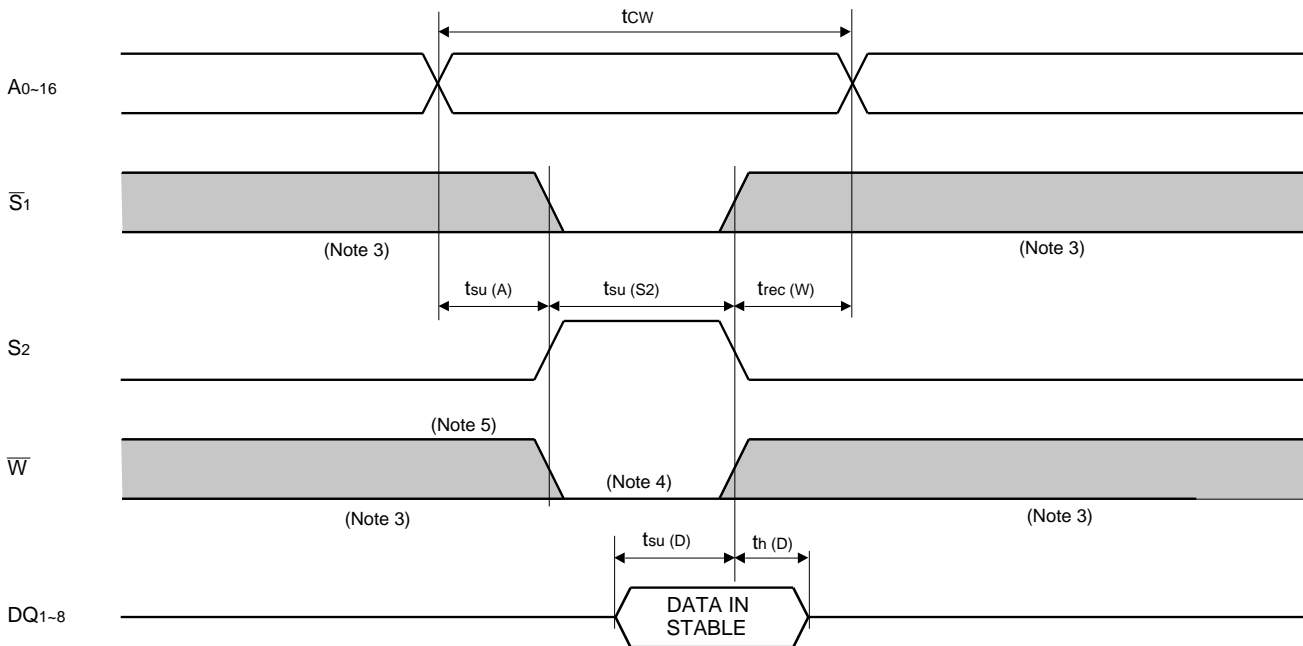


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Write cycle (\overline{S}_1 control mode)



Write cycle (S2 control mode)



- Note 3: Hatching indicates the state is "don't care".
 4: Writing is executed while S2 high overlaps \overline{S}_1 and \overline{W} low.
 5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of \overline{S}_1 or rising edge of S2, the outputs are maintained in the high impedance state.
 6: Don't apply inverted phase signal externally when DQ pin is output mode.

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

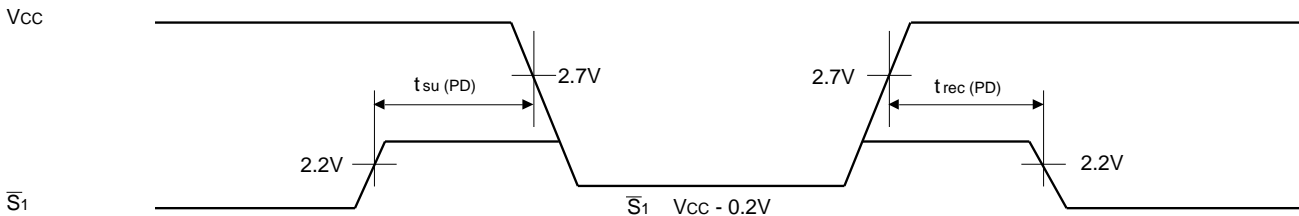
| Symbol | Parameter | Test conditions | Limits | | | Unit | |
|----------------------|----------------------------------|--|--------|---------------------|-----|------|----|
| | | | Min | Typ | Max | | |
| V _{CC (PD)} | Power down supply voltage | | 2 | | | V | |
| V _{I (S1)} | Chip select input \bar{S}_1 | | 2.0 | V _{CC(PD)} | | V | |
| V _{I (S2)} | Chip select input S ₂ | 2.7V V _{CC(PD)} | | | 0.6 | V | |
| | | V _{CC(PD)} <2.7V | | | 0.2 | V | |
| I _{CC (PD)} | Power down supply current | V _{CC} = 3V 1) S ₂ 0.2V, other inputs = 0~3V 2) \bar{S}_1 V _{CC} -0.2V, S ₂ V _{CC} -0.2V other inputs = 0~3V | -H | ~25°C | | 1 | μA |
| | | | | ~40°C | | 3 | |
| | | | -X | ~25°C | | 0.5 | |
| | | | | ~40°C | | 1.5 | |
| | | | -70°C | | 4 | | |

(2) TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------------|--------------------------|-----------------|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| t _{su (PD)} | Power down set up time | | 0 | | | ns |
| t _{rec (PD)} | Power down recovery time | | 5 | | | ms |

(3) POWER DOWN CHARACTERISTICS

\bar{S}_1 control mode



S₂ control mode

