

M5M5255DP,FP -45LL,-55LL,-70LL, -45XL,-55XL,-70XL

262,144-BIT (32,768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5255DP,FP is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5255DP, FP-45LL	45ns	55mA (V _{CC} =5.5V)	20μA (V _{CC} =5.5V)
M5M5255DP, FP-55LL	55ns		
M5M5255DP, FP-70LL	70ns		
M5M5255DP, FP-45XL	45ns	55mA (V _{CC} =5.5V)	5μA (V _{CC} =5.5V)
M5M5255DP, FP-55XL	55ns		0.05μA (V _{CC} =3.0V, Typical)
M5M5255DP, FP-70XL	70ns		

- Single +5V power supply
- No clocks, no refresh
- Data-Hold on +2.0V power supply
- Directly TTL compatible : all inputs and outputs
- Three-state outputs : OR-tie capability
- Simple memory expansion by /S1, S2
- Common Data I/O
- Battery backup capability
- Low stand-by current.....0.05μA(typ.)

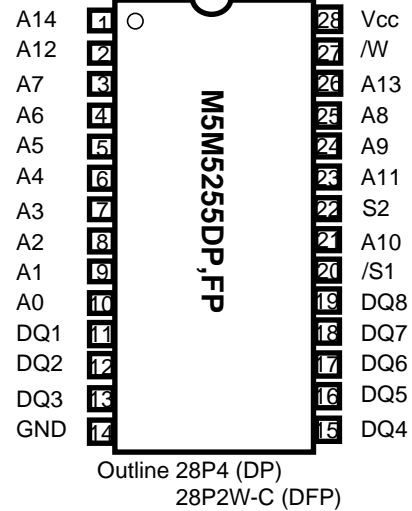
PACKAGE

M5M255DP : 28 pin 600 mil DIP
M5M5255DFP : 28 pin 450 mil SOP

APPLICATION

Small capacity memory units

PIN CONFIGURATION (TOP VIEW)



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FUNCTION

The operation mode of the M5M5255DP,FP is determined by a combination of the device control inputs /S1, S2 and /W. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with the low level /S1 and the high level S2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S1 or S2, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained.

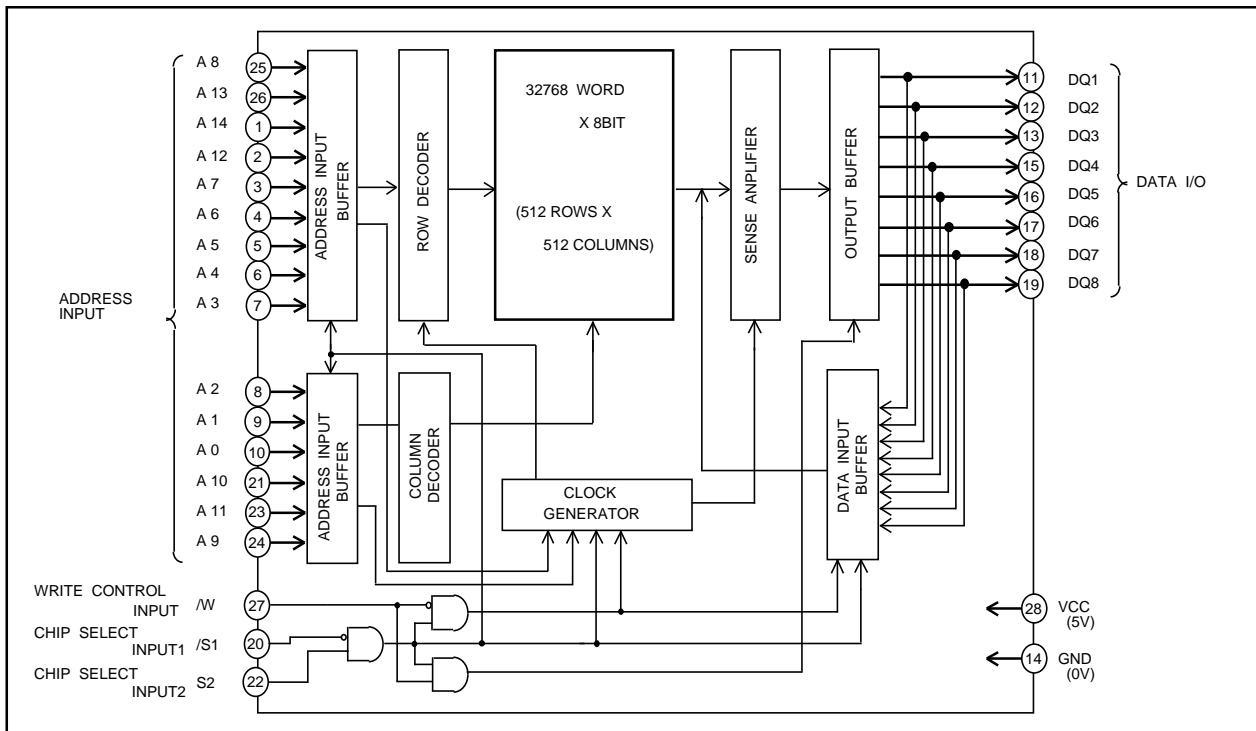
A read cycle is executed by setting /W at a high level while /S1 and S2 are in an active state(/S1="L", S2="H").

When setting /S1 at a high level or S2 at a low level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /S1 and S2. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

/S1	S2	/W	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Non selection	High-impedance	Stand-by
L	H	L	Write	D _{IN}	Active
L	H	H	Read	D _{OUT}	Active

FUNCTION TABLE



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	-0.3*~7.0	V
V _I	Input voltage		-0.3*~V _{cc} +0.3 (Max 7.0)	V
V _O	Output voltage		0~V _{cc}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width 30ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{cc}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{cc} +0.3	V
V _{IL}	Low-level input voltage		-0.3		0.8	V
V _{OH1}	High-level output voltage 1	I _{OH} =-1mA	2.4			V
V _{OH2}	High-level output voltage 2	I _{OH} =-0.1mA	V _{cc} -0.5			V
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	V
I _i	Input current	V _I =0~V _{cc}			±1	uA
I _o	Output current in off-state	/S ₁ =V _{IH} or S ₂ =V _{IL} or /OE=V _{IH} V _{I/O} =0~V _{cc}			±1	uA
I _{cc1}	Active supply current (AC, MOS level)	/S ₁ 0.2V, S ₂ >V _{cc} -0.2V Other inputs<0.2V or >V _{cc} -0.2V Output-open(duty 100%)	45ns	35	50	mA
			55ns	30	45	
			70ns	25	40	
I _{cc2}	Active supply current (AC, TTL level)	/S ₁ =V _{IL} , S ₂ =V _{IH} other inputs=V _{IH} or V _{IL} Output-open(duty 100%)	45ns	35	55	mA
			55ns	30	50	
			70ns	25	45	
I _{cc3}	Stand-by current	S ₂ 0.2V or /S ₁ V _{cc} -0.2V, S ₂ V _{cc} -0.2V other inputs=0~V _{cc}	-LL		20	uA
			-XL		5	
I _{cc4}	Stand-by current	/S ₁ =V _{IH} or S ₂ =V _{IL} , other inputs=0~V _{cc}			3	mA

* -3.0V in case of AC (Pulse width 30ns)

CAPACITANCE (T_a=0~70°C, V_{cc}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _i	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			6	pF
C _o	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			8	pF

Note 0: Direction for current flowing into an IC is positive (no mark).

1: Typical value is one at T_a = 25°C.2: C_i, C_o are periodically sampled and are not 100% tested.

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AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level..... $V_{IH}=2.4V, V_{IL}=0.6V$

Input rise and fall time.....5ns

Reference level..... $V_{OH}=V_{OL}=1.5V$

Output loads.....Fig.1, $CL=30pF$ (-45LL,-45XL)
 $CL=50pF$ (-55LL,-55XL)
 $CL=100pF$ (-70LL,-70XL)
 $CL=5pF$ (for t_{en}, t_{dis})

Transition is measured ±500mV from steady state voltage. (for t_{en}, t_{dis})

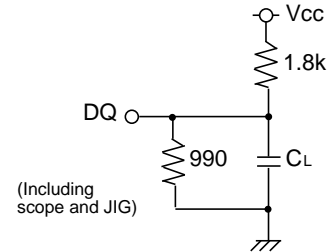


Fig.1 Output load

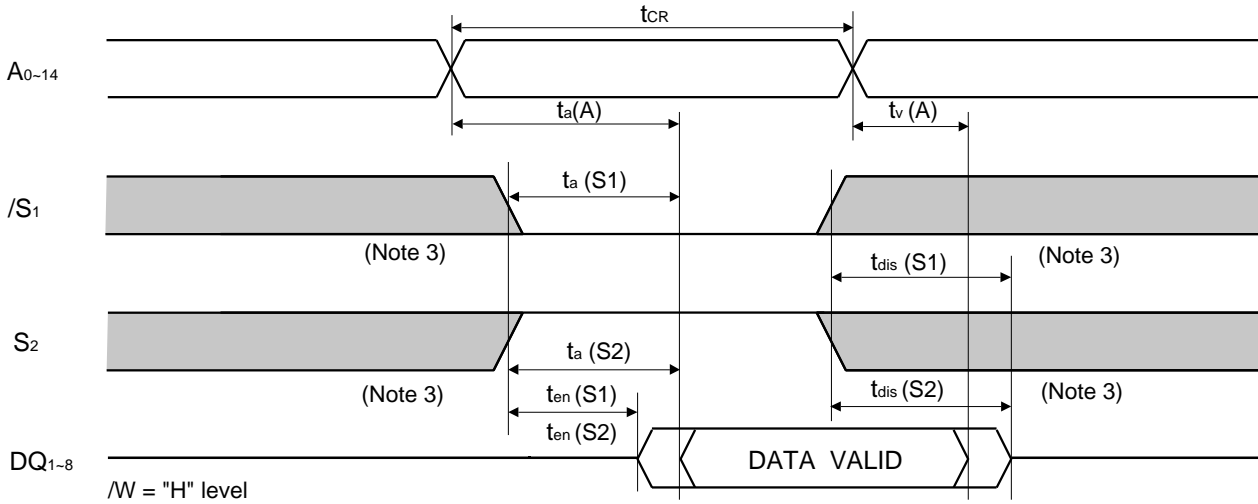
(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		-45LL, XL		-55LL, XL		-70LL, XL		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	45		55		70		ns
$t_{a(A)}$	Address access time		45		55		70	ns
$t_{a(S1)}$	Chip select 1 access time		45		55		70	ns
$t_{a(S2)}$	Chip select 2 access time		45		55		70	ns
$t_{dis(S1)}$	Output disable time after /S ₁ high		15		20		25	ns
$t_{dis(S2)}$	Output disable time after S ₂ low		15		20		25	ns
$t_{en(S1)}$	Output enable time after /S ₁ low	5		5		5		ns
$t_{en(S2)}$	Output enable time after S ₂ high	5		5		5		ns
$t_{v(A)}$	Data valid time after address	10		10		10		ns

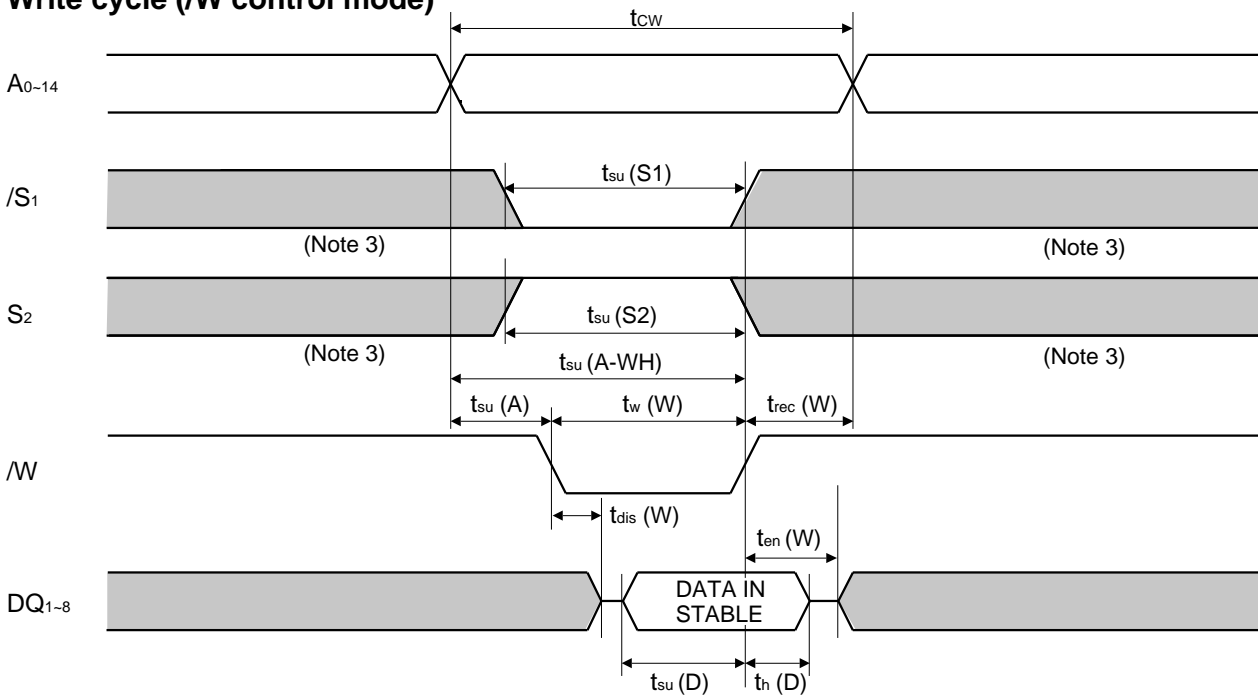
(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		-45LL, XL		-55LL, XL		-70LL, XL		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	45		55		70		ns
$t_{w(W)}$	Write pulse width	35		40		50		ns
$t_{su(A)}$	Address setup time	0		0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to /W	40		50		65		ns
$t_{su(S1)}$	Chip select 1 setup time	40		50		65		ns
$t_{su(S2)}$	Chip select 2 setup time	40		50		65		ns
$t_{su(D)}$	Data setup time	20		25		30		ns
$t_h(D)$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time from /W low		15		20		25	ns
$t_{en(W)}$	Output enable time from /W high	5		5		5		ns

(4) TIMING DIAGRAMS
Read cycle



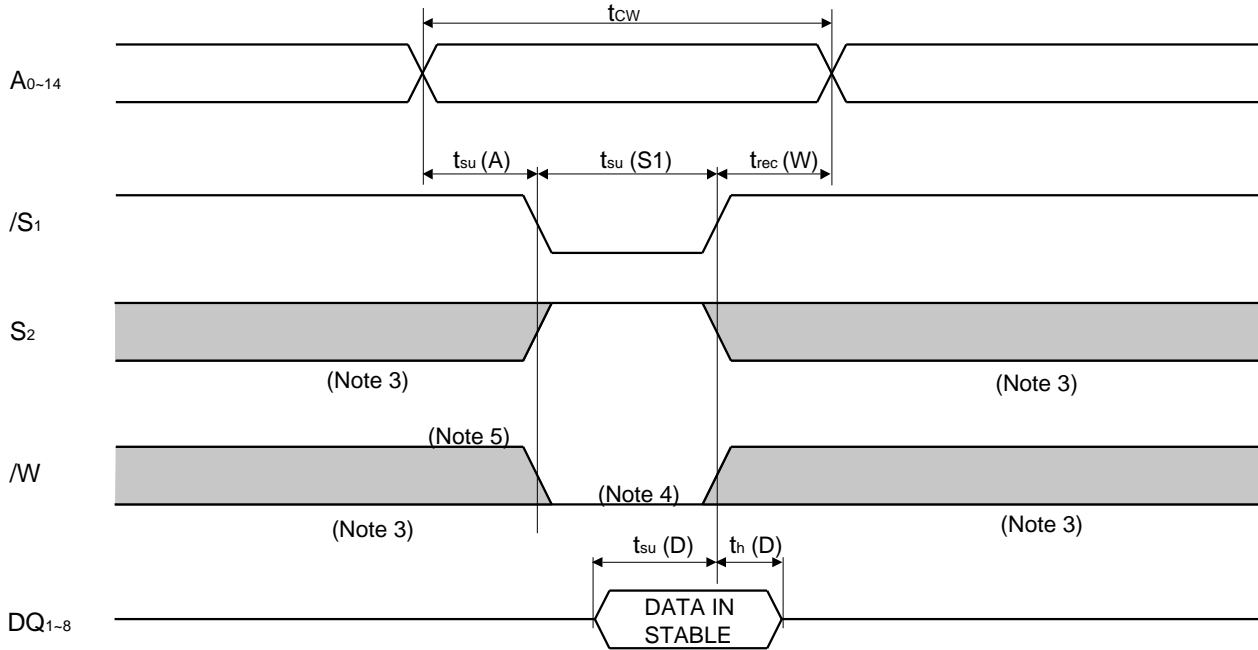
Write cycle (/W control mode)



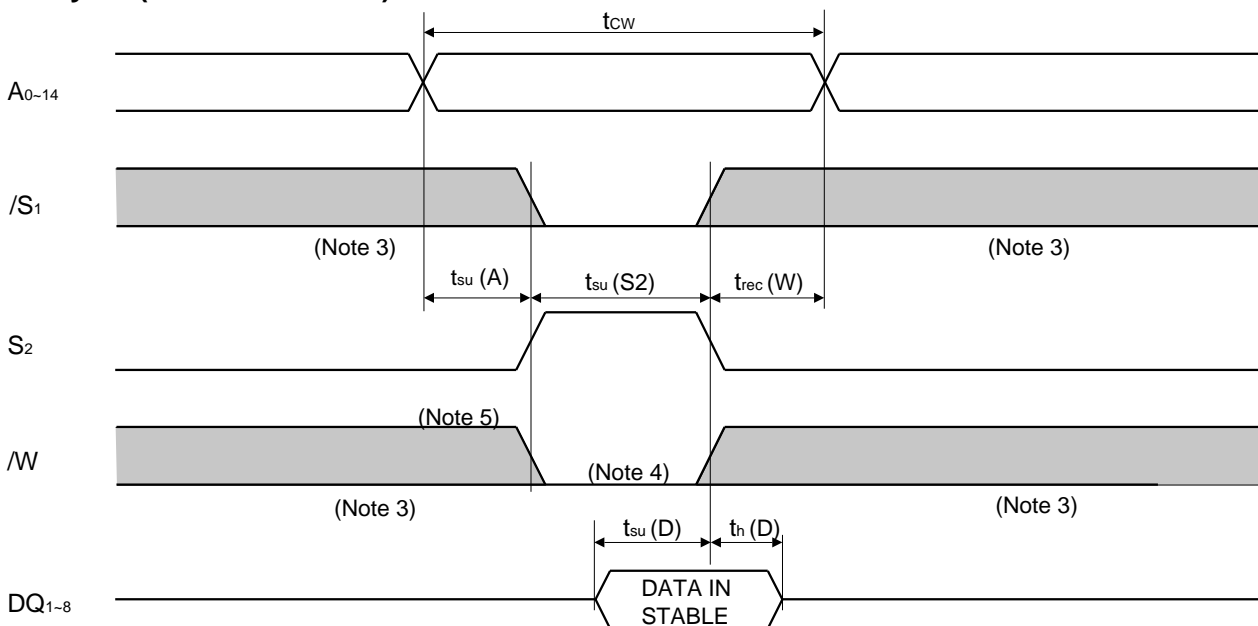
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Write cycle (/S1 control mode)



Write cycle (S2 control mode)



Note 3 : Hatching indicates the state is "don't care".

4 : Writing is executed while S₂ high overlaps /S₁ and /W low.

5 : When the falling edge of /W is simultaneously or prior to the falling edge of /S₁ or rising edge of S₂, the outputs are maintained in the high impedance state.

6 : Don't apply inverted phase signal externally when DQ pin is output mode.

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC(PD)}	Power down supply voltage		2			V
V _{I(S1)}	Chip select input /S ₁	2.2V V _{CC(PD)}	2.2			V
		2V V _{CC(PD)} 2.2V		V _{CC(PD)}		V
V _{I(S2)}	Chip select input S ₂	4.5V V _{CC(PD)}			0.8	
		V _{CC(PD)} <4.5V			0.2	
I _{CC(PD)}	Power down supply current	V _{CC} = 3V S ₂ 0.2V or /S ₁ V _{CC} -0.2V, S ₂ V _{CC} -0.2V	-LL		10 (Note 7)	uA
			-XL	0.1	2 (Note 8)	

Note7: I_{CC(PD)} = 1uA in case of Ta = 25°C

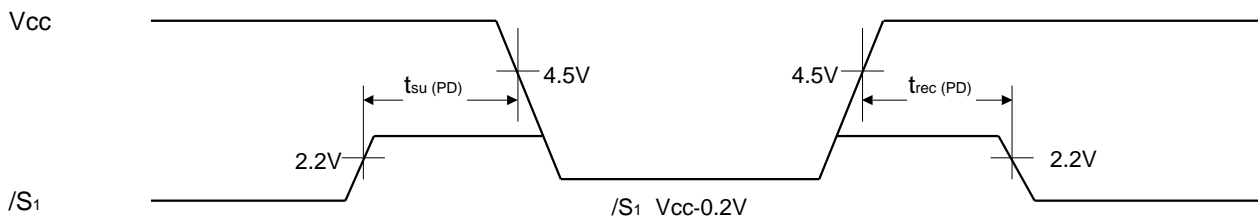
Note8: I_{CC(PD)} = 0.5uA in case of Ta = 25°C

(2) TIMING REQUIREMENTS (Ta = 0~70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su(PD)}	Power down set up time		0			ns
t _{rec(PD)}	Power down recovery time		t _{CR}			ns

(3) POWER DOWN CHARACTERISTICS

/S₁ control mode



S₂ control mode

