M5M28F101AFP,J,VP,RV-85,-10

1048576-BIT (131072-WORD BY 8-BIT) CMOS FLASH MEMORY

DESCRIPTION

The MITSUBISHI M5M28F101A is high-speed 1048576-bit CMOS Flash Memories. This is suitable for the applications with micro-processor or micro-controller where on-board reprogramming is required. The M5M28F101A is fabricated by N-channel double polysilicon gate for memory and CMOS technology for peripheral circuits, and is available in 32pin plastic molded packages.

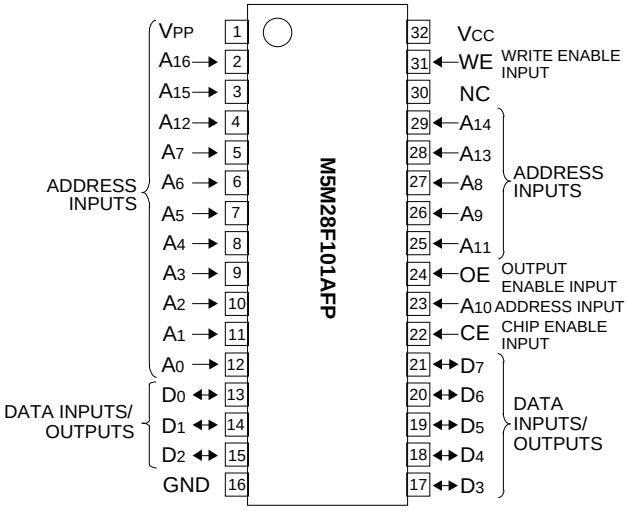
FEATURES

- Speed item ····· 85 ns (max.)
  100 ns (max.)
- Power supply voltage ····· V_{CC} = 5V±0.5V
- Write and erase voltage ····· V_{PP} = 12V±0.6V
- Byte program and Chip erase
- Auto program and Auto erase
- Program/erase operation controlled by software command
- Program/erase pulse controlled by an embedded timer
- 10000 program/erase cycles
- Tri-state output buffer
- TTL-compatible input and output in read and write mode
- Contained device-identifier code
- Incorporated data-protection
- Available packaging for Surface Mount

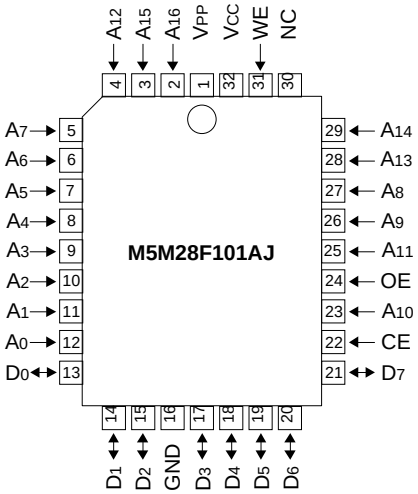
APPLICATION

Micro-computer system and peripheral equipment

PIN CONFIGURATION (TOP VIEW)



Outline 525mil 32pin SOP (32P2M-A)



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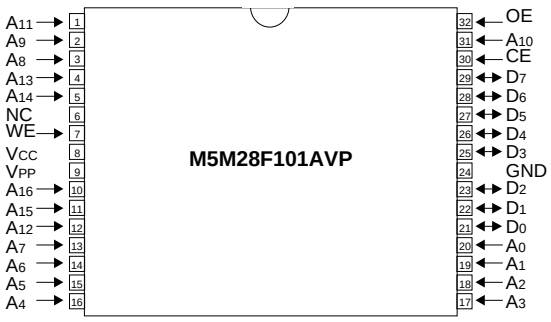
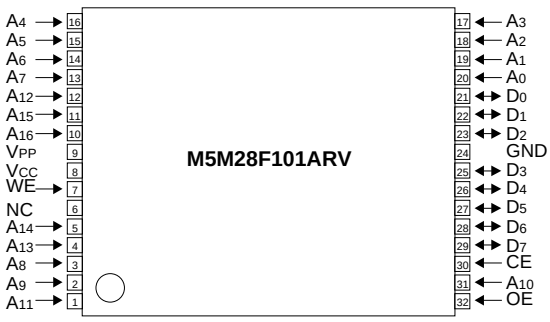


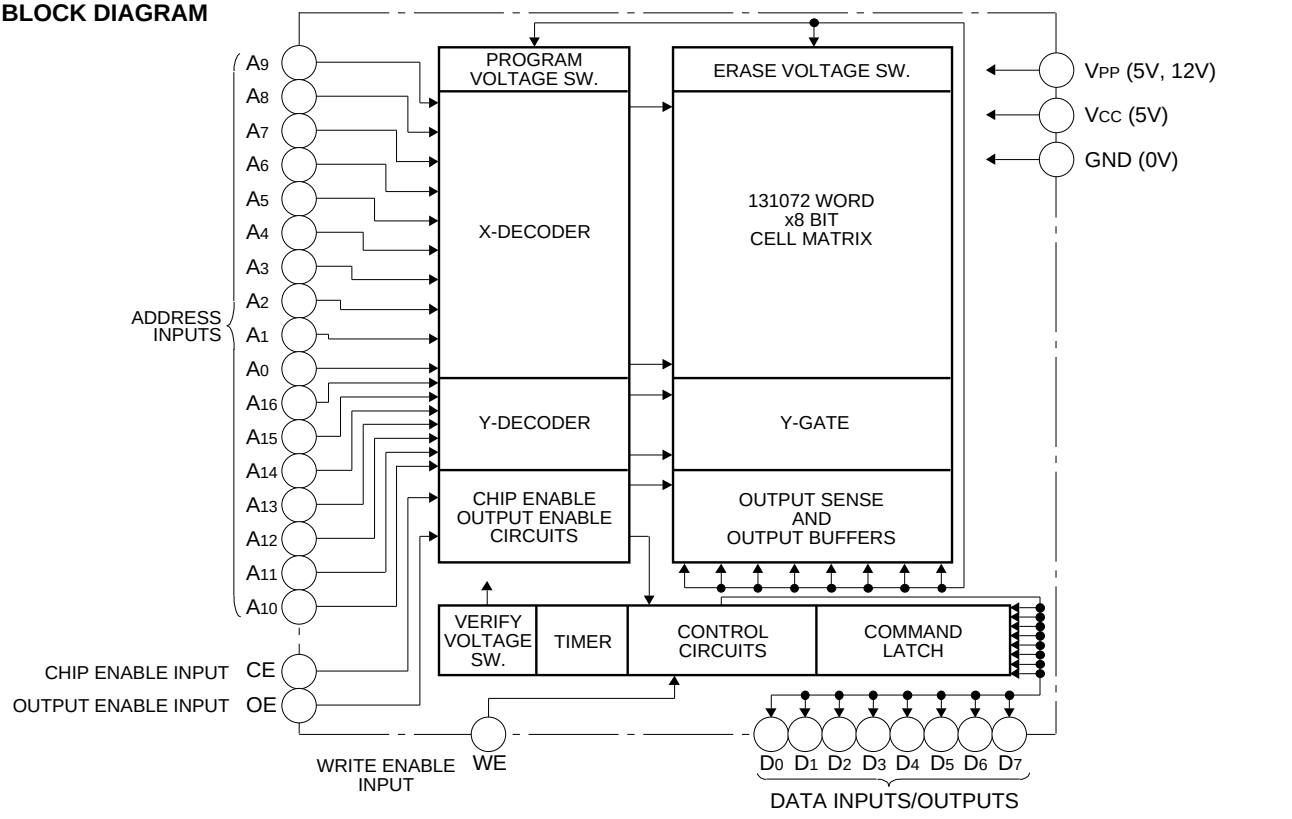
Outline 32pin TSOP type-I (8x20mm)
32P3H-E (normal bend)



Outline 32pin TSOP type-I (8x20mm)
32P3H-F (reverse bend)

NC : NO CONNECTION

BLOCK DIAGRAM



FUNCTION

M5M28F101A are set to the Read-only mode or Read-write mode by applying the voltage of V_{PPL} or V_{PPH}, respectively, to V_{PP} pin. In Read-only mode, three operation modes, Read, Out-put disable and Stand-by are accessible. While, in Read-Write mode, four operation modes, Read, Output disable, Stand-by and Write are functional.

Read

Set CE and OE terminals to the read mode (low level). Low level input to CE and OE, and address signals to the address inputs (A_0~A_{16}) make the data contents of the designated address location available at data input/output(D_0~D_7).

Output Disable

When OE is at high level, output from the devices is disabled. Data input/output are in a high-impedance (High-Z) state.

Stand-by

When CE is at high level, the devices is in the stand-by mode and its power consumption is substantially reduced. Data input/output are in a high-impedance (High-Z) state.

Write

Software command accomplishes program and erase operations via the command latch in the device, when high voltage is supplied to V_{PP}. The contents of the latch serve as input to the internal controller. The controller output dictates the function of device. The command latch is written by bringing WE to low level, while CE is at low level and OE is at high level. Addresses are latched on the falling edge of WE, while data is latched on the rising edge of WE. Standard micro-processor write timings are used.

DATA PROTECTION

1. Power Supply Voltage
   When the power supply voltage (Vcc) is less than 2.5V, the device ignores WE signal.
2. Write Inhibit
   In the cases, as below, write mode is not set.
   1) When OE is terminated to the low level.
   2) From each mode beginning through finish after 2nd rising edge of WE for program, auto-program, erase, and auto-erase.
3. Over-erase Protection
   Just after powering up, if erase command is inputted, erase operation is not executed. Once byte-program is performed or verified data is not FFH in the erase-verify mode, successive command input for erase will be accepted. Because of this, it is applicable to the case of multi-chip erasing simultaneously.

SOFTWARE COMMAND

When V_{PP} is low ($V_{PP} = V_{PPL}$), the contents of the command latch are fixed to 00H, and the device is in read-only mode. When V_{PP} is high ($V_{PP} = V_{PPH}$), the device enters read/write mode. The device operations are selected by writing specific software command into the command latch.

Read Command

The device is in read mode after writing Read Command (00H) to the command latch. The device continues to be in read mode until the other commands are written. When V_{PP} powers-up to high voltage ($V_{PP} = V_{PPH}$), the default contents of the command latch is 00H. So it is ensured that the false alteration of memory data does not occur during V_{PP} power transition.

Program Command

Program Command is the command for byte-program, and program is initiated by twice of write cycles. Program Command (40H) is written to the command latch in first write cycle, and the address and data to be programmed are latched in second write cycle. Then the address and data are latched on the falling edge and the rising edge of WE pulse, respectively. The byte- program operation is initiated at the rising edge of WE in second write cycle, and terminates in 10 µs, controlled by the internal timer.

Program Verify Command

Following byte program, the programmed byte must be verified. The program-verify is initiated by writing Program Verify Command (C0H) to the command latch. After writing Program Verify Command, programmed data is verified in read mode. Then the address information is not needed.

Auto Program Command

Auto Program Command is the command for automated program and program-verify of one byte, and Auto Program is initiated by twice of write cycles.

Auto Program Command (10H or 50H) is written to the command latch in first write cycle, and the address and data to be programmed are latched in second write cycle. Then the address and data are latched on the falling edge and the rising edge of WE pulse, respectively. The program operation is initiated at the rising edge of WE in second write cycle, and program-verify begin automatically. So it is not necessary to program-verify mode after this. And the complete of Auto Program can be indicated by data polling.

Data polling is the indication of the complete of Auto Program. During the Auto Program, on $WE=V_{IH}$ and $CE=OE=V_{IL}$, the data of D_0~D_7 are the inverse of written datum. When Auto Program is completed, the written datum will be output. It is necessary to fix the address of written byte during data polling.

Erase Command

Erase Command is the command for chip-erase, and chip-erase is initiated by writing twice of the Erase Command (20H) consecutively to the command latch. The erase operation is initiated with the rising edge of the WE pulse and terminates in 9.5ms, controlled by the internal timer. This two-step sequence for chip-erase prevents from erasing accidentally.

Erase Verify Command

Following each erase, all bytes must be verified. The erase verify is initiated by writing Erase Verify Command (A0H) to the command latch, while the address to be verified is latched on the falling edge of the WE pulse. The erase verify command must be written to the command latch and each address is latched before each byte is verified. The operation continues for each byte until a byte is not erased, or the last address is accessed.

Auto Erase Command

Auto Erase Command is the command for automated erase and erase-verify of all bytes, and Auto Erase is initiated by twice of the Erase Command (30H) consecutively to the command latch. First, the preprogram operation is initiated at the rising edge of WE in second write cycle, and so all byte become zero data. Second, erase and erase-verify begin, automatically. So it is not necessary to preprogram and erase-verify mode. And the complete of Auto Erase can be indicated by status polling.

Status polling is the indication of the complete of Auto Erase. During the Auto Erase, on $WE=V_{IH}$ and $CE=OE=V_{IL}$, the data of D_7 is "0". When Auto Erase is completed, the data of D_7 is "1". (D_0~D_7 are "FFH".)

Reset Command

Reset Command is the command to safely abort the erase or program sequences. Following erase or program command in first write cycle, the operation is aborted safely by writing the two consecutive Reset Commands (FFH). Then the device enters read mode without altering memory contents.

Read Device Identifier Code

Device Identifier operation is initiated by writing 80H into the command latch. Following the command write, the manufacturer code (1CH) and the device code (D9H) can be read from address-00000H and 00001H, respectively.

The M5M28F101A is supported with the Common Device Identifier Code of MITSUBISHI 1M Flash memory (x8) family. Common Device Identifier operation is initiated by writing 90H into the command latch. Under this case, following the command write, the manufacturer code (1CH) and the device code (D0H) can be read from address-00000H and 00001H, respectively. Additionally, Common Device Identifier operation is initiated by rising A_9 to high voltage for PROM programmers.

MODE SELECTION

Mode \ Pins		CE	OE	WE	V_{PP}	Data I/O
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	Hi-Z
	Stand by	V_{IH}	X	X	V_{PPL}	Hi-Z
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	Data out
	Output disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	Hi-Z
	Stand by	V_{IH}	X	X	V_{PPH}	Hi-Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	Data out

Note 1 : X can be V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{I1}	All input or output voltage except V_{PP}/A_9	With respect to Ground	–0.6~7	V
V_{I2}	V_{PP} supply voltage		–0.6~14.0	V
V_{I3}	A_9 supply voltage		–0.6~13.5	V
T_{opr}	Operating temperature		–10~80	°C
T_{stg}	Storage temperature		–65~125	°C

SOFTWARE COMMAND DEFINITION

Command	First bus cycle			Second bus cycle		
	Mode	Address	Data I/O	Mode	Address	Data I/O
Read	Write	X	00H	——	——	——
Program (Byte Program)	Write	X	40H	Write	Program Address	Program Data
Program verify	Write	X	C0H	Read	X	Verify Data
Auto Program	Write	X	10H or 50H	Write	Program Address	Program Data
Erase (Chip Erase)	Write	X	20H	Write	X	20H
Erase verify	Write	Verify address	A0H	Read	X	Verify Data
Auto Erase	Write	X	30H	Write	X	30H
Reset	Write	X	FFH	Write	X	FFH
Read device identifier code	Write	X	80H	Read	ADI	DDI1
Read common device identifier code	Write	X	90H	Read	ADI	DDI2

Note 2 : Write and read mode are defined in mode selection table.
ADI = Address of Device Identifier : 00000H for manufacturer code, 00001H for device code.
DDI1 = Data of Device Identifier : 1CH for manufacturer code, D9H for device code.
DDI2 = Data of Common Device Identifier : 1CH for manufacturer code, D0H for device code.

COMMON DEVICE IDENTIFIER CODE (not use the software command)

Code \ Pins	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Hex. Data
Manufacturer Code	V_{IL}	0	0	0	1	1	1	0	0	1CH
Device Code	V_{IH}	1	1	0	1	0	0	0	0	D0H

Note 3 : A_9 = 11.5V~13.0V
A_1~A_8, A_{10}~A_{16}, CE, OE = V_{IL}, WE = V_{IH}
V_{CC} = V_{PP} = 5V±0.5V

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, CE, OE, WE)	Ta = 25°C, f = 1MHz, V_{in} = V_{out} = 0V			8	pF
C_{OUT}	Output capacitance				12	pF

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V±0.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$			10	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$			10	µA
I_{SB1}	V_{CC} stand-by current	V_{CC} = 5.5V, CE = V_{IH}			1	mA
I_{SB2}		V_{CC} = 5.5V, CE = V_{CC}±0.2V			100	µA
I_{CC1}	V_{CC} active read current	V_{CC} = 5.5V, CE = V_{IL}, f = 11.8MHz, I_{OUT} = 0mA			30	mA
I_{CC2}	V_{CC} program current	V_{PP} = V_{PPH}			30	mA
I_{CC3}	V_{CC} erase current	V_{PP} = V_{PPH}			30	mA
I_{PP1}	V_{PP} read current	$0V \le V_{PP} \le V_{CC}$			10	µA
		$V_{CC} < V_{PP} \le 6.5V$			100	
		V_{PP} = V_{PPH}			100	
I_{PP2}	V_{PP} program current	V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} erase current	V_{PP} = V_{PPH}			30	mA
V_{IL}	Input low voltage		– 0.5		0.8	V
V_{IH}	Input high voltage		2.0		Vcc+0.5	V
V_{OL}	Output low voltage	I_{OL} = 5.8mA			0.45	V
V_{OH1}	Output high voltage	I_{OH} = –2.5mA	2.4			V
V_{OH2}		I_{OH} = –100µA	Vcc–0.4			
V_{PPL}	V_{PP} voltage during read-only mode		0		6.5	V
V_{PPH}	V_{PP} voltage during read/write mode		11.4	12.0	12.6	V

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V±0.5V, unless otherwise noted)
Read-Only Mode

Symbol		Parameter	Limits				Unit
			M5M28F101A-85		M5M28F101A-10		
			Min	Max	Min	Max	
t_{RC}	t_{AVAV}	Read cycle time	85		100		ns
$t_{a\,(AD)}$	t_{AVQV}	Address access time		85		100	ns
$t_{a\,(CE)}$	t_{ELQV}	Chip enable access time		85		100	ns
$t_{a\,(OE)}$	t_{GLQV}	Output enable access time		45		50	ns
t_{CLZ}	t_{ELQX}	Chip enable to output in low Z	0		0		ns
t_{OLZ}	t_{GLQX}	Output enable to output in low Z	0		0		ns
t_{DF}	t_{GHQZ}	Output enable high to output in low Z		25		25	ns
t_{OH}	t_{OH}	Output hold from CE, OE, addresses	0		0		ns
t_{WRR}	t_{WHGL}	Write recovery time before read	6		6		µs

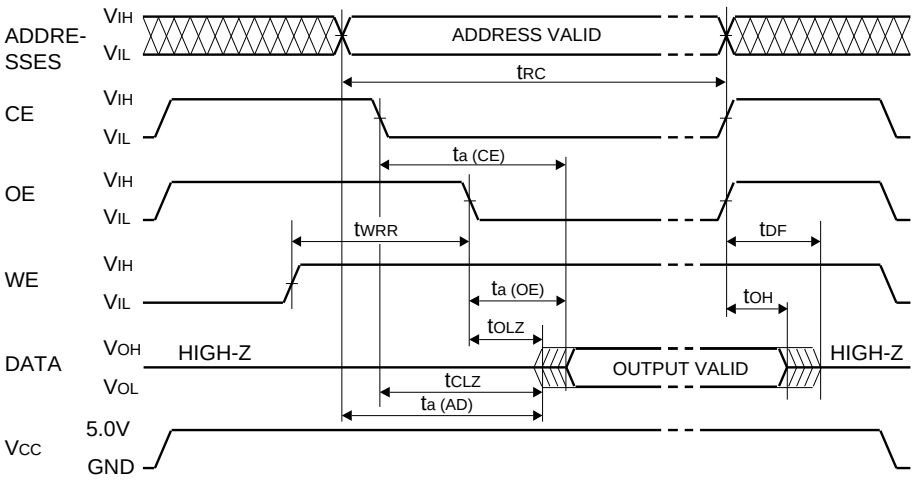
Note 4 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
Timing measurements are made under AC WAVEFORMS FOR READ OPERATIONS.

Read/Write Mode

Symbol		Parameter	Limits				Unit
			M5M28F101A-85		M5M28F101A-10		
			Min	Max	Min	Max	
t_{WC}	t_{AVAV}	Write cycle time	85		100		ns
t_{AS}	t_{AVWL}	Address set-up time	0		0		ns
t_{AH}	t_{WLAX}	Address hold time	60		60		ns
t_{DS}	t_{DVWH}	Data set-up time	50		50		ns
t_{DH}	t_{WHDX}	Data hold time	10		10		ns
t_{WRR}	t_{WHGL}	Write recovery time before read	6		6		µs
t_{RRW}	t_{GHWL}	Read recovery time before write	0		0		ns
t_{CS}	t_{ELWL}	Chip enable set-up time	20		20		ns
t_{CH}	t_{WHEH}	Chip enable hold time	0		0		ns
t_{WP}	t_{WLWH}	Write pulse width	60		60		ns
t_{WPH}	t_{WHWL}	Write pulse width high	20		20		ns
t_{DP}	t_{WHWL1}	Duration of program operation	10		10		µs
t_{DE}	t_{WHWL2}	Duration of erase operation	9.5		9.5		ms
t_{OEH}		Output enable hold time before status / data polling	100		100		ns
t_{DAEC}		Duration of auto erase operation	1.7	12.5	1.7	12.5	s
t_{DAP}		Duration of auto program operation	12	400	12	400	µs
t_{VSC}	t_{VPEH}	V_{PP} set-up time to chip enable low	1		1		µs
t_{OWP}		Write pulse width (optional write)	70		70		ns
t_{OWS}		Write enable set-up time (optional write)	0		0		ns
t_{OWH}		Write enable hold time (optional write)	0		0		ns
t_{OAS}		Address set-up time (optional write)	0		0		ns
t_{OAH}		Address hold time (optional write)	55		55		ns
t_{ODS}		Data set-up time (optional write)	45		45		ns
t_{ODH}		Data hold time (optional write)	20		20		ns

Note 5 : a. Read timing parameters during read/write mode are the same as during read-only mode.
b. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

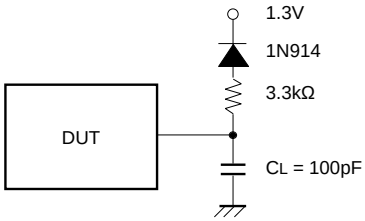
AC WAVEFORMS FOR READ OPERATIONS



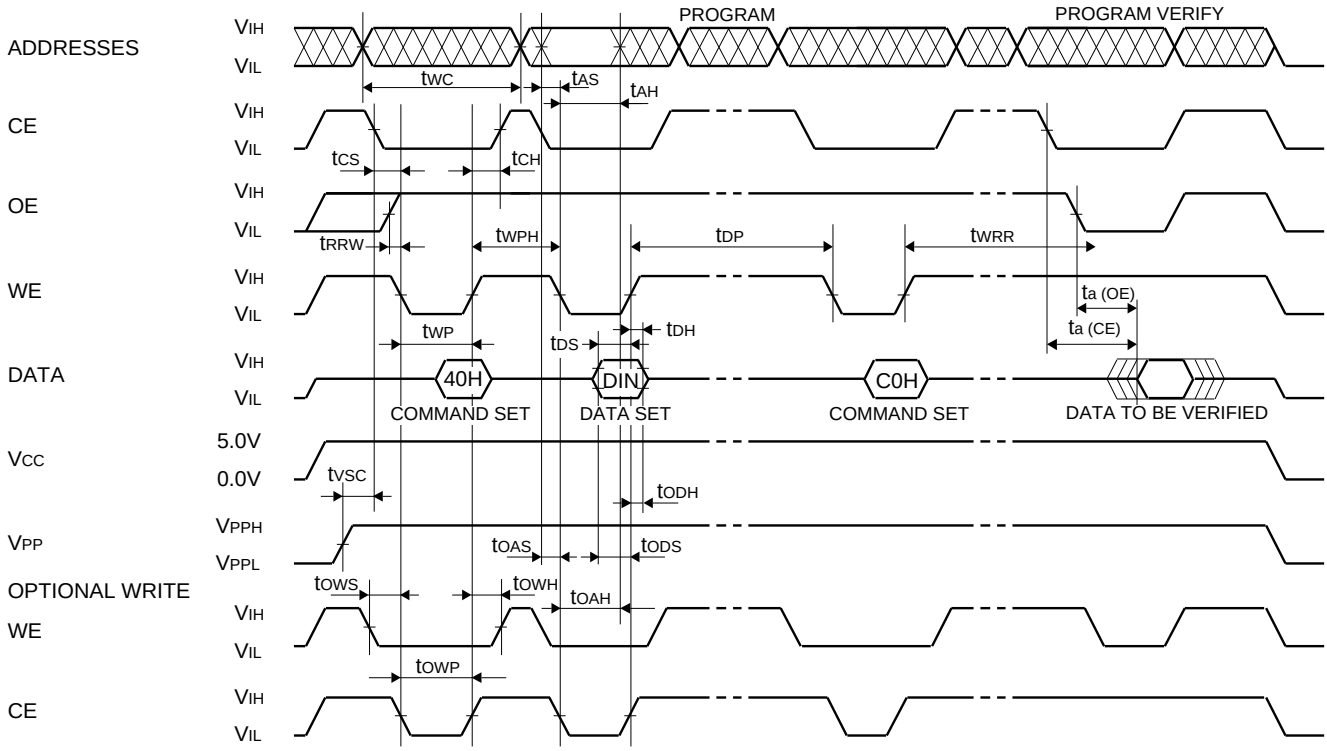
TEST CONDITIONS
FOR AC CHARACTERISTICS

Input voltage : V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times : ≤10ns
Reference voltage
at timing measurement : 1.5V
Output load : 1TTL gate + C_L
(= 100pF)

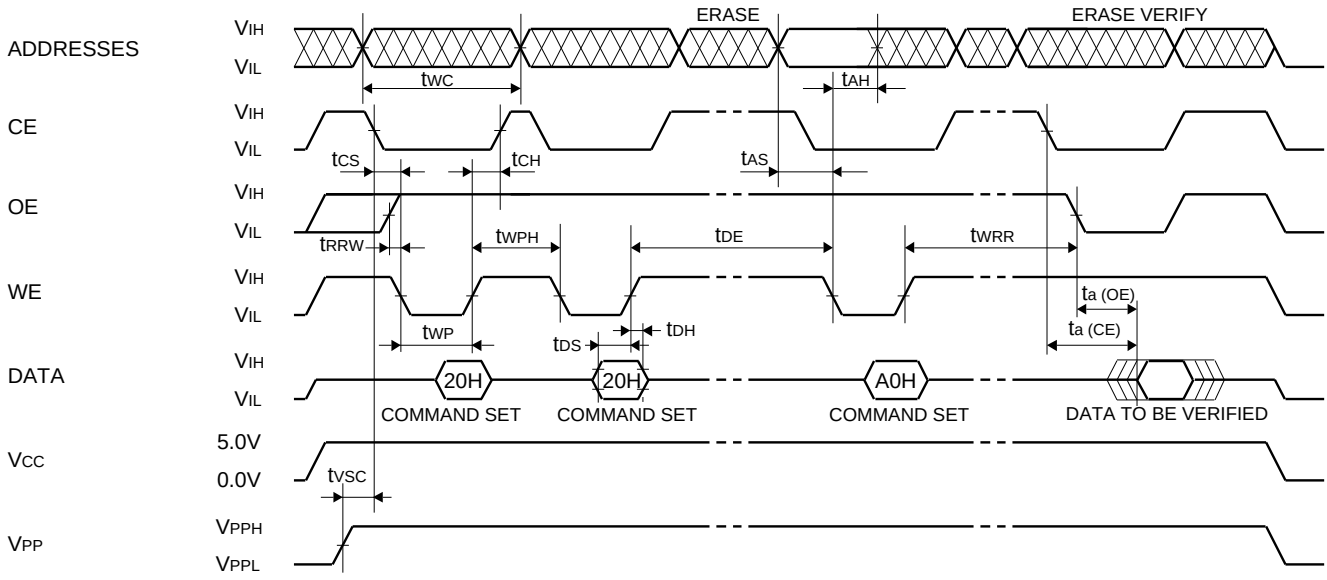
or



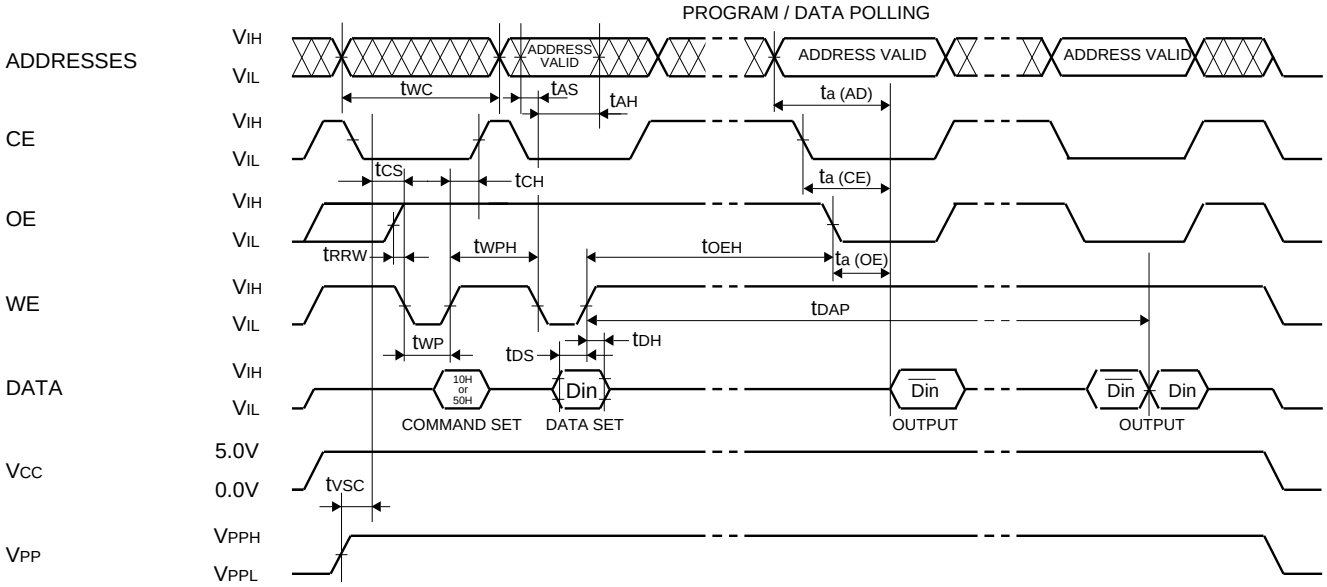
AC WAVEFORMS FOR PROGRAM OPERATIONS



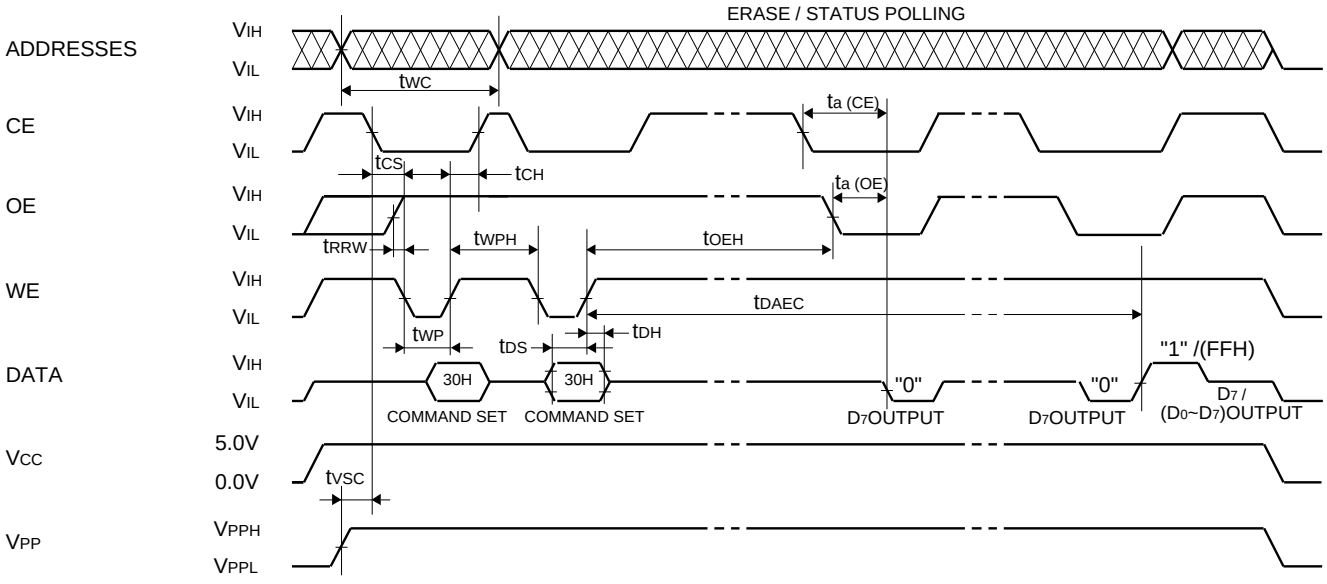
AC WAVEFORMS FOR ERASE OPERATIONS



AC WAVEFORMS FOR AUTO PROGRAM OPERATION

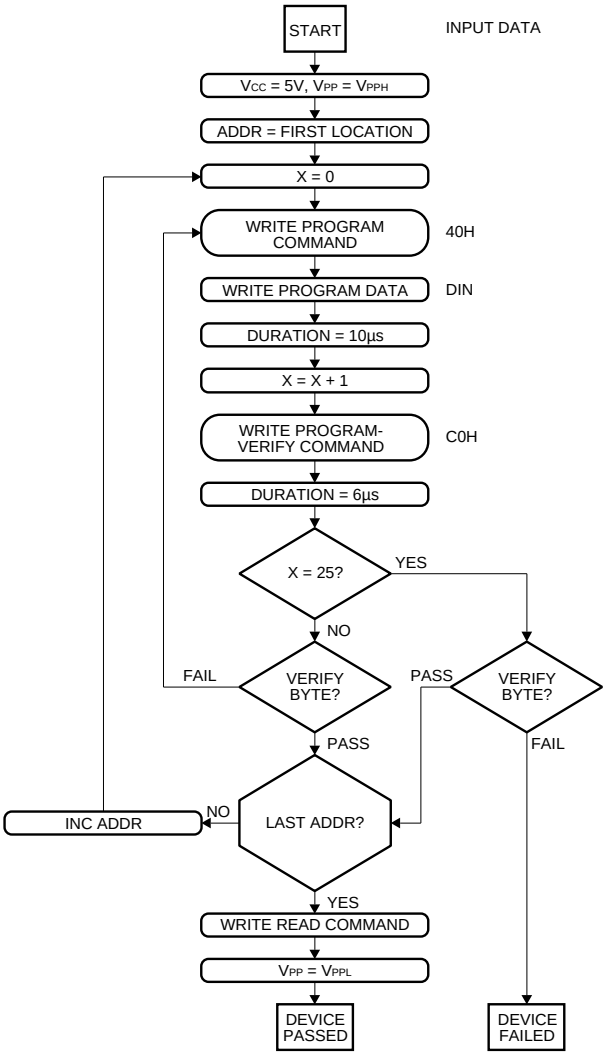


AC WAVEFORMS FOR AUTO CHIP ERASE OPERATION

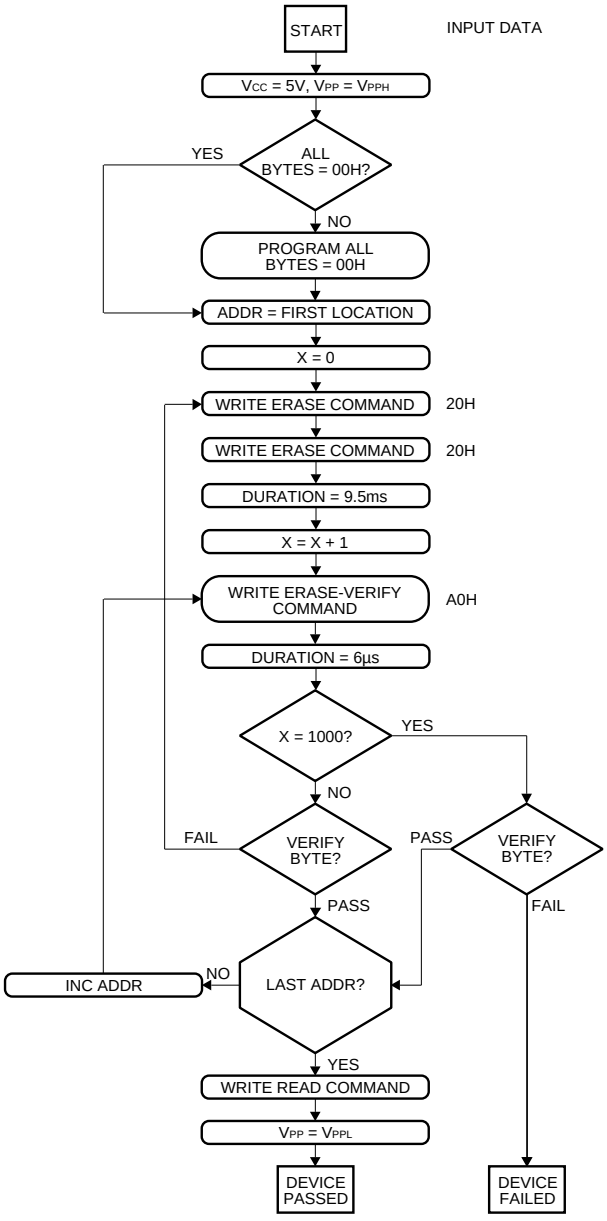


PROGRAMMING AND ERASE ALGORITHM FLOW CHART

PROGRAM :



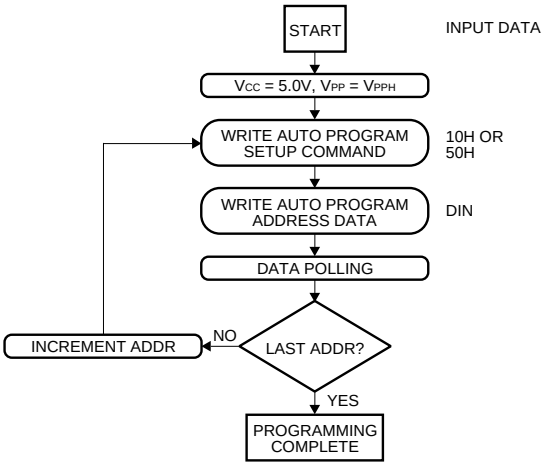
ERASE :



(Erase Complete)

AUTO PROGRAM AND AUTO ERASE OPERATION

AUTO PROGRAM :



AUTO ERASE :