

Surface Mount

# Monolithic Amplifier

**NEW!**

**ERA-4XSM**

50Ω, Broadband, DC to 4 GHz



CASE STYLE : WW107

## Features

- wide bandwidth, DC-4 GHz
- gain, 14.7 dB typ. at 100 MHz
- high dynamic range, 4.2 dB NF, 35 dBm IP3
- low thermal resistance for high reliability
- supply voltage transient protection
- patent pending

## Applications

- cellular
- PCS
- communication receivers & transmitters

## Electrical Specifications @ 25°C

MODEL NO.	FREQ.* (GHz)	GAIN, dB Typical						MAXIMUM POWER (dBm) @1GHz			DYNAMIC RANGE @2GHz		VSWR (:1) Typ.				MAXIMUM RATING**		DC OPERATING POWER @ Pin 3***			THERMAL RESISTANCE θjc, typ. °C/W	PRICE \$ Qty. (25)	
		over frequency, GHz					Min. @ 2 GHz	Output (1dB Comp.) Typ. Min.	Input (no dmg.) Typ. Min.	NF (dB) Typ.	IP3 (dBm) Typ.	In DC-3 GHz	Out DC-2 GHz	I mA	P mW	Cur-rent (mA) Typ	Volt Min	Max						
ERA-4XSM	DC-4	14.7	14.2	13.5	12.0	11.8	12	17.0	15	20	4.2	35	1.2	1.2	1.2	1.4	100	650	65	4.5	4.2	5.5	196	1.69

\* Low frequency cutoff determined by external coupling capacitors.  
 \*\* Permanent damage may occur if any of these limits are exceeded. These ratings are not intended for continuous normal operation.  
 \*\*\*Reliability predictions and normal operating conditions are applicable at current specified.

## Maximum Ratings

Operating Temperature -45°C to 85°C  
 Storage Temperature -65°C to 150°C

## Model Identification

Model	Marking†
ERA-4XSM	4X

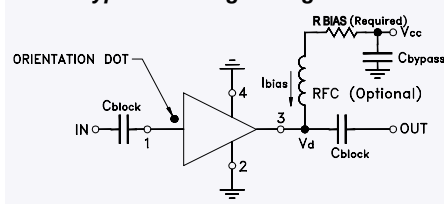
† Prefix letter (optional) designates assembly location. Suffix letters (optional) are for wafer identification.

## Pin Configuration

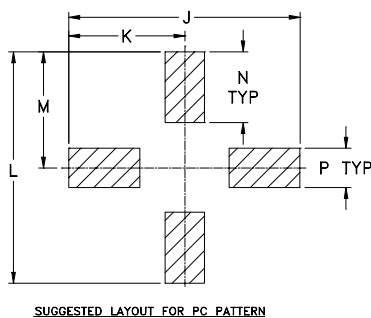
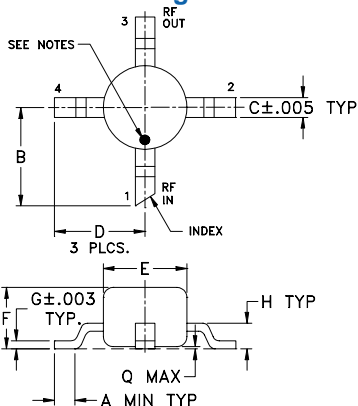
RF IN	1
RF OUT	3
DC	3
GND EXT.	2,4

R BIAS	
*1% Resistor Values	
Vcc	ERA-4XSM
7	38.3
8	52.3
9	66.5
10	80.6
11	95.3
12	110
13	127
14	143
15	158
16	174
17	187
18	205
19	221
20	237

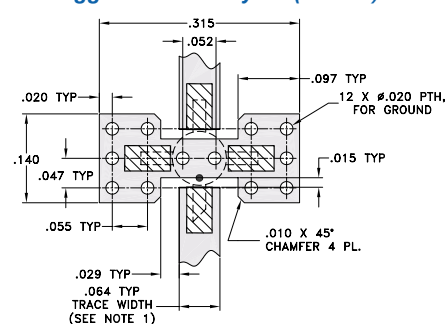
## Typical Biasing Configuration



## Outline Drawing



## Suggested PCB Layout (PL-075)



## NOTES:

1. TRACE WIDTH IS SHOWN FOR ROGERS RO4350 WITH DIELECTRIC THICKNESS 0.030" ± 0.002", COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. IF YOUR PCB DESIGN RULES ALLOW, GROUND VIAS SHOULD BE PLACED UNDER THE LAND PATTERN FOR BETTER RF PERFORMANCE. OTHERWISE GROUND VIAS SHOULD BE PLACED AS CLOSE TO LAND PATTERN AS POSSIBLE.

- DENOTES PCB COPPER LAYOUT
- ▨ DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

## Outline Dimensions (inch/mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	wt. grams
.012	.10	.020	.092	.085	.060	.007	.026	.235	.118	.235	.118	.072	.040	.020	
.30	2.54	.51	2.34	2.16	1.52	.18	.66	5.97	3.00	5.97	3.00	1.83	1.02	0.51	.015



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