DRAM MODULE

MT9D436
MT18D836

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/datasheets

FEATURES

- Four-CAS#, ECC-optimized configuration in a 72-pin, single in-line memory module (SIMM)
- 16MB (4 Meg x 36) and 32MB (8 Meg x 36)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE (FPM) access

OPTIONS — MARKING

- Timing
  60ns access — -6
- Packages
  72-pin SIMM — M
  72-pin SIMM (Gold) — G

KEY TIMING PARAMETERS

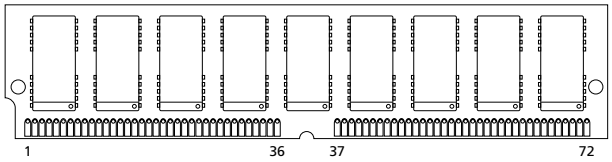
SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

PART NUMBERS

PART NUMBER	CONFIGURATION	FEATURES	MODE
MT9D436M-x	4 Meg x 36	4 CAS#, ECC	FPM
MT9D436G-x	4 Meg x 36	4 CAS#, ECC	FPM
MT18D836M-x	8 Meg x 36	4 CAS#, ECC	FPM
MT18D836G-x	8 Meg x 36	4 CAS#, ECC	FPM

x = speed

PIN ASSIGNMENT (Front View)
72-Pin SIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{SS}	19	A10	37	DQ18	55	DQ13
2	DQ1	20	DQ5	38	DQ36	56	DQ31
3	DQ19	21	DQ23	39	V_{SS}	57	DQ14
4	DQ2	22	DQ6	40	CAS0#	58	DQ32
5	DQ20	23	DQ24	41	CAS2#	59	V_{DD}
6	DQ3	24	DQ7	42	CAS3#	60	DQ33
7	DQ21	25	DQ25	43	CAS1#	61	DQ15
8	DQ4	26	DQ8	44	RAS0#	62	DQ34
9	DQ22	27	DQ26	45	NC/RAS1#*	63	DQ16
10	V_{DD}	28	A7	46	NC	64	DQ35
11	NC	29	NC (A11)	47	WE#	65	DQ17
12	A0	30	V_{DD}	48	NC	66	NC
13	A1	31	A8	49	DQ10	67	PRD1
14	A2	32	A9	50	DQ28	68	PRD2
15	A3	33	NC/RAS3#*	51	DQ11	69	PRD3
16	A4	34	RAS2#	52	DQ29	70	PRD4
17	A5	35	DQ27	53	DQ12	71	NC
18	A6	36	DQ9	54	DQ30	72	V_{SS}

*32MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

GENERAL DESCRIPTION

The MT9D436 and MT18D836 are randomly accessed, 16MB and 32MB solid-state memories organized in a x36 configuration. These modules are designed for systems that utilize ECC and do not conduct single-byte accesses. These modules do not support parity functionality.

During READ or WRITE cycles, each bit is uniquely addressed through 20 address bits that are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS#, the latter 10 bits. READ or WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. EARLY WRITE occurs when WE# goes LOW prior to CAS# going LOW, and the output pin(s) remain open (High-Z) until the next CAS# cycle.

PAGE MODE

Page operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The page cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning

PAGE MODE (continued)

RAS# HIGH terminates page mode operation, i.e., closes the page.

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing anyRAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS# ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS# addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS# addressing.

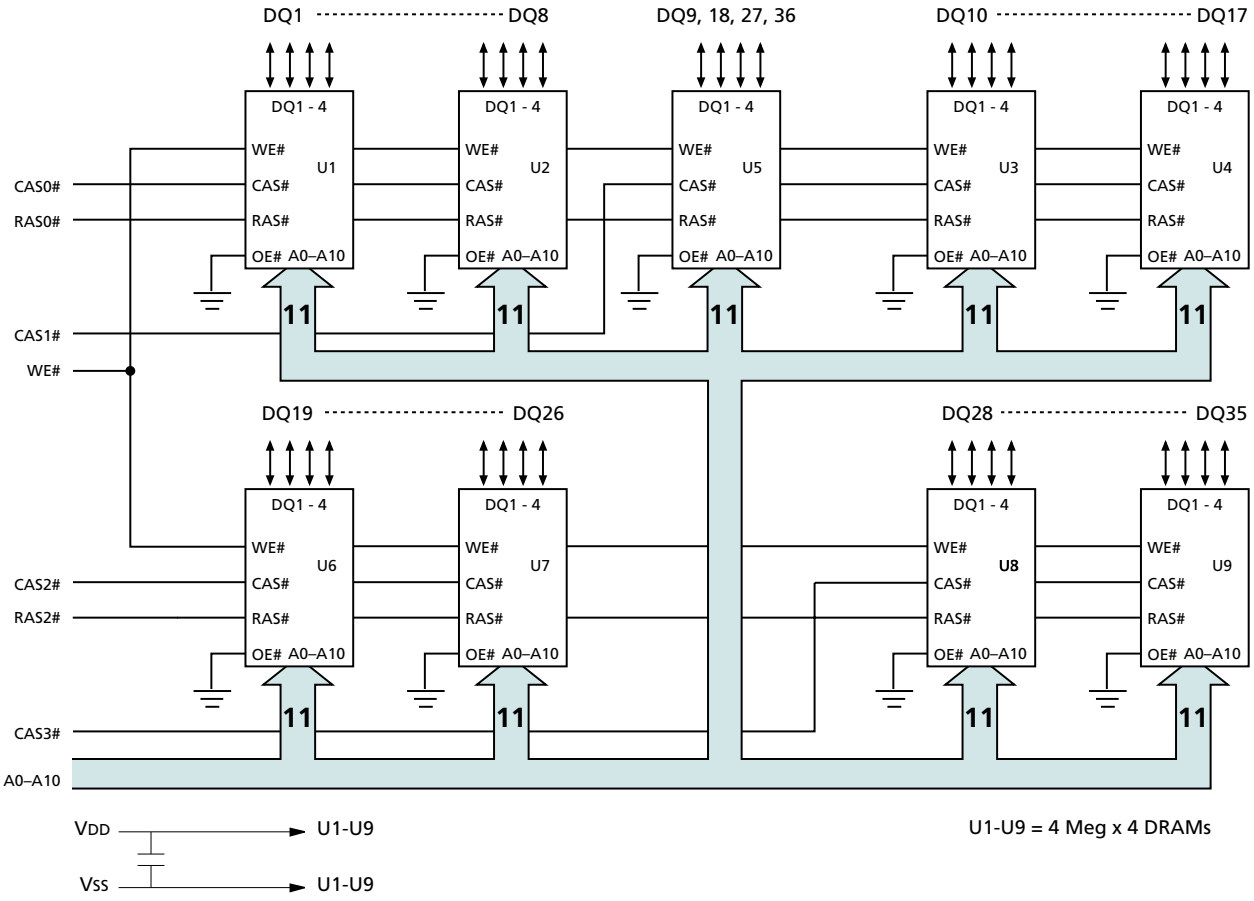
JEDEC-DEFINED PRESENCE-DETECT – MT9D436 (16MB)

SYMBOL	PIN	-6
PRD1	67	Vss
PRD2	68	NC
PRD3	69	NC
PRD4	70	NC

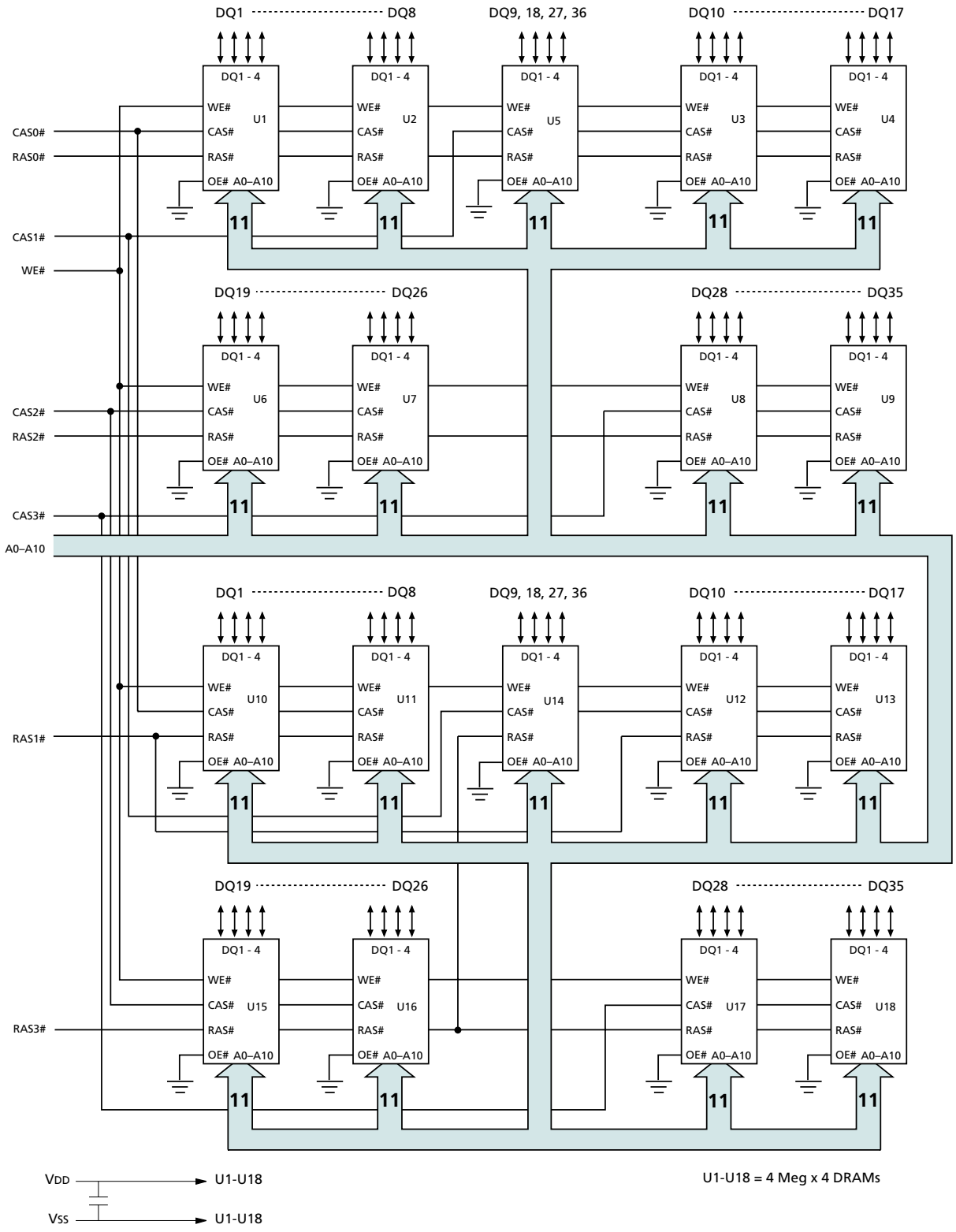
JEDEC-DEFINED PRESENCE-DETECT – MT18D836 (32MB)

SYMBOL	PIN	-6
PRD1	67	NC
PRD2	68	Vss
PRD3	69	NC
PRD4	70	NC

FUNCTIONAL BLOCK DIAGRAM
MT9D436 (16MB)



FUNCTIONAL BLOCK DIAGRAM
MT18D836 (32MB)



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 9W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{DD} = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	4.5	5.5	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2.4	V_{DD} +1	V	
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT:	CAS0#-CAS3#	I_{I1}	-12	12	µA	22
Any input 0V ≤ V_{IN} ≤ 5.5V	A0-A10, WE#	I_{I2}	-36	36	µA	22
(All other pins not under test = 0V)	RAS0#-RAS3#	I_{I3}	-10	10	µA	
OUTPUT LEAKAGE CURRENT: (DQ is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	DQ1-DQ36	I_{OZ}	-10	10	µA	22
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -5mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4.2mA)		V_{OL}	–	0.4	V	

Icc SPECIFICATIONS AND CONDITIONS

(Notes: 1, 5, 6) (V_{DD} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -6	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	16MB 32MB	18 36	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = Other Inputs = V_{DD} - 0.2V)	I_{CC2}	16MB 32MB	5 9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	16MB 32MB	1,170 1,188	mA	3, 21
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	16MB 32MB	900 918	mA	3, 21
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	16MB 32MB	1,170 1,188	mA	3, 21
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	16MB 32MB	1,170 1,188	mA	3, 4

CAPACITANCE

		MAX			
PARAMETER	**SYMBOL**	**16MB**	**32MB**	**UNITS**	**NOTES**
Input Capacitance: A0-A10	C_{I1}	52	105	pF	2
Input Capacitance: WE#	C_{I2}	70	140	pF	2
Input Capacitance: RAS0#-RAS3#	C_{I3}	42	42	pF	2
Input Capacitance: CAS0#-CAS3#	C_{I4}	25	50	pF	2
Input/Output Capacitance: DQ1-DQ36	C_{IO}	10	18	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 5-12) (V_{DD} = +5V ±10%)

AC CHARACTERISTICS		**-6**			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	45		ns	
Column-address setup time	^tASC	0		ns	
Row-address setup time	^tASR	0		ns	
Access time from CAS#	^tCAC		15	ns	
Column-address hold time	^tCAH	10		ns	
CAS# pulse width	^tCAS	15	10,000	ns	
CAS# hold time (CBR Refresh)	^tCHR	10		ns	4
CAS# to output in Low-Z	^tCLZ	3		ns	
CAS# precharge time	^tCP	10		ns	13
Access time from CAS# precharge	^tCPA		35	ns	
CAS# to RAS# precharge time	^tCRP	5		ns	
CAS# hold time	^tCSH	60		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		ns	4
WRITE command to CAS# lead time	^tCWL	15		ns	
Data-in hold time	^tDH	10		ns	18
Data-in setup time	^tDS	0		ns	18
Output buffer turn-off delay	^tOFF	3	15	ns	17
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	15
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	110		ns	
RAS# to CAS# delay time	^tRCD	20		ns	14
READ command hold time (referenced to CAS#)	^tRCH	0		ns	16
READ command setup time	^tRCS	0		ns	
Refresh period (2,048 cycles)	^tREF		32	ms	
RAS# precharge time	^tRP	40		ns	
RAS# to CAS# precharge time	^tRPC	0		ns	

AC ELECTRICAL CHARACTERISTICS

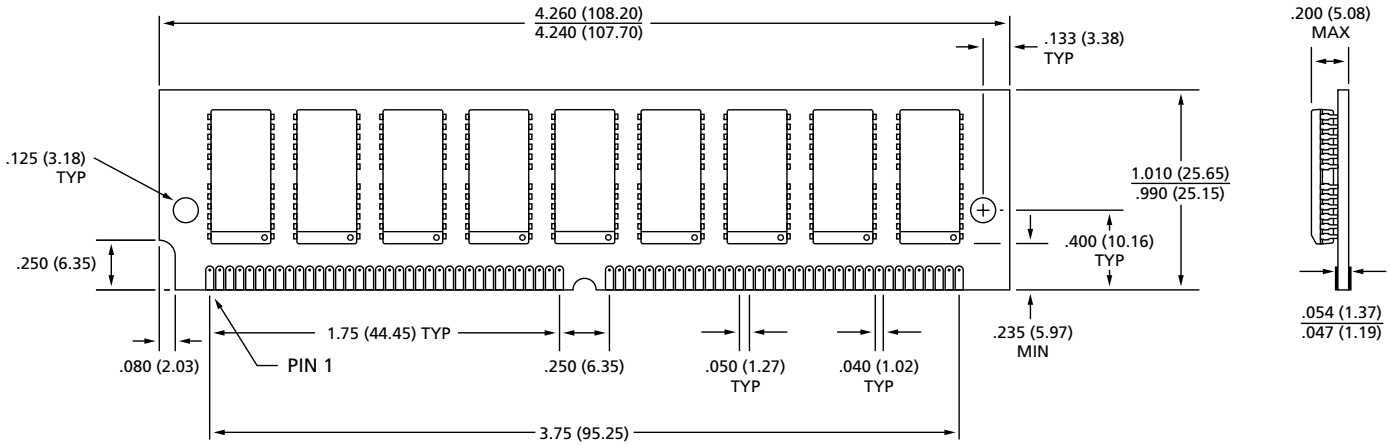
(Notes: 5-12) (V_{DD} = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ command hold time (referenced to RAS#)	^{t}RRH	0		ns	16
RAS# hold time	^{t}RSH	15		ns	
WRITE command to RAS# lead time	^{t}RWL	15		ns	
Transition time (rise or fall)	^{t}T	2	50	ns	
WRITE command hold time	^{t}WCH	10		ns	
WRITE command hold time (referenced to RAS#)	^{t}WCR	45		ns	
WE# command setup time	^{t}WCS	0		ns	
WRITE command pulse width	^{t}WP	10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	10		ns	

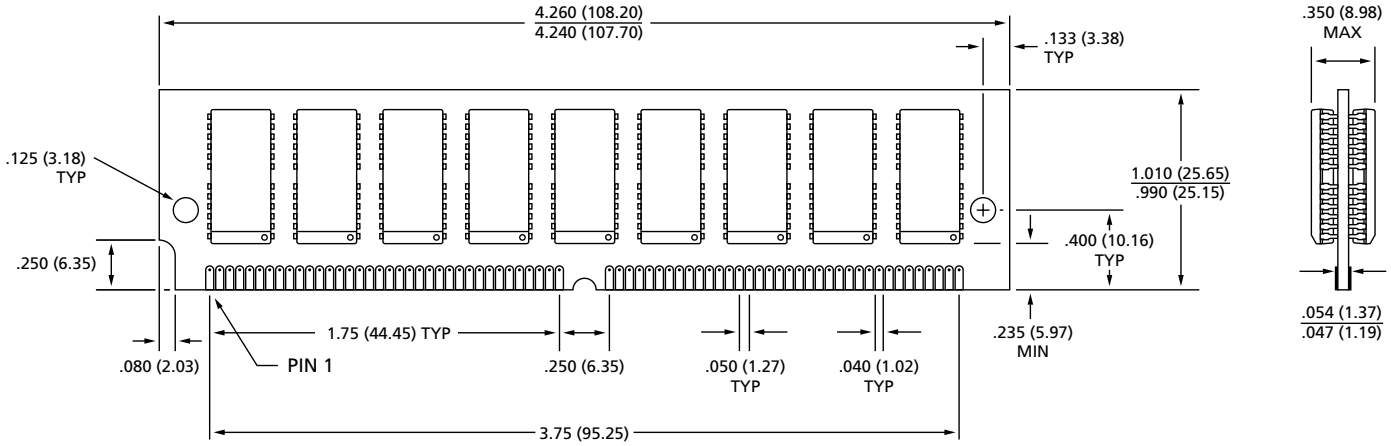
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, V_{DD} = 4.5V, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. Column address changed once each cycle.
22. 16MB module values will be half of those shown.

72-Pin SIMM (16MB)



72-Pin SIMM (32MB)



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