DDR SDRAM DIMM

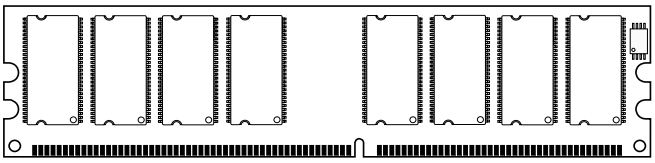
MT8VDDT1664A – 128MB
MT8VDDT3264A – 256MB

For the latest data sheet, please refer to the Micron® Web site: www.micron.com/moduleds

Features

- 184-pin dual in-line memory module (DIMM)
- Fast data transfer rates: PC3200
- CAS Latency 3
- Utilizes 400 MT/s DDR SDRAM components
- 128MB (16 Meg x 64) and 256MB (32 Meg x 64)
- V_{DD}= $V_{DD}Q$= +2.6V
- V_{DDSPD} = +2.3V to +3.6V
- 2.6V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—*i.e.*, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (128MB), 7.8125µs (256MB) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Gold edge connectors

Figure 1: 184-Pin DIMM (MO-206)



OPTIONS	MARKING
• Package	
184-pin DIMM (Standard)	G
184-pin DIMM (Lead-free)	Y
• Memory Clock/Speed, CAS Latency	
5ns (200 MHz), 400 MT/s, CL = 3	-40B

Table 1: Address Table

	128MB	256MB
Refresh Count	4K	8K
Row Addressing	4K (A0–A11)	8K (A0–A12)
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	16 Meg x 8	32 Meg x 8
Column Addressing	1K (A0–A9)	1K (A0–A9)
Module Rank Addressing	1 (S0#)	1 (S0#)

Table 2: Part Numbers and Timing Parameters

PARTNUMBER	MODULE DENSITY	CONFIGURATION	MODULE BANDWITH	MEMORYCLOCK/ DATA RATE	LATENCY (CL - ^{t}RCD - ^{t}RP)
MT8VDDT1664AG-40B__	128MB	16 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT1664AY-40B__	128MB	16 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT3264AG-40B__	256MB	32 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT8VDDT3264AY-40B__	256MB	32 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3

NOTE:

All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8VDDT3264AG-40BA1

Table 3: Pin Assignment (184-Pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VREF	24	DQ17	47	DNU	70	VDD
2	DQ0	25	DQS2	48	A0	71	NC
3	VSS	26	VSS	49	DNU	72	DQ48
4	DQ1	27	A9	50	VSS	73	DQ49
5	DQS0	28	DQ18	51	DNU	74	VSS
6	DQ2	29	A7	52	BA1	75	CK2#
7	VDD	30	VDDQ	53	DQ32	76	CK2
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ
9	NC	32	A5	55	DQ33	78	DQS6
10	NC	33	DQ24	56	DQS4	79	DQ50
11	VSS	34	VSS	57	DQ34	80	DQ51
12	DQ8	35	DQ25	58	VSS	81	VSS
13	DQ9	36	DQS3	59	BA0	82	NC
14	DQS1	37	A4	60	DQ35	83	DQ56
15	VDDQ	38	VDD	61	DQ40	84	DQ57
16	CK1	39	DQ26	62	VDDQ	85	VDD
17	CK1#	40	DQ27	63	WE#	86	DQS7
18	VSS	41	A2	64	DQ41	87	DQ58
19	DQ10	42	VSS	65	CAS#	88	DQ59
20	DQ11	43	A1	66	VSS	89	VSS
21	CKE0	44	DNU	67	DQS5	90	NC
22	VDDQ	45	DNU	68	DQ42	91	SDA
23	DQ16	46	VDD	69	DQ43	92	SCL

Table 4: Pin Assignment (184-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
93	VSS	116	VSS	139	VSS	162	DQ47
94	DQ4	117	DQ21	140	DNU	163	NC
95	DQ5	118	A11	141	A10	164	VDDQ
96	VDDQ	119	DQS11/DM2	142	DNU	165	DQ52
97	DQS9/DM0	120	VDD	143	VDDQ	166	DQ53
98	DQ6	121	DQ22	144	DNU	167	NC
99	DQ7	122	A8	145	VSS	168	VDD
100	VSS	123	DQ23	146	DQ36	169	DQS15/DM6
101	NC	124	VSS	147	DQ37	170	DQ54
102	NC	125	A6	148	VDD	171	DQ55
103	NC	126	DQ28	149	DQS13/DM4	172	VDD
104	VDDQ	127	DQ29	150	DQ38	173	NC
105	DQ12	128	VDDQ	151	DQ39	174	DQ60
106	DQ13	129	DQS12/DM3	152	VSS	175	DQ61
107	DQS10/DM1	130	A3	153	DQ44	176	VSS
108	VDD	131	DQ30	154	RAS#	177	DQS16/DM7
109	DQ14	132	VSS	155	DQ45	178	DQ62
110	DQ15	133	DQ31	156	VDDQ	179	DQ63
111	DNU	134	DNU	157	S0#	180	VDDQ
112	VDDQ	135	DNU	158	DNU	181	SA0
113	NC	136	VDDQ	159	DQS14/DM5	182	SA1
114	DQ20	137	CK0	160	VSS	183	SA2
115	NC/A12	138	CK0#	161	DQ46	184	VDDSPD

NOTE:

Pin 115 is “No Connect” for the 128MB module, or “A12” for the 256MB module.

Figure 2: 184-Pin DIMM Pin Locations

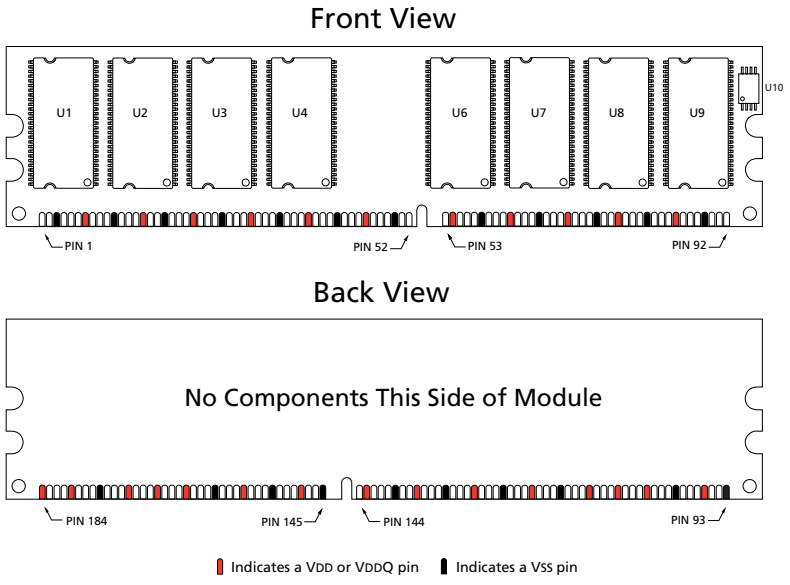


Table 5: Pin Descriptions

Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables on page 2 for more information

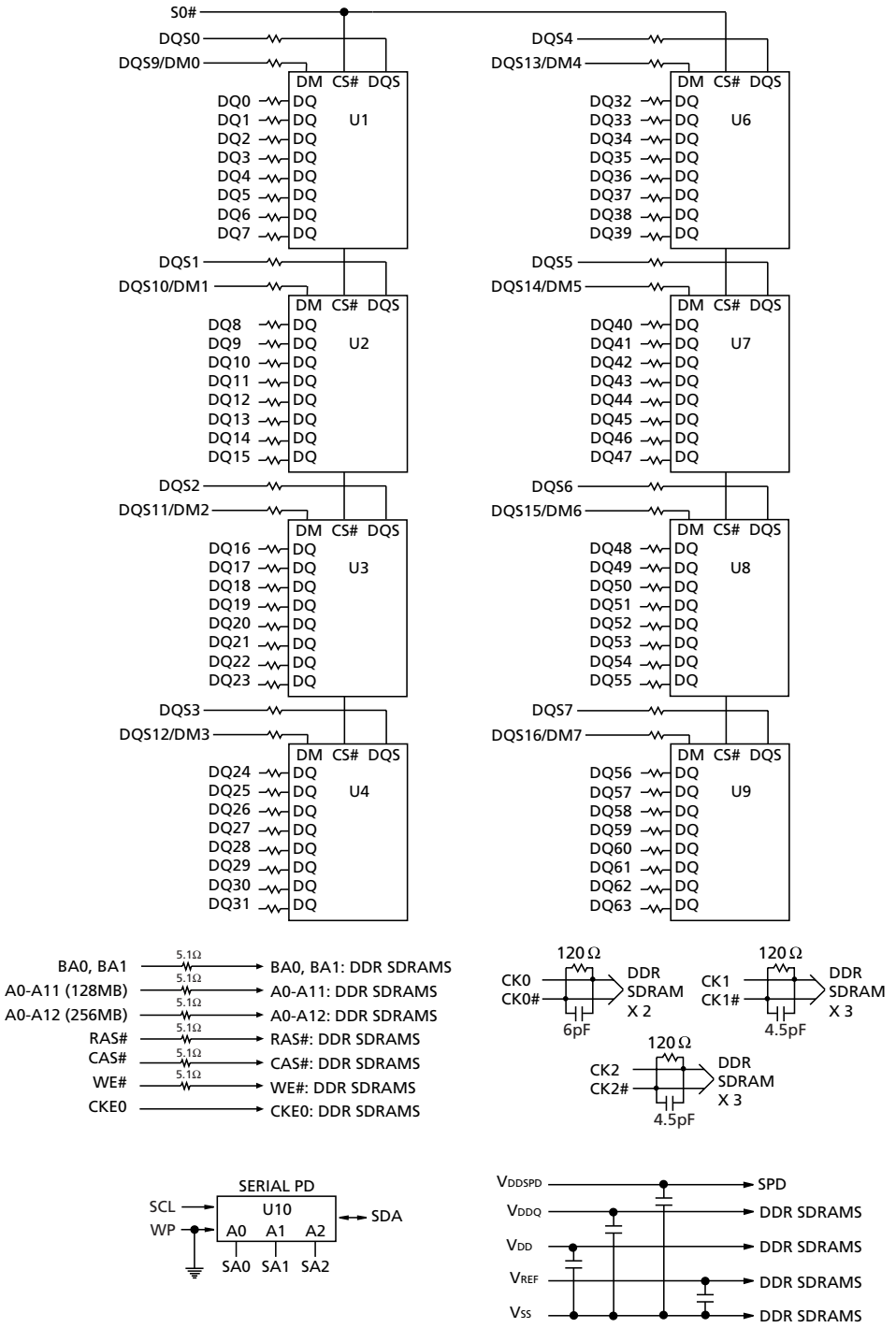
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	V_{REF}	Input	SSTL_2 reference voltage.
63, 65, 154	WE#, CAS#, RAS#	Input	Command Inputs: WE#, RAS#, and CAS# (along with S#) define the command being entered.
16, 17, 75, 76, 137, 138	CK0, CK0#, CK1, CK1#, CK2, CK2#	Input	Clocks: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
21	CKE0	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) internal clock signals, device input buffers, and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWERDOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH. After CKE is brought HIGH, it becomes an SSTL_2 input only.
157	S0#	Input	Chip Select: S# enables (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
52, 59	BA0, BA1	Input	Bank Addresses: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
27, 29, 32, 37, 41, 43, 48, 115 (256MB), 118, 122, 125, 130, 141	A0-A11 128MB A0-A12 256MB	Input	Address Inputs: Sampled during the ACTIVE command (row-address) and READ/WRITE command (column-address, with A10 defining auto precharge) to select one location out of the memory array in the respective device device bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one device bank (A10 LOW) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command.
91	SDA	Input/ Output	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
92	SCL	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
181, 182, 183	SA0-SA2	Input	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
5, 14, 25, 36, 56, 67, 78, 86, 97, 107, 119, 129, 149, 159, 169, 177	DQS0–DQS7, DQS9–DQS16	Input/ Output	Data I/Os: Check bits. ECC, one-bit error detection and correction.

Table 5: Pin Descriptions

Pin numbers may not correlate with symbols. Refer to Pin Assignment Tables on page 2 for more information

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2, 4, 6, 8, 12, 13, 19, 20, 23, 24, 28, 31, 33, 35, 39, 40, 53, 55, 57, 60, 61, 64, 68, 69, 72, 73, 79, 80, 83, 84, 87, 88, 94, 95, 98, 99, 105, 106, 109, 110, 114, 117, 121, 123, 126, 127, 131, 133, 146, 147, 150, 151, 153, 155, 161, 162, 165, 166, 170, 171, 174, 175, 178, 179	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	$V_{DD}Q$	Supply	DQ Power Supply: +2.6V ±0.1V.
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	Supply	Power Supply: +2.6V ±0.1V.
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	Supply	Ground.
184	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V.
9, 10, 71, 82, 90, 101, 102, 103, 113, 115 (128MB), 163, 167, 173	NC	–	No Connect: These pins should be left unconnected.
44, 45, 47, 49, 51, 111, 134, 135, 140, 142, 144, 158	DNU	–	Do Not Use: These pins are not connected on this module but are assigned pins on other modules in this product family.

Figure 3: Functional Block Diagram



NOTE:

1. All resistor values are 22Ω unless otherwise specified.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

MT46V16M8TG = DDR SDRAMs, 128MB Modules
MT46V32M8TG = DDR SDRAMs, 256MB Modules

General Description

The MT8VDDT1664A and MT8VDDT3264A are high-speed CMOS, dynamic random-access, 128MB and 256MB memory modules organized in a x64 configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. Double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from multiple differential clocks (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select devices bank; A0–A11 select device row for the 128MB module, A0–A12 select device row for the 256MB module). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

DDR SDRAM modules provide for programmable read or write burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All outputs are SSTL_2, Class II compatible. For more information regarding DDR SDRAM operation, refer to the 128Mb and 256Mb DDR SDRAM data sheets.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Mode Register Definition

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 4, Mode Register Definition Diagram, on page 7. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A11 (for the 128MB module) or A7–A12 (for the 256MB module) specify the operating mode.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6, Burst Definition Table, on page 8.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A9 when the burst length is set to two, by A2–A9 when the burst length is set to four and by A3–A9 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 3, 2.5, or 2 clocks, as shown in Figure 5, CAS Latency Diagram.

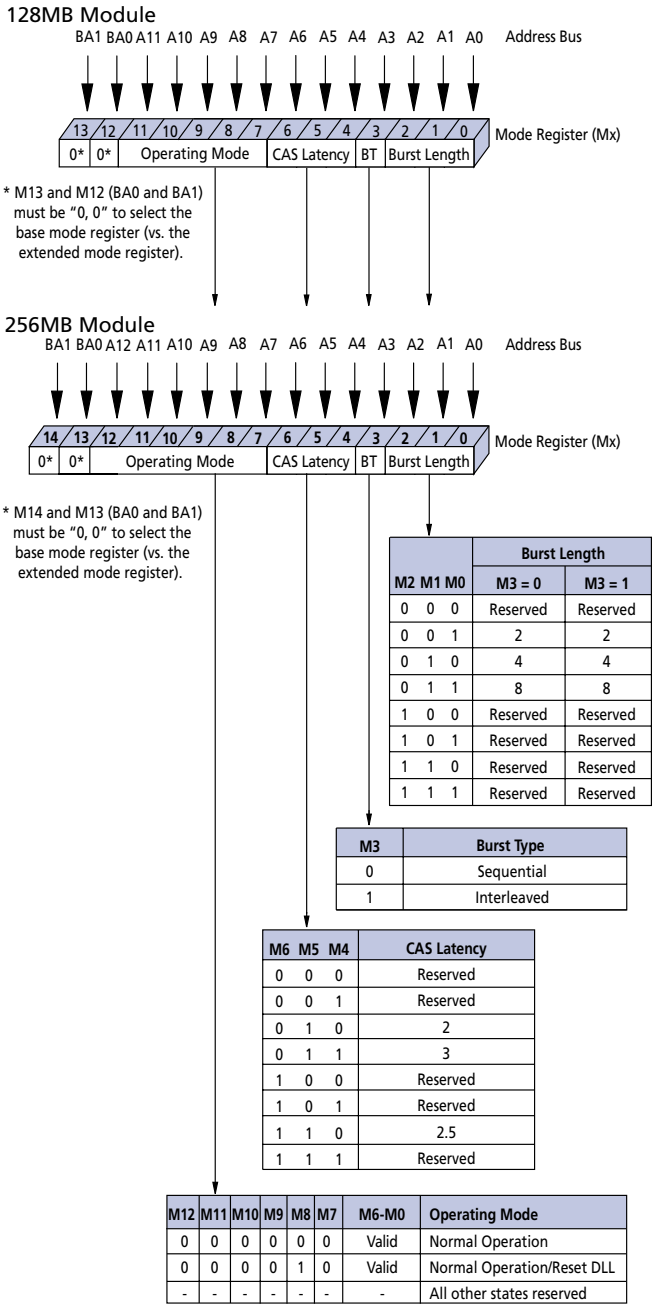
If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table Table 7:, CAS Latency (CL) Table, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7–A11 (for the 128MB module), or A7–A12 (for the 256MB module) each set to zero, and bits A0–A6 set to the desired values.

Figure 4: Mode Register Definition Diagram



	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	Reserved	Reserved
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	2.5
1 1 1	Reserved

M12	M11	M10	M9	M8	M7	M6-M0	Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
0	0	0	0	1	0	Valid	Normal Operation/Reset DLL
-	-	-	-	-	-	-	All other states reserved

Table 6: Burst Definition Table

BURST LENGTH	STARTING COLUMN ADDRESS			ORDER OF ACCESSES WITHIN A BURST	
				TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

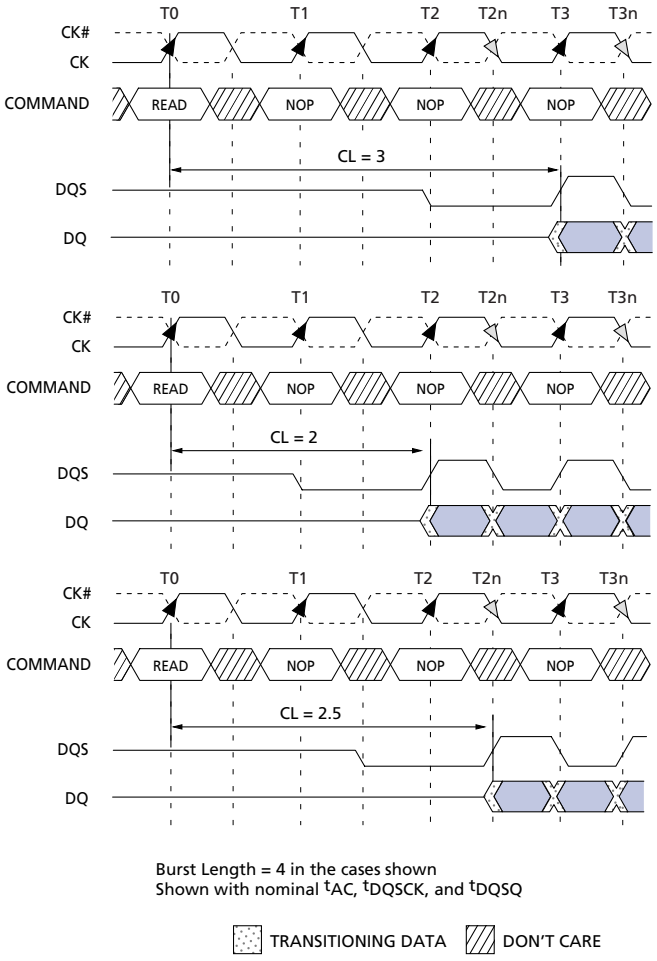
NOTE:

1. For a burst length of two, A1–A9 select the two-data-element block; A0 selects the first access within the block.
2. For a burst length of four, A2–A9 select the four-data-element block; A0–A1 select the first access within the block.
3. For a burst length of eight, A3–A9 select the eight-data-element block; A0–A2 select the first access within the block.
4. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

Table 7: CAS Latency (CL) Table

	ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ)		
SPEED	CL = 2	CL = 2.5	CL = 3
-40B	75 ≤ f ≤ 133	75 ≤ f ≤ 167	125 ≤ f ≤ 200

Figure 5: CAS Latency Diagram



A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9–A11 (for 128MB module), or A7 and A9–A12 (for 256MB module) each set to zero, bit A8 set to one, and bits A0–A6 set to the desired values.

Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7–A11, or A7–A12, are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

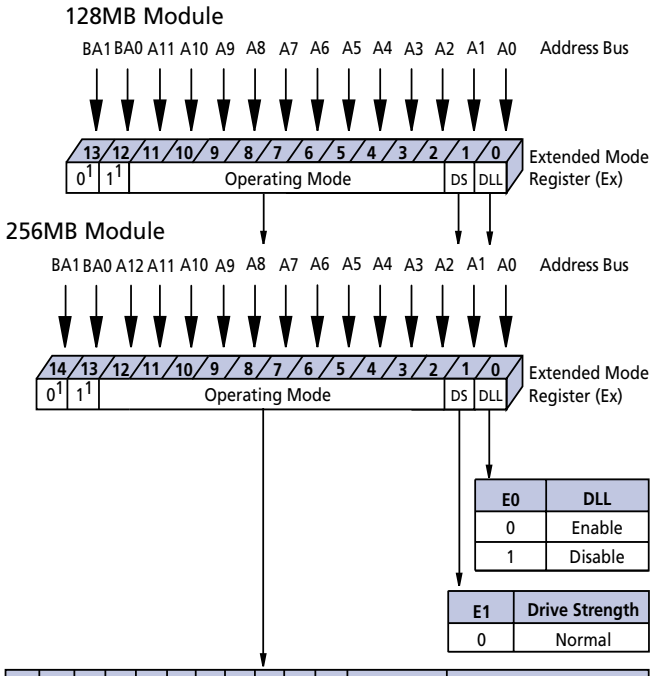
The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 6, Extended Mode Register Definition Diagram. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both low) to reset the DLL.

The extended mode register must be loaded when all device banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Figure 6: Extended Mode Register Definition Diagram



E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2[2]	E1, E0	Operating Mode
0	0	0	0	0	0	0	0	0	0	0	Valid	Reserved
–	–	–	–	–	–	–	–	–	–	–	–	Reserved

NOTE:

1. E13 and E12 (128MB module), or E14 and E13 (256MB Module) (BA1 and BA0) must be "0, 1" to select the Extended Mode Register (vs. the base Mode Register).
2. The QFC# option is not supported.

Commands

The Truth Tables below provide a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb and 256Mb DDR SDRAM data sheets.

Table 8: Truth Table – Commands

CKE is HIGH for all commands shown except SELF REFRESH

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	1
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	2
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	3
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	3
BURST TERMINATE	L	H	H	L	X	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	8

NOTE:

1. DESELECT and NOP are functionally interchangeable.
2. BA0–BA1 provide device bank address and A0–A11 (128MB) or A0–A12 (256MB) provide device row address.
3. BA0–BA1 provide device bank address; A0–A9 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
4. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for read bursts with auto precharge enabled and for write bursts.
5. A10 LOW: BA0–BA1 determine which device bank is precharged. A10 HIGH: all device banks are precharged and BA0–BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls device row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. BA0–BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A11 (for 128MB module) or A0–A12 (for 256MB module) provide the op-code to be written to the selected mode register.

Table 9: Truth Table DM Operation

Used to mask write data; provided coincident with the corresponding data

NAME (FUNCTION)	DM	DQ
WRITE Enable	L	Valid
WRITE Inhibit	H	X

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on VDD Supply
Relative to VSS -1V to +3.6V
Voltage on VDDQ Supply
Relative to VSS -1V to +3.6V
Voltage on VREF and Inputs
Relative to VSS -1V to +3.6V
Voltage on I/O Pins
Relative to VSS -0.5V to VDDQ +0.5V

Operating Temperature
TA (ambient)0°C to +70°C
Storage Temperature (plastic) . . . . . -55°C to +150°C
Power Dissipation 8W
Short Circuit Output Current. 50mA

Table 10: DC Electrical Characteristics and Operating Conditions

Notes: 1–5, 14; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		VDD	2.5	2.7	V	32, 36, 47
I/O Supply Voltage		VDDQ	2.5	2.7	V	32, 36, 39, 47
I/O Reference Voltage		VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 39
I/O Termination Voltage (system)		VTT	VREF - 0.04	VREF + 0.04	V	7, 39
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.15	VDD + 0.3	V	25
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.15	V	25
INPUT LEAKAGE CURRENT Any Input 0V ≤ VIN ≤ VDD, VREF Pin 0V ≤ VIN ≤ 1.35V (All other pins not under test = 0V)	Command/ Address, S#, CKE	II	-16	16	µA	46
	CK1, CK1#, CK2, CK2#		-6	6		
	CK0, CK0#		-4	4		
	DM		-2	2		
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ VOUT ≤ VDDQ)	DQ, DQS	IOZ	-5	5	µA	46
OUTPUT LEVELS: High Current (VOUT = VDDQ-0.373V, minimum VREF, minimum VTT)		IOH	-16.8	–	mA	33, 34
Low Current (VOUT = 0.373V, maximum VREF, maximum VTT)		IOL	16.8	–	mA	

Table 11: AC Input Operating Conditions

Notes: 1–5, 14; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(AC)	VREF + 0.310	–	V	12, 25, 35
Input Low (Logic 0) Voltage	VIL(AC)	–	VREF - 0.310	V	12, 25, 35
I/O Reference Voltage	VREF(AC)	0.49 x VDDQ	0.51 x VDDQ	V	6

Table 12: IDD Specifications and Conditions (128MB)

DDR SDRAM components only

Notes: 1–5, 8, 10, 12; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

			MAX		
PARAMETER/CONDITION		SYM	-40B	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	920	mA	20, 41
OPERATING CURRENT: One device bank; Active-Read-Pre-charge; Burst = 4; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,080	mA	20, 41
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD2P	24	mA	21, 28, 43
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	400	mA	44
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	200	mA	21, 28, 43
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	400	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,080	mA	20, 41
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,240	mA	20
AUTO REFRESH CURRENT	tRC = tRFC (MIN)	IDD5	1,920	mA	43
	tRC = 15.625µs	IDD5A	48	mA	24, 43
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	32	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL= 4) with auto precharge,tRC = minimum tRC allowed; tCK = tCK (MIN); Address and control inputs change only during Active, READ, or WRITE commands		IDD7	2,840	mA	20, 42

Table 13: IDD Specifications and Conditions (256MB)

DDR SDRAM components only

Notes: 1–5, 8, 10, 12; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

			MAX		
PARAMETER/CONDITION		SYM	-40B	UNITS	NOTES
OPERATING CURRENT: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	1,080	mA	20, 41
OPERATING CURRENT: One device bank; Active-Read-Pre-charge; Burst = 4; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,360	mA	20, 41
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD2P	32	mA	21, 28, 43
IDLE STANDBY CURRENT: CS# = HIGH; All device banks idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	480	mA	44
ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	320	mA	21, 28, 43
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	560	mA	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,600	mA	20, 41
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,480	mA	20
AUTO REFRESH CURRENT	tRC = tRFC (MIN)	IDD5	2,080	mA	20, 43
	tRC = 15.625µs	IDD5A	48	mA	24, 43
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD6	32	mA	9
OPERATING CURRENT: Four device bank interleaving READs (BL= 4) with auto precharge,tRC = minimum tRC allowed; tCK = tCK (MIN); Address and control inputs change only during Active, READ, or WRITE commands		IDD7	3,760	mA	20, 42

Table 14: Capacitance

Note: 11; notes appear on pages 16–18

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	CIO	4.0	5.0	pF
Input Capacitance: Command and Address, S#	CI1	16.0	24.0	pF
Input Capacitance: CK0, CK0#	CI2	10.0	12.0	pF
Input Capacitance: CK1, CK1#; CK2, CK2#	CI3	10.5	13.5	pF
Input Capacitance: CKE	CI4	16.0	24.0	pF

Table 15: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–5, 8, 12–15, 29, 31; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.6V ±0.1V

AC CHARACTERISTICS			-40B			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access window of DQs from CK/CK#		^tAC	-0.7	+0.7	ns	
CK high-level width		^tCH	0.45	0.55	^tCK	26
CK low-level width		^tCL	0.45	0.55	^tCK	26
Clock cycle time	CL= 3	^tCK (3)	5	7.5	ns	41, 46
	CL= 2.5	^tCK (2.5)	6	13	ns	41, 46
	CL= 2	^tCK (2)	7.5	13	ns	41, 46
DQ and DM input hold time relative to DQS		^tDH	0.4		ns	23, 27
DQ and DM input setup time relative to DQS		^tDS	0.4		ns	23, 27
DQ and DM input pulse width (for each input)		^tDIPW	1.75		ns	27
Access window of DQS from CK/CK#		^tDQSCK	-0.6	+0.6	ns	
DQS input high pulse width		^tDQSH	0.35		^tCK	
DQS input low pulse width		^tDQSL	0.35		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.40	ns	22, 23
Write command to first DQS latching transition		^tDQSS	0.72	1.28	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.2		^tCK	
Half clock period		^tHP	^tCH,^tCL		ns	30
Data-out high-impedance window from CK/CK#		^tHZ		+0.70	ns	16, 38
Data-out low-impedance window from CK/CK#		^tLZ	-0.70		ns	16, 39
Address and control input hold time (1 V/ns)		^tIH_F	0.6		ns	12
Address and control input setup time (1 V/ns)		^tIS_F	0.6		ns	12
Address and control input hold time (0.5 V/ns)		^tIH_S	0.6		ns	12
Address and control input setup time (0.5 V/ns)		^tIS_S	0.6		ns	12
LOAD MODE REGISTER command cycle time		^tMRD	2		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS		ns	22, 23
Data hold skew factor		^tQHS		0.50	ns	
ACTIVE to PRECHARGE command		^tRAS	40	70,000	ns	31
ACTIVE to READ with Auto precharge command		^tRAP	15		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	55		ns	
AUTO REFRESH command period		^tRFC	70		ns	44
ACTIVE to READ or WRITE delay		^tRCD	15		ns	
PRECHARGE command period		^tRP	15		ns	
DQS read preamble		^tRPRE	0.9	1.1	^tCK	38
DQS read postamble		^tRPST	0.4	0.6	^tCK	
ACTIVE bank a to ACTIVE bank b command		^tRRD	10		ns	

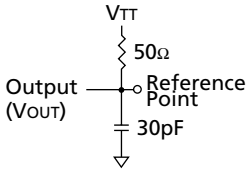
Table 15: DDR SDRAM Component Electrical Characteristics and Recommended AC Operating Conditions (Continued)

Notes: 1–5, 8, 12–15, 29, 31; notes appear on pages 16–18; 0°C ≤ T_A ≤ +70°C; VDD = VDDQ = +2.6V ±0.1V

AC CHARACTERISTICS		-40B			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
DQS write preamble	^{t}WPRE	0.25		^{t}CK	
DQS write preamble setup time	^{t}WPRES	0		ns	18, 19
DQS write postamble	^{t}WPST	0.4	0.6	^{t}CK	17
Write recovery time	^{t}WR	15		ns	
Internal WRITE to READ command delay	^{t}WTR	2		^{t}CK	
Data valid output window	na	^{t}QH - ^{t}DQSQ		ns	22
REFRESH to REFRESH command interval 128MB	^{t}REFC		140.6	µs	21
REFRESH to REFRESH command interval 256MB	^{t}REFC		70.3	µs	21
Average periodic refresh interval 128MB	^{t}REFI		15.6	µs	21
Average periodic refresh interval 256MB	^{t}REFI		7.8	µs	21
Terminating voltage delay to VDD	^{t}VTD	0		ns	
Exit SELF REFRESH to non-READ command	^{t}XSNR	75		ns	
Exit SELF REFRESH to READ command	^{t}XSRD	200		^{t}CK	

Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, Idd, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to Vref (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. V_{REF} is expected to equal VddQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on $_{Vref}$ may not exceed ±2 percent of the DC value. Thus, from $V_{DD}Q/2$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
7. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
8. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 3 for -40B with the outputs open.
9. Enables on-chip refresh and address counters.
10. I_{DD} specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
11. This parameter is sampled. V_{DD} = +2.6V ±0.1V, $V_{DD}Q$ = +2.6V ±0.1V, V_{REF} = Vss, f = 200 MHz, T_A = 25°C, $V_{OUT}(DC) = V_{DD}Q/2$, V_{OUT} (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
12. Slew rates less than 0.5V/ ns are not allowed. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
13. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
14. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before Vref stabilizes, CKE ≤ 0.3 x $V_{DD}Q$ is recognized as LOW.
15. The output timing reference level, as measured at the timing reference point indicated in Note 3, is V_{TT}.
16. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
17. If DQS transitions to HIGH above V_{IH} (DC) MIN, then it must not transition to LOW below V_{IH}(DC) MIN prior to $^{t}DQSH$ (MIN).
18. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
19. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}DQSS$.
20. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
21. The refresh period 64ms. This equates to an average refresh rate of 15.625µs (128MB modules), or 7.821µs (256MB modules). However, an AUTO REFRESH command must be asserted at least once every 140.6µs (128MB modules) or 70.3µs (256MB modules); burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
22. The valid data window is derived by achieving other specifications: ^{t}HP ($^{t}CK/2$), $^{t}DQSQ$, and ^{t}QH ($^{t}QH = {}^{t}HP - {}^{t}QHS$). The data valid window derates in direct proportion to the clock duty cycle and a

practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.

23. Each byte lane has a corresponding DQS.
24. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (i.e., during standby).
25. To maintain a valid level, the transitioning edge of the input must:
    a) Sustain a constant slew rate from the current AC level through to the target AC level, V_{IL}(AC) or V_{IH}(AC).
    b) Reach at least the target AC level.
    c) After the AC target level is reached, continue to maintain at least the target DC level, V_{IL}(DC) or V_{IH}(DC).
26. JEDEC specifies CK and CK# input slew rate must be ≤ 1V/ns (2V/ns differentially).
27. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate less than 0.5V/ns is not allowed. If slew rate exceeds 4V/ns, functionality is uncertain.
28. V_{DD} must not vary more than 4 percent if CKE is not active while any bank is active.
29. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
30. ^{t}HP min is the lesser of ^{t}CL minimum and ^{t}CH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.
31. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS(min) can be satisfied prior to the internal precharge command being issued.
32. Any positive glitch in the nominal voltage must be less than 1/3 of the clock and not more than +400mV or 2.9V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.4V, whichever is more positive. However, the DC average cannot be below +2.5V minimum.
33. Normal Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 7, Pull-Down Characteristics.
    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 7, Pull-Down Characteristics.
    c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 8, Pull-Up Characteristics.
    d) The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 8, Pull-Up Characteristics.
    e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
    f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10 percent, for device drain-to-source voltages from 0.1V to 1.0V.

Figure 7: Pull-Down Characteristics

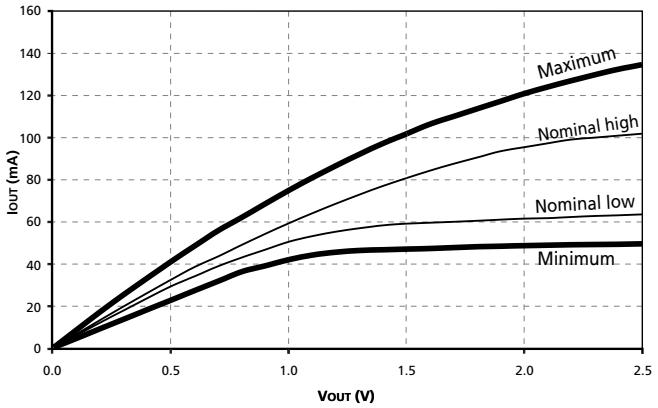
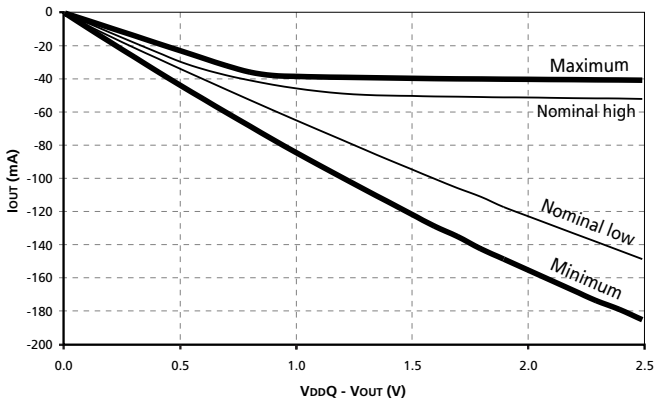


Figure 8: Pull-Up Characteristics



34. The voltage levels used are derived from a minimum Vdd level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
35. VIH overshoot: $V_{IH(MAX)}$ = $V_{DD}Q$ + 1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: $V_{IL(MIN)}$ = -1.5V for a pulse width ≤ 3ns and the pulse width can not be greater than 1/3 of the cycle rate.
36. V_{DD} and $V_{DD}Q$ must track each other.
37. This maximum value is derived from the referenced test load. In practice, the values obtained in a typical terminated design may reflect up to 310ps less for ^{t}HZ (MAX) and the last DVW. ^{t}HZ (MAX) will prevail over ^{t}DQSCK MAX) + ^{t}RPST (MAX) condition. ^{t}LZ(MIN) will prevail over ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition.
38. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
39. During initialization, $V_{DD}Q$, V_{TT}, and Vref must be equal to or less than V_{DD} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power up, even if $V_{DD}/V_{DD}Q$ are 0V, provided a minimum of 42Ω of series resistance is used between the V_{TT} supply and the input pin.
40. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
41. Random addressing changing and 50 percent of data changing at every transfer.
42. Random addressing changing and 100 percent of data changing at every transfer.
43. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}REF later.
44. I_{DD2N} specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to I_{DD2F} except I_{DD2Q} specifies the address and control inputs to remain stable. Although I_{DD2F}, I_{DD2N}, and I_{DD2Q} are similar, I_{DD2F} is "worst case."
45. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.
46. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
47. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz. Any noise above 20MHz at the DRAM generated from any source other than the DRAM istelf may not exceed the DC voltage range of +2.6V ±0.1V.

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 9, Data Validity, and Figure 10, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 11, Acknowledge Response From Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 9: Data Validity

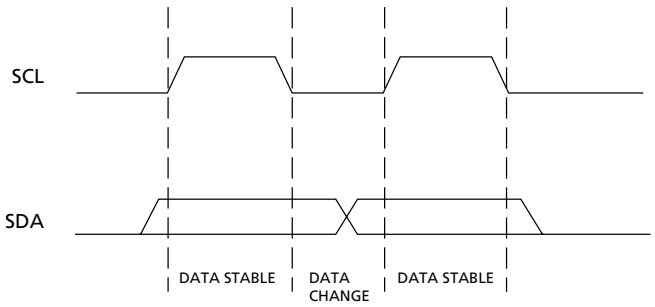


Figure 10: Definition of Start and Stop

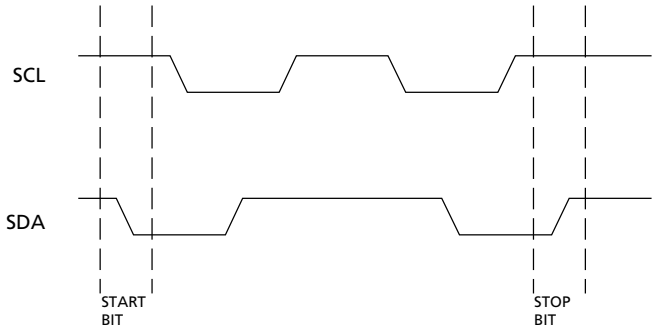


Figure 11: Acknowledge Response From Receiver

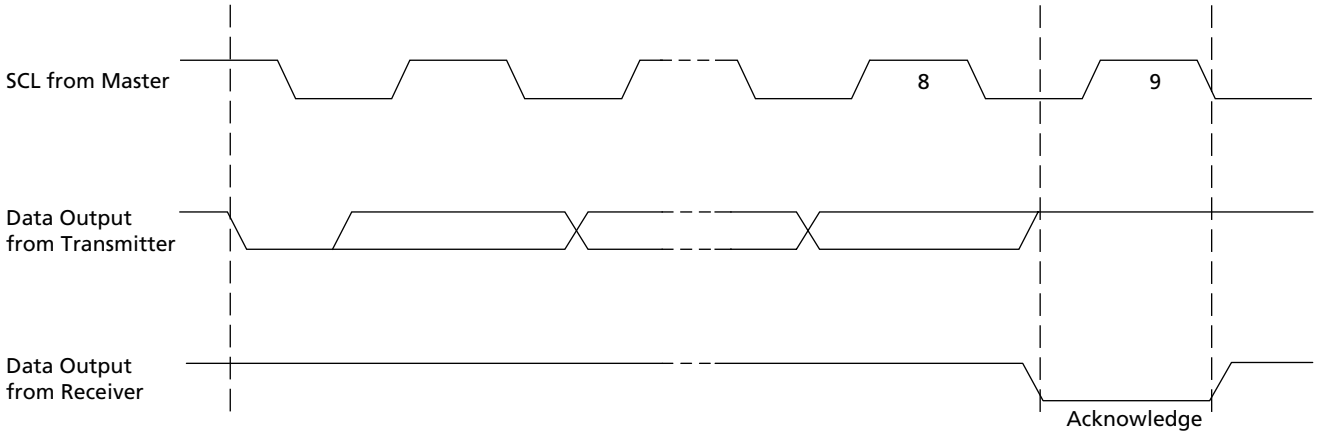


Table 16: EEPROM Device Select Code

Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 17: EEPROM Operating Modes

MODE	RW BIT	WC	BYTES	INITIAL SEQUENCE
Current Address Read	1	VIH or VIL	1	START, Device Select, RW = "1"
Random Address Read	0	VIH or VIL	1	START, Device Select, RW = "0", Address
	1	VIH or VIL	1	reSTART, Device Select, RW = "1"
Sequential Read	1	VIH or VIL	≥ 1	Similar to Current or Random Address Read
Byte Write	0	VIL	1	START, Device Select, RW = "0"
Page Write	0	VIL	≤ 16	START, Device Select, RW = "0"

Figure 12: SPD EEPROM Timing Diagram

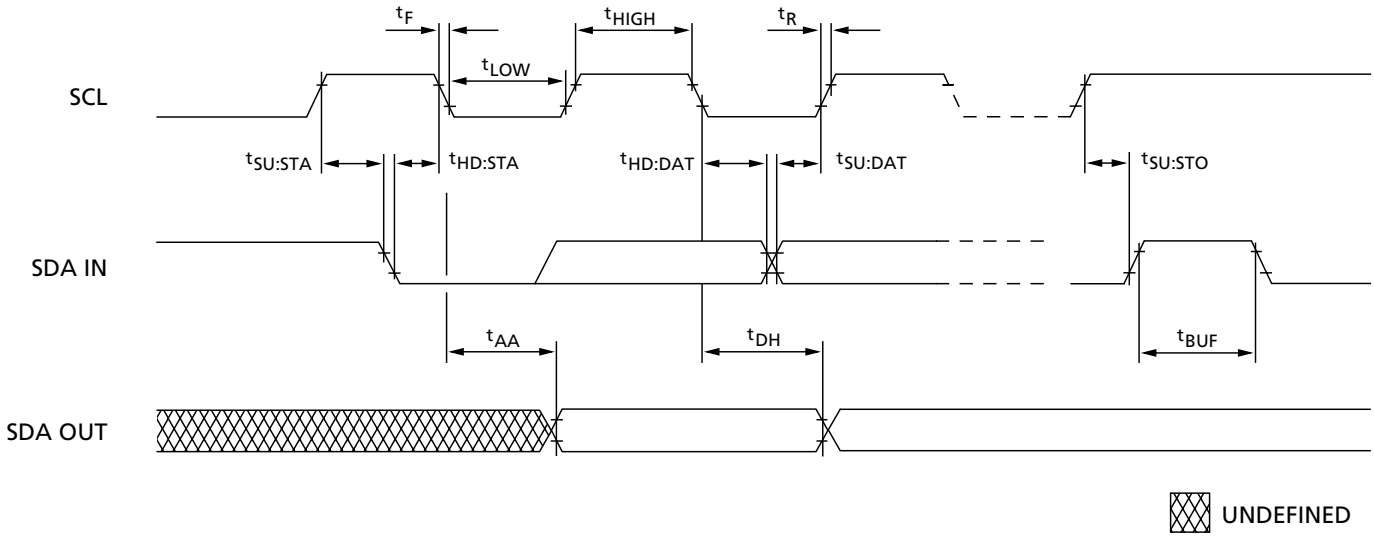


Table 18: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DDSPD}	2.3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DDSPD} \times 0.7$	V_{DDSPD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DDSPD} \times 0.3$	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{DD} or V_{SS}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

Table 19: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V TO +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

NOTE:

1. To aviod spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 20: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

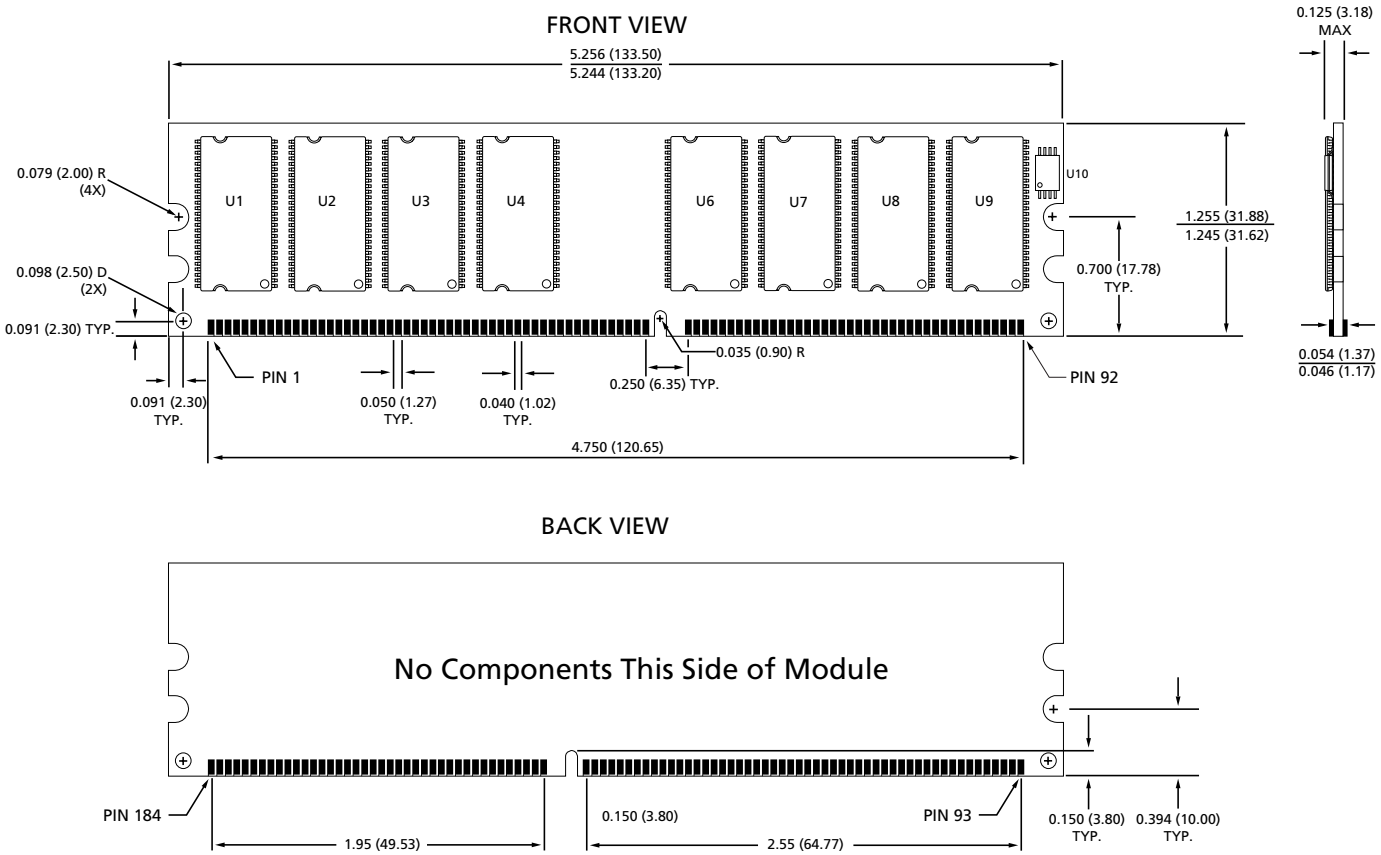
BYTE	DESCRIPTION	ENTRY(VERSION)	MT8VDDT1664A	MT8VDDT3264A
0	Number of SPD Bytes Used by Micron	128	80	80
1	Total Number of Bytes in SPD Device	256	08	08
2	Fundamental Memory Type	SDRAM DDR	07	07
3	Number of Row Addresses on Assembly	12, 13	0C	0D
4	Number of Column Addresses on Assembly	10	0A	0A
5	Number of Physical Ranks on DIMM	1	01	01
6	Module Data Width	64	40	40
7	Module Data Width (Continued)	0	00	00
8	Module Voltage Interface Levels	SSTL 2.5V	04	04
9	SDRAM Cycle Time, (^{t}CK) (CAS Latency = 3)	5ns (-40B)	50	50
10	SDRAM Access From Clock,(^{t}AC) (CAS Latency = 3)	0.7ns (-40B)	70	70
11	Module Configuration Type	None	00	00
12	Refresh Rate/Type	15.62µs, 7.8µs/SELF	80	82
13	SDRAM Device Width (Primary DDR SDRAM)	8	08	08
14	Error-Checking DDR SDRAM Data Width	None	00	00
15	Minimum Clock Delay, Back-to-Back Random Column Access	1 clock	01	01
16	Burst Lengths Supported	2, 4, 8	0E	0E
17	Number of Banks on DDR SDRAM Device	4	04	04
18	CAS Latencies Supported	3, 2.5, 2	1C	1C
19	CS Latency	0	01	01
20	WE Latency	1	02	02
21	SDRAM Module Attributes	Unbuffered/Diff. Clock	20	20
22	SDRAM Device Attributes: General	Fast/Concurrent AP	C0	C0
23	SDRAM Cycle Time, (^{t}CK) CAS Latency = 2.5	6ns (for PC2700 system compatibility)	60	60
24	SDRAM Access From CK, (^{t}AC) CAS Latency = 2.5	0.7ns (for PC 2700 system compatibility)	70	70
25	SDRAM Cycle Time, (^{t}CK) CAS Latency =2	7.5ns (for PC 2100 and PC 1600 system compatibility)	75	75
26	SDRAM Access From CK , (^{t}AC) CAS Latency = 2	0.75ns (for PC 2100 and PC 1600 system compatibility)	75	75
27	Minimum Row Precharge Time, (^{t}RP)	15ns (-40B)	3C	3C
28	Minimum Row Active to Row Active, (^{t}RRD)	10ns (-40B)	28	28
29	Minimum Ras# to CAS# Delay, (^{t}RCD)	15ns (-40B)	3C	3C
30	Minimum RAS# Pulse Width, (^{t}RAS)	40ns (-40B)	28	28
31	Module Rank Density	128MB, 256MB	20	40
32	Address and Command Setup Time, (^{t}IS)	0.6ns (-40B)	60	60
33	Address and Command Hold Time, (^{t}IH)	0.6ns (-40B)	60	60

Table 20: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY(VERSION)	MT8VDDT1664A	MT8VDDT3264A
34	Data/Data Mask Input Setup Time, (^{t}DS)	0.4ns (-40B)	40	40
35	Data/Data Mask Input Hold Time, (^{t}DH)	0.4ns (-40B)	40	40
36-40	Reserved		00	00
41	Min Active Auto Refresh Time (^{t}RC)	55ns (-40B)	37	37
42	Minimum Auto Refresh to Active/ Auto Refresh Command Period, (^{t}RFC)	70ns (-40B)	46	46
43	SDRAM Device Max Cycle Time (^{t}CK$_{MAX}$)	12ns (-40B)	30	30
44	SDRAM Device Max DQS-DQ Skew Time (^{t}DQSQ)	0.4ns (-40B)	28	28
45	SDRAM Device Max Read Data Hold Skew Factor (^{t}QHS)	0.5ns (-40B)	50	50
46	Reserved		00	00
47	DIMM Height		01	01
48–61	Reserved		00	00
62	SPD Revision	Release 1.1	11	11
63	Checksum For Bytes 0-62	-40B	5D	80
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC ID Code	(Continued)	FF	FF
72	Manufacturing Location	01–12	01–0C	01–0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1-9	01-09	01-09
92	Identification Code (Continued)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-specific Data (RSVD)		–	–

Figure 13: 184-Pin DIMM Dimensions



NOTE:

All dimensions in inches (millimeters) with $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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