

**FEATURES**

- On-chip clock ÷4 and ÷8
- Extended 100E VEE range of -4.2V to -5.5V
- 1.6Gb/s typical data rate capability
- Differential clock and serial inputs
- VBB output for single-ended use
- Asynchronous data synchronization
- Mode select to expand to 8 bits
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E446
- Available in 28-pin PLCC package

**DESCRIPTION**

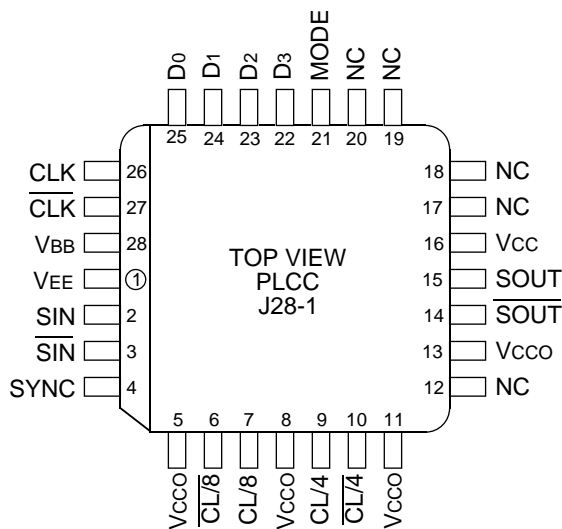
The SY10/100E446 are integrated 4-bit parallel-to-serial data converters. These devices are designed to operate for NRZ data rates of up to a minimum of 1.3Gb/s. The chips generate a divide-by-4 and a divide-by-8 clock for both 4-bit conversion and a two-chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D0 to D3. A serial input is provided to cascade two E446 devices for 8-bit conversion applications.

The SYNC input will asynchronously reset the internal clock circuitry. This pin allows the user to reset the internal clock conversion unit and, thus, select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW (or open) the device will function as a 4-bit converter. When the mode input is driven HIGH, the internal load clock will change on every eighth clock cycle, thus allowing for an 8-bit conversion scheme using two E446s. When cascaded in an 8-bit conversion scheme, the devices will not operate at the 1.3Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E446.

For lower data rate applications, a VBB reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz, differential input signals are recommended. For single-ended inputs, the VBB pin is tied to the inverting differential input and bypassed via a 0.01μF capacitor. The VBB provides the switching reference for the input differential amplifier. The VBB can also be used to AC couple an input signal.

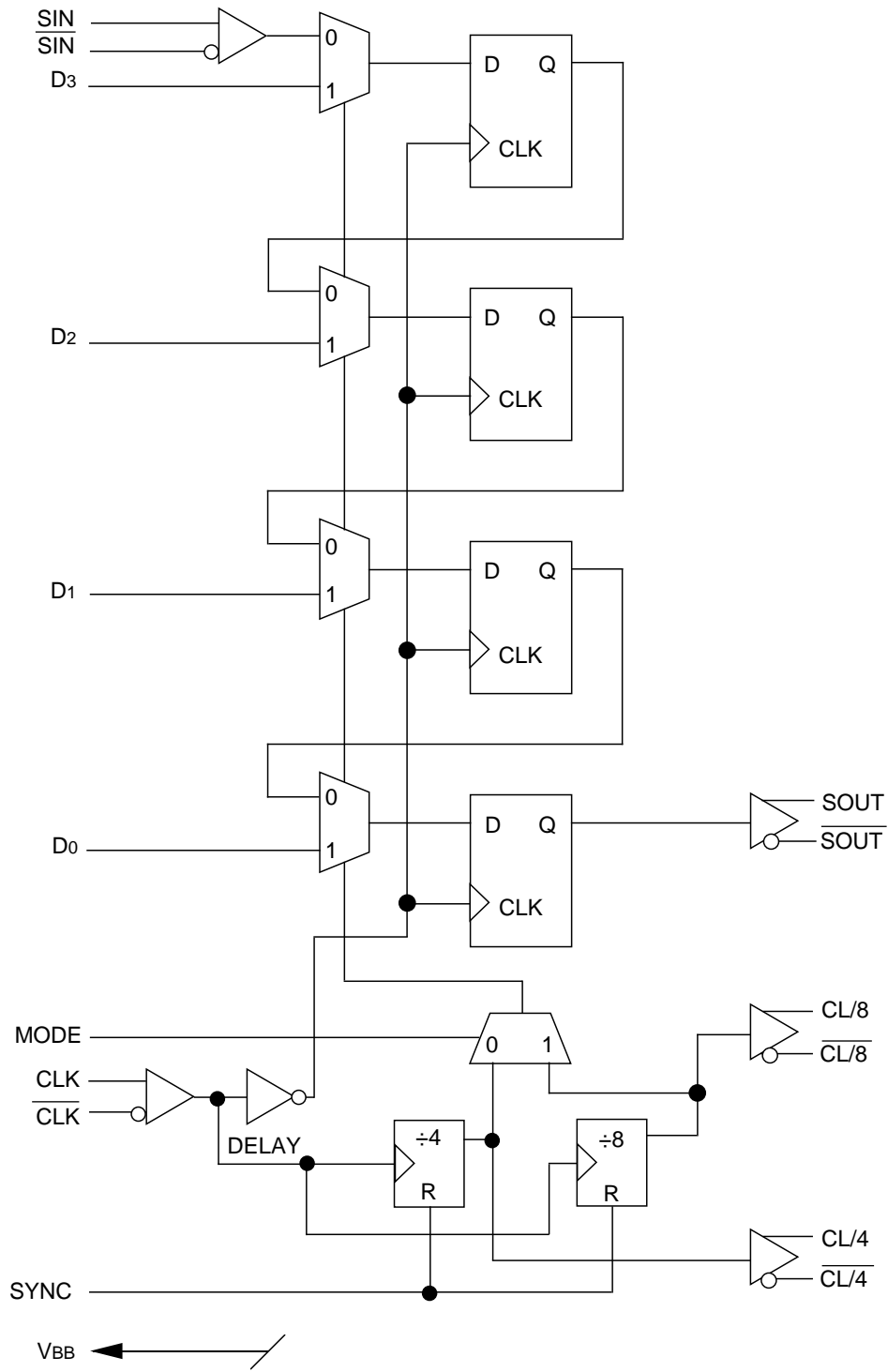
**PIN CONFIGURATION**



**PIN NAMES**

Pin	Function
SIN, $\overline{\text{SIN}}$	Differential Serial Data Input
D0 – D3	Parallel Data Input
SOUT, $\overline{\text{SOUT}}$	Differential Serial Data Output
CLK, $\overline{\text{CLK}}$	Differential Clock Input
CL/4, $\overline{\text{CL/4}}$	Differential 4 Clock Output
CL/8, $\overline{\text{CL/8}}$	Differential 8 Clock Output
MODE	Conversion Mode, 4-bit/8-bit
SYNC	Conversion Synchronizing Input
VCCO	VCC to Output

**BLOCK DIAGRAM**



**TRUTH TABLE**

Mode	Conversion
L	4-Bit
H	8-Bit

**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = V_{EE} (\text{Min.})$  to  $V_{EE} (\text{Max.})$ ;  $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
V <sub>OH</sub>	Output HIGH Voltage (SOUT Only) 10E (SOUT Only) 100E	-1020 -1025	— —	-790 -830	-980 -1025	— —	-760 -830	-910 -1025	— —	-670 -830	V	1
V <sub>BB</sub>	Output Reference Voltage 10E 100E	-1.38 -1.38	— —	-1.27 -1.26	-1.35 -1.38	— —	-1.25 -1.26	-1.31 -1.38	— —	-1.19 -1.26	V	—
I <sub>EE</sub>	Power Supply Current 10E 100E	— —	110 110	132 132	— —	110 110	132 132	— —	110 127	132 152	mA	—

**NOTE:**

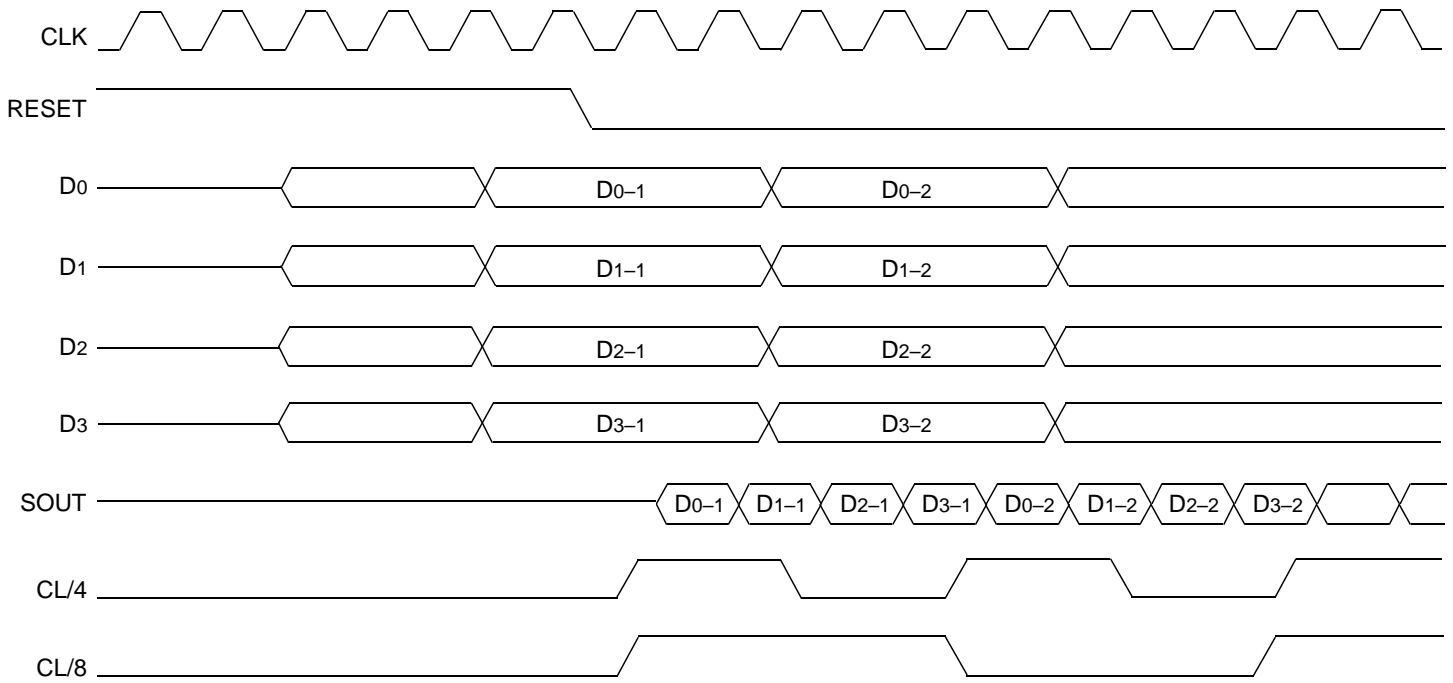
1. The maximum V<sub>OH</sub> limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V<sub>OH</sub> levels.

**AC ELECTRICAL CHARACTERISTICS**

$V_{EE} = V_{EE} (\text{Min.})$  to  $V_{EE} (\text{Max.})$ ;  $V_{CC} = V_{CCO} = \text{GND}$

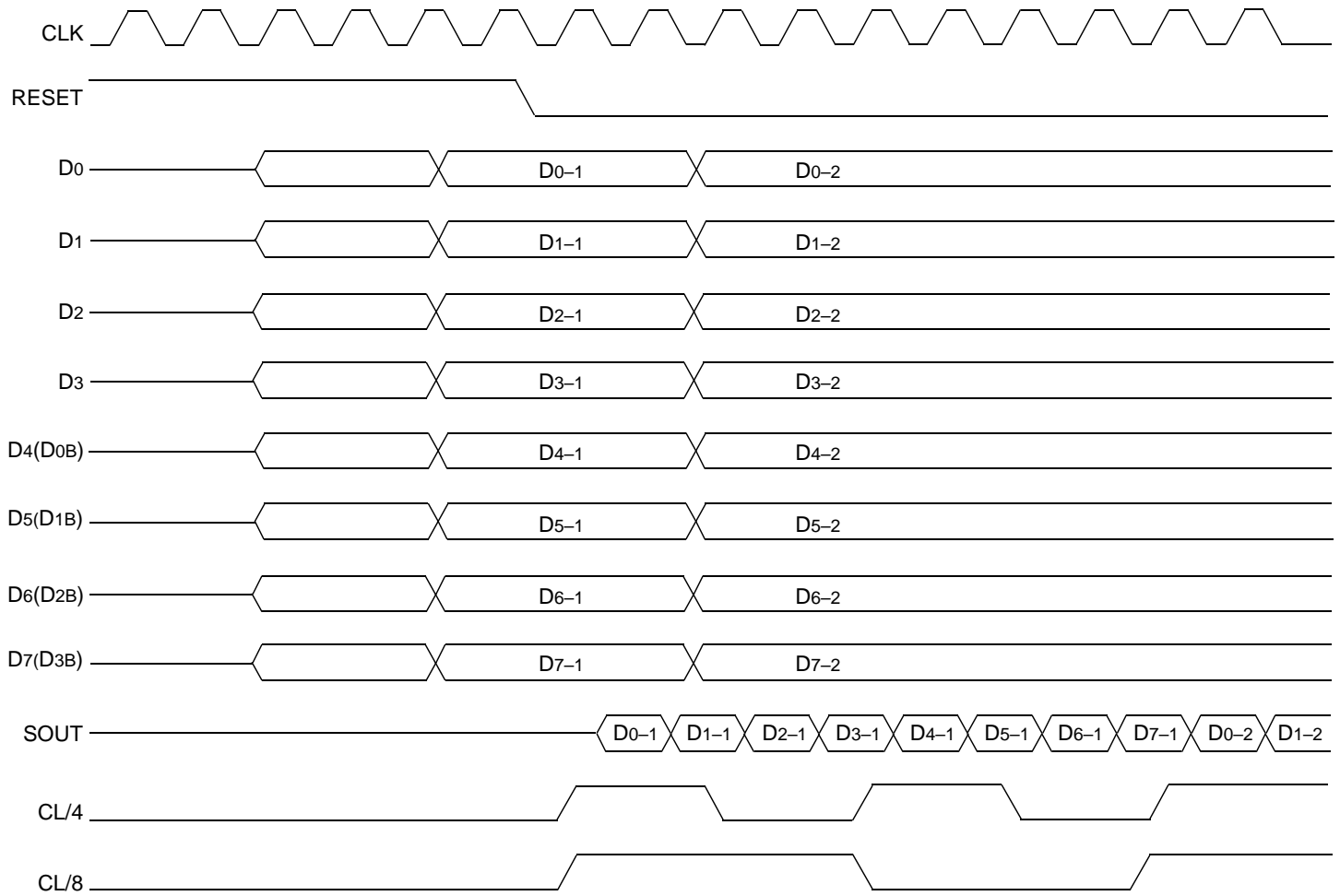
Symbol	Parameter	$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f <sub>MAX</sub>	Max. Conversion Frequency	1.3	1.6	—	1.3	1.6	—	1.3	1.6	—	Gb/s NRZ	—
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output CLK to SOUT CLK to CL/4 CLK to CL/8 SYNC to CL/4, CL/8	1000 500 800 500	1400 800 1100 800	1700 1100 1400 1100	1000 500 800 500	1400 800 1100 800	1700 1100 1400 1100	1000 500 800 500	1400 800 1100 800	1700 1100 1400 1100	ps	—
t <sub>S</sub>	Set-up Time SIN D <sub>n</sub> Mode	-200 -200 0	-400 -400 -250	— — —	-200 -200 0	-400 -400 -250	— — —	-200 -200 0	-400 -400 -250	— — —	ps	—
t <sub>H</sub>	Hold Time SIN D <sub>n</sub> Mode	750 800 500	550 600 300	— — —	750 800 500	550 600 300	— — —	750 800 500	550 600 300	— — —	ps	—
t <sub>RR</sub>	Reset Recovery Time	500	200	—	500	200	—	500	200	—	ps	—
t <sub>PW</sub>	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time SOUT Other	100 200	225 425	350 650	100 200	225 425	350 650	100 200	225 425	350 650	ps	20–80%

**TIMING DIAGRAMS**



Timing Diagram A. 4:1 Parallel-to-Serial Conversion

**TIMING DIAGRAMS (CONTINUED)**



**Timing Diagram B. 8:1 Parallel-to-Serial Conversion**

**APPLICATIONS INFORMATION**

The SY10E/100E446 are integrated 4:1 parallel-to-serial converters. The chips are designed to work with the E445 device to provide both transmission and receiving of a high-speed serial data path. The E446 can convert 4 bits of data into a 1.3Gb/s NRZ data stream. The device features a SYNC input which allows the user to reset the internal clock circuitry and restart the conversion sequence (see Timing Diagram A). Note that SOUT is triggered by negative clock edges.

The E446 features a differential serial input and internal divide-by-eight circuitry to facilitate the cascading of two devices to build an 8:1 multiplexer. Figure 1 illustrates the architecture for an 8:1 multiplexer using two E446s (see Timing Diagram B). Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs (SIN) of the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock-to-serial output propagation delay, plus the set-up time of the

serial input pins, must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet,  $t_{PD} \text{ CLK to SOUT} = 1600\text{ps}$  and  $t_s \text{ for SIN} = -200\text{ps}$ , yields a minimum period of 1400ps or a clock frequency of 700MHz.

The clock frequency is somewhat lower than that of a single converter. In order to increase this frequency, it is recommended that the clock edge feeding the E446A be delayed with respect to the E446B, as shown in Figure 2.

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E446. By connecting the clock for E446A to the complimentary clock input pin, the device will clock a half a clock period after E446B (Figure 2). Utilizing this simple technique will raise the potential conversion frequency up to the maximum 1.3GHz of a stand-alone E446.

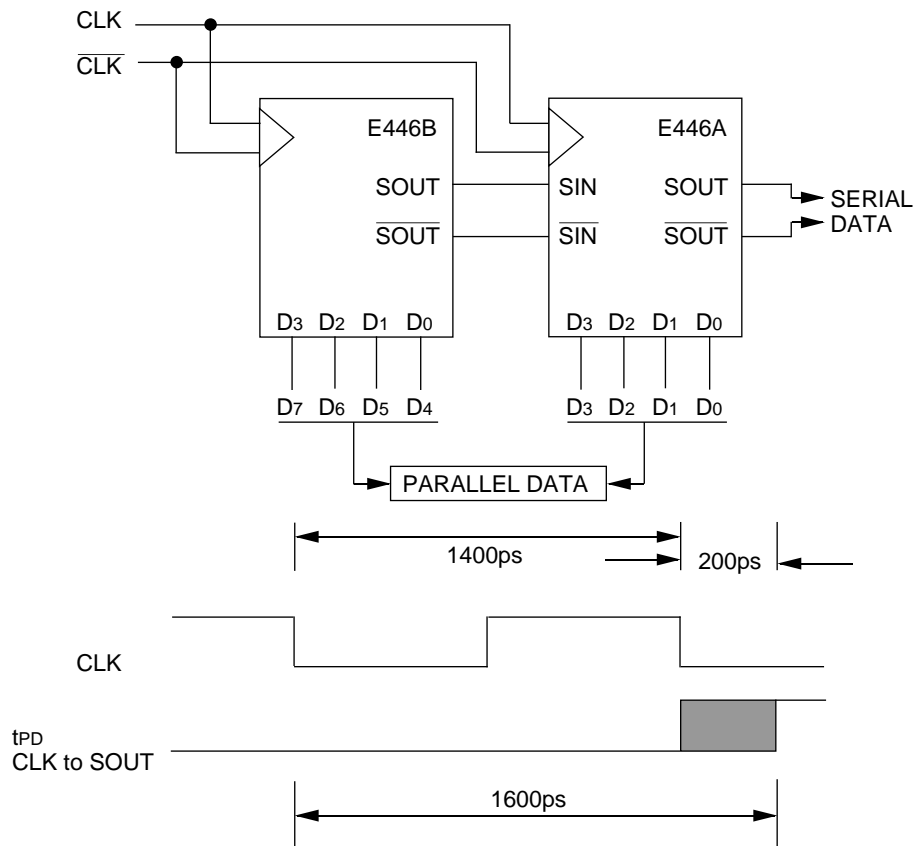


Figure 1. Cascaded 8:1 Converter Architecture

**APPLICATIONS INFORMATION**

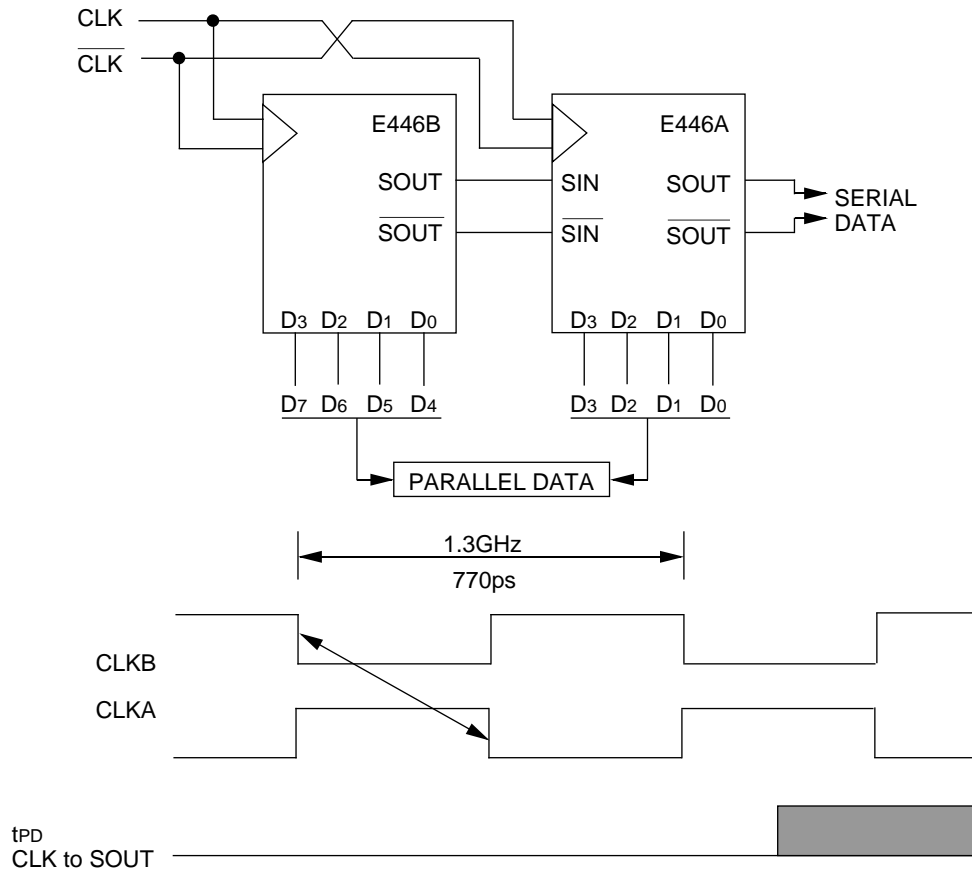
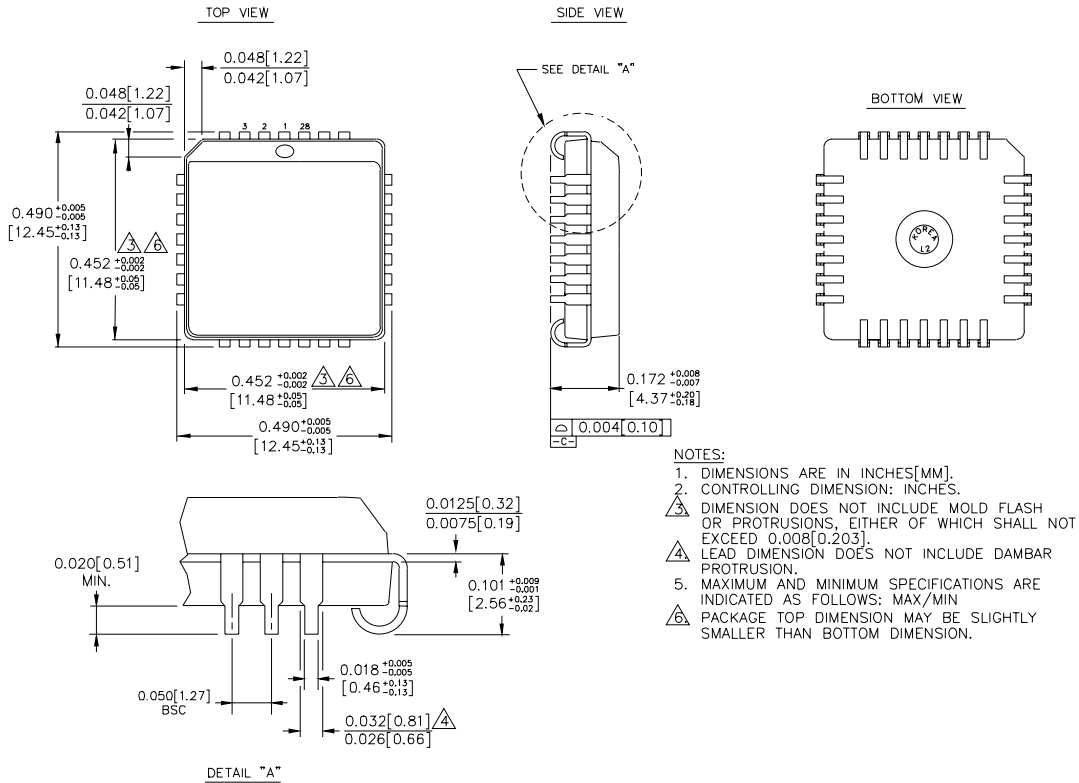


Figure 2. Extended Frequency 8:1 Converter Architecture

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range
SY10E446JC	J28-1	Commercial
SY10E446JCTR	J28-1	Commercial
SY100E446JC	J28-1	Commercial
SY100E446JCTR	J28-1	Commercial

**28 LEAD PLCC (J28-1)**



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
  2. CONTROLLING DIMENSION: INCHES.
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
  4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
  5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
  6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**  
TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

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