

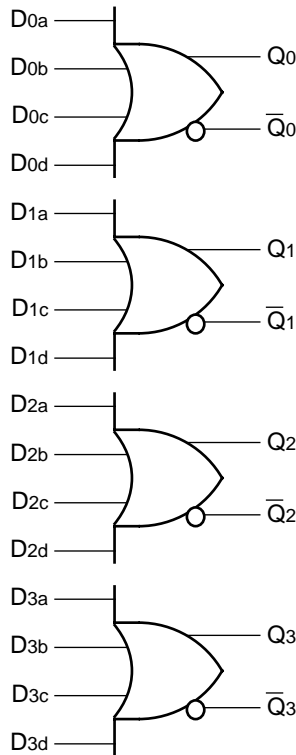
**FEATURES**

- 500ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- True and complementary outputs
- Fully compatible with industry standard 10KH, 100K I/O levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E101
- Available in 28-pin PLCC package

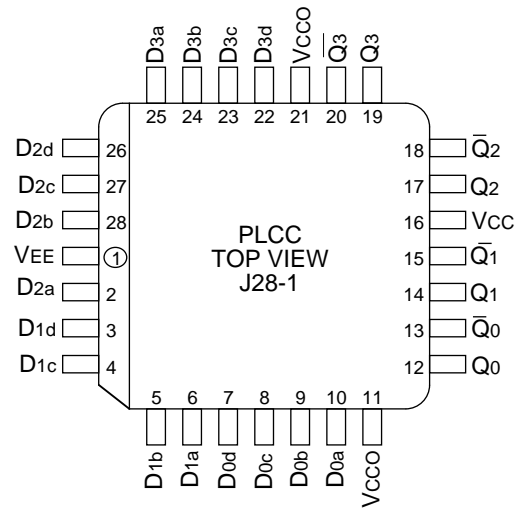
**DESCRIPTION**

The SY10/100E101 are quad 4-input OR/NOR gates designed for use in new, high-performance ECL systems. The E101 features both true and complementary outputs.

**BLOCK DIAGRAM**



**PIN CONFIGURATION**



**PIN NAMES**

Pin	Function
Dna, Dnb, Dnc, Dnd	Data Inputs
Q0-Q3	True Outputs
Q0-bar-Q3-bar	Inverting Outputs
Vcco	Vcc to Output

**LOGIC EQUATION**

$$Q_n = D_{na} + D_{nb} + D_{nc} + D_{nd}$$

**DC ELECTRICAL CHARACTERISTICS**

$V_{EE} = V_{EE}(\text{Min.})$  to  $V_{EE}(\text{Max.})$ ;  $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I <sub>IH</sub>	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
I <sub>EE</sub>	Power Supply Current	—	—	—	—	—	—	—	—	—	—	—	—	mA
	10EL	—	30	36	—	30	36	—	30	36	—	30	36	
	100EL	—	30	36	—	30	36	—	30	36	—	35	42	

**AC ELECTRICAL CHARACTERISTICS**

$V_{EE} = V_{EE}(\text{Min.})$  to  $V_{EE}(\text{Max.})$ ;  $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output D to Q	150	—	550	200	350	500	200	350	500	200	350	500	ps
t <sub>skew</sub>	Within-Device Skew <sup>(1)</sup>	—	50	—	—	50	—	—	50	—	—	50	—	ps
	Within-Gate Skew <sup>(2)</sup>	—	25	—	—	25	—	—	25	—	—	25	—	ps
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20% to 80%	275	—	625	300	380	575	300	380	575	300	380	575	ps

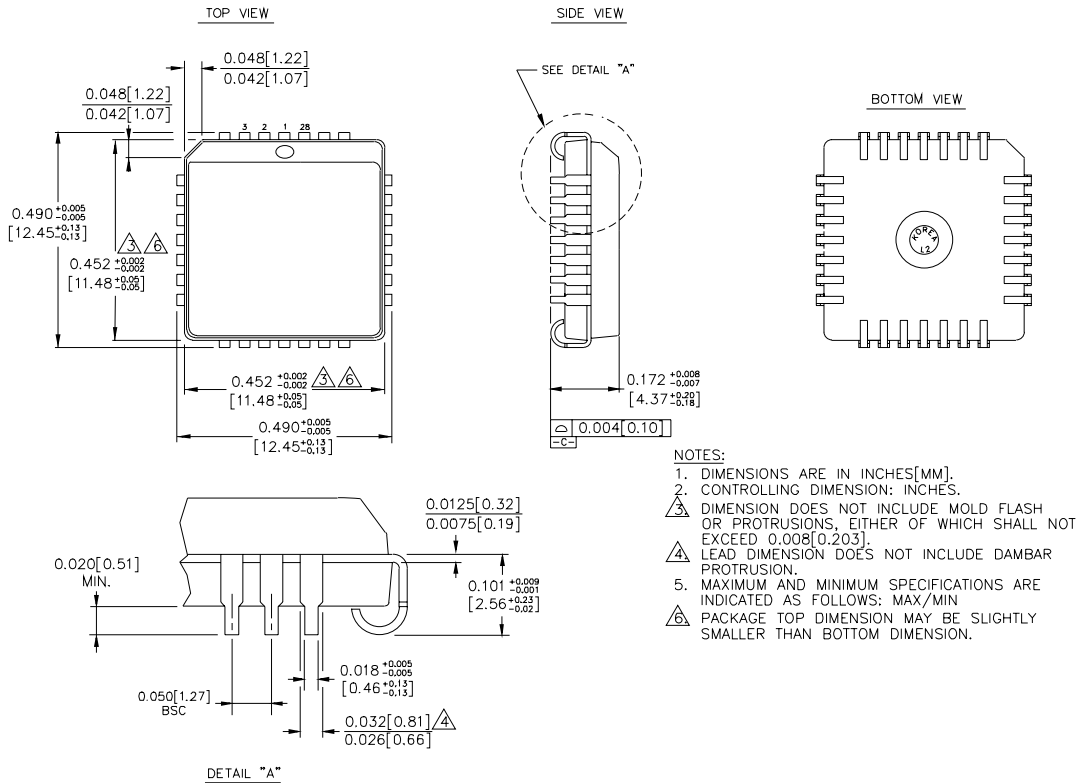
**NOTES:**

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagation delays through a single gate when driven from its different inputs.

**PRODUCT ORDERING CODE**

Ordering Code	Package Type	Operating Range	Ordering Code	Package Type	Operating Range
SY10E101JC	J28-1	Commercial	SY10E101JI	J28-1	Industrial
SY10E101JCTR	J28-1	Commercial	SY10E101JITR	J28-1	Industrial
SY100E101JC	J28-1	Commercial	SY100E101JI	J28-1	Industrial
SY100E101JCTR	J28-1	Commercial	SY100E101JITR	J28-1	Industrial

**28 LEAD PLCC (J28-1)**



Rev. 03

**MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA**

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