DATASHEET

RC1800
Foundation Slice Family

April 2003

Advance

LSI LOGIC®

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This document describes LSI Logic Corporation's RC1800 Foundation Slice family and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

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Preface

This document provides an overview of the RapidChip program and describes the functional blocks within the RC1800 Foundation Slice family in detail. The detailed information provided includes functional block descriptions, configurability, testing, packaging data, and specifications.

Audience

This document assumes you are familiar with custom logic design, either with ASICs or FPGAs, and related support tools. The people who benefit from this book are:

- engineers and managers who are evaluating the RC1800 Foundation Slices for possible use in a chip
- engineers who are designing the RC1800 Foundation Slices into a system

Organization

This document has the following sections and appendixes:

- Section 1, “The RapidChip™ Program,” provides a high-level description of the RapidChip program.
- Section 2, “RC1800 Foundation Slices,” provides detailed descriptions of the configurable I/Os, IPs, memories, PLLs, and clocking resources that are available in the RC1800 Foundation Slice family.
- Section 3, “Library Elements,” briefly describes the available libraries.
- Section 4, “Design Tools,” presents an overview of the design flow process and the RTL generation tools used.

- Section 5, “Packaging,” provides the mechanical drawings and specifications for the initial package drawings.
- Section 6, “Specifications,” lists the electrical specifications and AC timing parameters for the RC1800 Foundation Slice family.

Related Publications

Overview of G12® Cell-Based Technologies, DB06-000160-04

GigaBlaze® G12™ Rev 1.0 Core Design Manual, DB14-000079-02

G12 DDR Core (cw000701_2_0) Design Manual, DB14-000169-03

ARM 926EJ-S Technical Reference Manual, ARM Ltd.

Conventions Used in This Manual

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

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RC1800 Foundation Slice Family
Datasheet

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1 The RapidChip™ Program

The RapidChip program from LSI Logic is a fundamentally new way for engineers to design custom ICs. This robust platform approach to silicon design combines the best attributes of FPGA and standard-cell ASIC product spaces. Using new technologies and methodologies, the RapidChip program delivers packaged, tested, working silicon with complex embedded Intellectual Property (IP) in half the time needed by current methods and at one-quarter their development costs.

The primary objectives of the RapidChip product line are:

- Dramatically reduce time-to-market for complex, highly integrated, high-performance custom ICs
- Dramatically reduce engineering costs, CAD tool costs, and tooling costs associated with the development of deep submicron devices
- Deliver a very cost-effective production solution for use in medium-volume applications

RapidSlice™ silicon platforms, also known as slices, use LSI Logic 0.18 micron (G12®) and 0.11 micron (Gflx™) cell-based ASIC technologies, resulting in near ASIC performance, density, and power consumption. The diffused memories and IP cores within slices are the same as those used in LSI Logic cell-based ASIC product offerings.

The fundamental technology used in the RapidChip program is the metal customization of a partially manufactured semiconductor wafer, containing multiple copies of a predefined slice. The silicon layers of a slice are predefined and implement diffused IP resources that are connected later with customer-specific metallization patterns. Each slice incorporates diffused memory blocks, PLLs, IP blocks from the extensive LSI Logic CoreWare® library, and a configurable Transistor Fabric. The I/O ring is made up of configurable and dedicated I/Os to satisfy specific needs.

Because slices are available as partially manufactured devices, lead times for prototypes and production units are reduced dramatically and benefit customers with lower inventory costs. The broad range of resources available in slices also ensures that the needs of many different systems and applications can be met.

1.1 RapidSlice Platform Elements

This section describes the different elements that can be incorporated on a RapidSlice platform.

1.1.1 Transistor Fabric and R-Cells

The Transistor Fabric provides the basis for the implementation of the user's logic. An R-Cell is the basic unit within the Transistor Fabric; it is made up of specially sized "N" and "P" type transistors for maximum flexibility and performance. R-Cells are diffused in a regular pattern throughout the slice and are architected to implement memory as well as logic structures efficiently. They are configured in up to five layers of metal to create the full range of logic functions available within the RapidChip logic cell library. The library contains over 400 cells, with a range of drive strengths. R-Cells can be configured efficiently as small memory blocks, further adding flexibility to a designer's memory implementation. Transistors within the Fabric are activated only when they are part of the implementation of a function used in the design, ensuring the most power-efficient solution.

1.1.2 Embedded Memory Blocks

Single-port and dual-port, high-density, high-performance RAM blocks are diffused into each slice, defining a memory space that can be configured to meet a particular application need. The customization of the memory space is done using the GenMem tool. Memory blocks can be combined to create larger memories. Diffused memories also can be combined with RAMs constructed from the Transistor Fabric, allowing designers to specify memory arrays of arbitrary width and depth. The result is the most efficient use of resources without sacrificing diffused RAM capacity.

1.1.3 IP Blocks

Depending on the specifications, a CoreWare IP block is delivered in one of three distinct forms: Hard, Firm, or Soft.

- Hard IP blocks are diffused at optimal locations within the RapidSlice platform using cell-based elements for maximum performance and density.

- Firm IP blocks are preconfigured for high performance and have known characteristics. They are locatable anywhere within the Transistor Fabric region of a slice design.
- Soft IP blocks are incorporated into the RapidChip design as functional blocks and are implemented in the Transistor Fabric like any other block in the design with specific timing criteria to ensure their functionalities.

1.1.4 Configurable I/Os

High-performance I/O is one of the key features of RapidChip products. Dedicated I/Os are diffused in the slice where industry standards dictate and performance and power provide justification.

Because designers require flexibility, all slices have Configurable I/Os, of which all can address the most commonly used signalling standards, such as LVTTL, LVDS, HSTL, SSTL, and so on. Through use of the LSI Logic GenIO configuration tool, designers specify the industry standard as well as voltage levels, drive strengths, and pin locations.

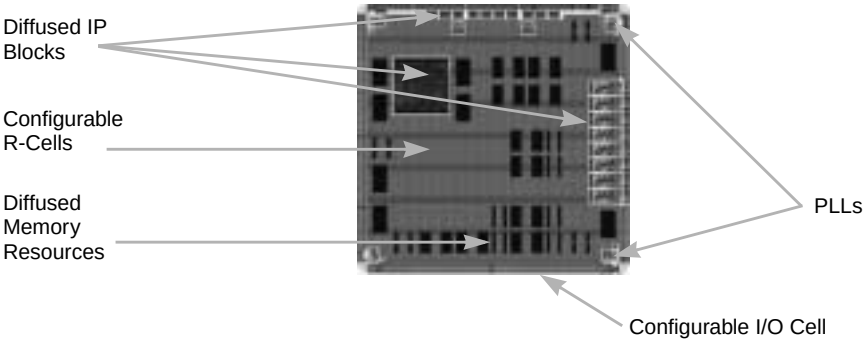
These design parameters cause the tool to create customized metal patterns that connect uncommitted transistor networks in a slice's I/O region in order to implement all required buffer types.

When taken in combination with packages optimized to the I/O capabilities of the RC1800 Family of Slices, LSI Logic Configurable Buffer technology provides extremely flexible I/O assignments that are simultaneous switching output (SSO) hazard-free.

1.1.5 Typical RapidSlice Platform

Figure 1 shows a typical slice with the major elements highlighted.

Figure 1 Typical RapidSlice Platform



1.2 Packaging

RapidSlice platforms have individually optimized packages to ensure all electrical and mechanical design requirements are met based on worst-case conditions. The design and construction of each package provides a highly optimized electrical environment and excellent thermal characteristics for the most demanding applications. Each package also meets the requirements for very high-speed serializer/deserializer (SERDES) I/Os. The number of I/Os, the available IP resources, the performance, and the power consumption of a particular slice determine which package(s) can be used.

With multiple low-inductance independent power and ground domains, all packages are optimized to reduce VDD/VSS path inductance, signal I/O path inductance, and signal-to-signal crosstalk, resulting in superior signal integrity. 100% differential pair routing for I/Os with a Z_0 of 50-55 ohms provides a “no compromises” environment for operating multiple high-performance SERDES at the maximum data rates of 3.1875 Gbits/s. Alternatively, single-ended configurable I/Os can utilize differential traces as single-ended transmission lines with a Z_0 of 100 ohms.

To simplify the task of PCB design, solder ball layouts are optimized by placing the I/Os in columns between VDD/VSS, allowing for efficient escape routing with fewer signal layers when using conventional PCB

geometries. As of this printing, 1 mm ball pitch FC-BGA packages are available for the RC1800 Foundation Slice family. Other package types will be available in the near future. Contact your local LSI Logic sales representative for more information.

1.3 RC1800 Foundation Slices

Table 1 lists the seven initial members of the RC1800 Foundation Slice Family. Slices differ from one another in terms of available IP, gate, memory, and I/O resources. As project needs evolve, designers have the option to migrate gracefully to another slice for accessing needed IP, memory, I/O, and gate resources.

RC1800 family members integrate the most popular System-on-a-Chip IP building blocks and leverage LSI Logic Corporation's unrivalled experience in CoreWare based System-on-a-Chip integration. Designers can draw from the following:

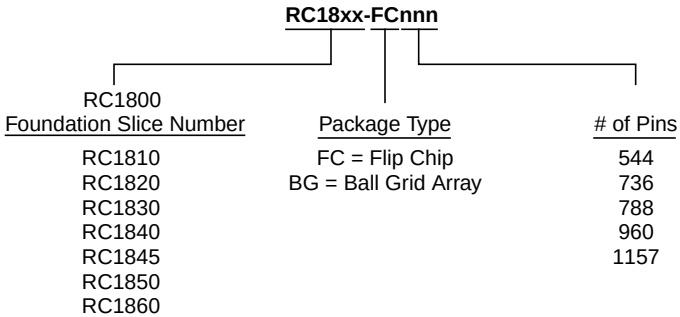
- 200 MHz ARM926 processor
- GigaBlaze SERDES Transceivers
- High-Performance DDR PHY

Listed by device number, Table 1 summarizes the main attributes of the initial RC1800 Foundation Slices and their resource configurations. The slice device numbering conventions are elaborated in Figure 2.

Table 1 RC1800 Foundation Slices

	RC1810-FC544	RC1820-FC736	RC1830-FC788	RC1840-FC960	RC1845-FC960	RC1850-FC1157	RC1860-FC1157
Customer Usable Gates (M)	0.5	1.0	1.3	1.5	1.8	2.2	2.5
# of 211 9-KBit Blocks (256x36)	8	8	6	12	12	12	16
# of 211 36-KBit Blocks (1Kx36)	6	8	12	16	16	20	24
# of 222 9-KBit Blocks (256x36)	2	4	4	8	8	8	12
# of 111 144-KBit Blocks (2Kx72)	2	4	3	5	6	8	2
Grand Total of RAM bits (M)	**0.6**	**1.0**	**0.9**	**1.6**	**1.6**	**2.0**	**1.3**
ARM926 with 8K/8K Caches	0	0	0	1	1	1	0
GigaBlaze SERDES Transceivers @3.1875 GHz	4	4	4	8	0	8	12
DDR PHY Bits	0	0	40	40	0	80	0
# of 600 MHz to 1250 MHz PLLs # of 100 MHz to 500 MHz PLLs	1 3	1 3	1 3	1 3	1 3	1 3	1 3
Base Configurable I/Os Configurable I/Os with DDR PHY	304	422	428 346	486 404	638	514 432	546
Number of pins (1 mm pitch) FC-BGA Package Body Size	544 27 mm	736 31 mm	788 31 mm	960 35 mm	960 35 mm	1157 40 mm	1157 40 mm

Figure 2 RC1800 Slice Numbering Conventions



1.4 Features Summary

The key features of the RapidChip program and RC1800 Foundation Slices are listed below:

- RapidChip technology combines a partially manufactured slice with customer logic, which is fixed in the metallization layers
- RapidSlice platforms have the following:
  - Base silicon with fully diffused memories, IP, and R-Cells
  - Completed power mesh and package planning
- The RC1800 Foundation Slices allow designers to specify:
  - 4, 8, or 12 GigaBlaze SERDES Transceivers
  - High-performance diffused 200 MHz ARM926 CPU
  - Multiple soft processor cores implementable in the Transistor Fabric
  - Choice of 40-bit or 80-bit wide DDR PHY with optimized data path
  - Memory options
    - ◊ High-performance single and dual port RAMs, ranging from 600 Kbits to 2.0 Mbits per slice
    - ◊ Arbitrary number of RAM blocks (up to 9 Kbits each) built on the Transistor Fabric
  - Flexible choice of Phase-Locked Loops (PLLs)
    - ◊ Standard PLL (VCO range from 100 to 500 MHz)
    - ◊ High-Range PLL (VCO range from 600 to 1250 MHz)
  - Device-optimized Ball Grid Array (BGA) Packages (1 mm ball pitch)

2 RC1800 Foundation Slices

This section covers the features of the available functional blocks within the RC1800 Foundation Slices and describes their configurations.

2.1 Configurable I/Os

The RC1800 Foundation Slice family provides designers with access to a broad range of user-configurable I/O types. Configured by patterning of metal interconnect, RC1800 I/O buffers are compact yet address the majority of industry-standard applications without overheads associated with reprogrammability.

Through optimization of package power domains and slice-specific VDD/VSS placements, the configuration I/O resources of RC1800 slices enable designers to assign buffers with fine granularity of typically four or eight pins per group.

Table 2 lists the available I/O bus types and drive strengths for I/Os.

Table 2 I/O Driver Types and Strengths

I/O Signaling Standard	Type	Vdd Voltage	Drive Strength
CMOS/LVTTL[1]	Bidirect	3.3 V	12 ma
			8 ma
			4 ma
			2 ma
CMOS/LVTTL[1]	Bidirect	2.5 V	12 ma
			8 ma
			4 ma
			2 ma
CMOS/LVTTL[1]	Bidirect	1.8 V	12 ma
			8 ma
			4 ma
			2 ma

Table 2 I/O Driver Types and Strengths (Cont.)

I/O Signaling Standard	Type	Vdd Voltage	Drive Strength
SSTL-2	Bidirect	2.5 V	Class-1
			Class-2
HSTL Single-Ended	Bidirect	1.5 V	Class-1
			Class-2
			Class-3
LVDS Differential Output	Output	2.5 V	4 ma
LVDS Differential Input	Input	2.5 V	
LVPECL	Input	3.3 V	
PCI-66	Bidirect	3.3 V	
Impedance Match (50 ohm)	Bidirect	3.3 V	

1. Available with pull-ups and pull-downs.

2.2 GigaBlaze SERDES Transceivers

Depending on the selected RC1800 slice, designers can specify 4, 8, or 12 GigaBlaze SERDES transceivers. These transceivers support multiple serial transfer rates up to 3.1875 Gbits/s, and comply with a wide range of industry standards.

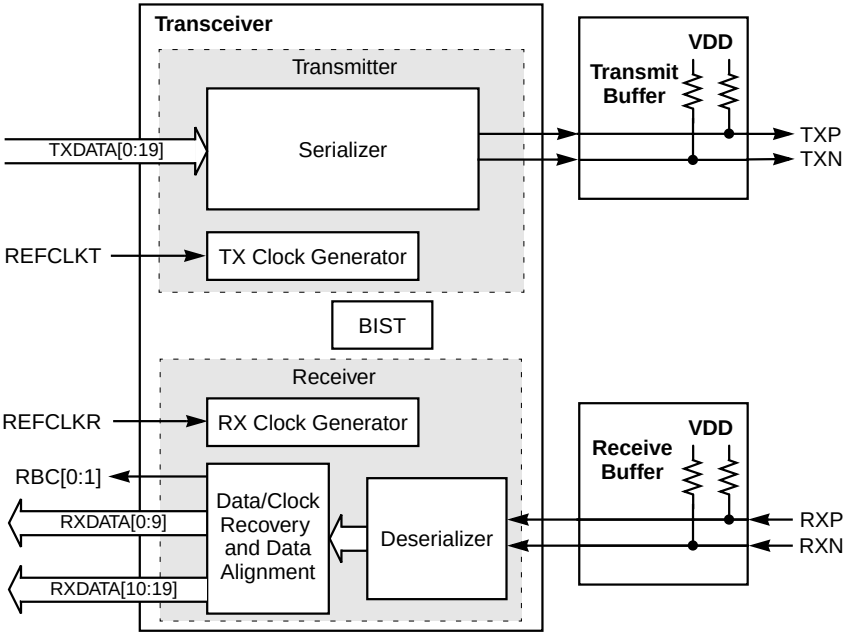
Table 3 lists the serial data rates and the standards for each rate.

Table 3 Range of Serial Data Rates

Serial Data Rate (Gbits/s)	Standard
1.0625	Fibre Channel
1.25	Gigabit Ethernet
1.5	Serial ATA, SAS
2.125	Fibre Channel
2.5	Infiniband
3.0	SAS
3.125	10 Gigabit Ethernet XAUI
3.1875	10 Gigabit Fibre Channel XAUI

Figure 3 is a block diagram of the GigaBlaze SERDES transceiver, which consists of a full-duplex transceiver, a built-in self-test (BIST) unit, and special high-speed transmit and receive buffers.

Figure 3 GigaBlaze SERDES Transceiver Block Diagram



Because the transmitter and receiver operate independently, the GigaBlaze SERDES transceiver can send and receive data simultaneously. The GigaBlaze SERDES transceiver allows the transmitter and receiver to work at different data transfer rates. It transmits data at a rate controlled by the Reference Clock (REFCLKT). The transmitter accepts 20-bit parallel data clocked in on REFCLKT. It serializes and transmits the data at 20 times the REFCLKT frequency.

The transmitter serializes data input on the TXDATA bus and transmits the bitstream in nonreturn-to-zero (NRZ) format from its dedicated differential transmit buffer. The buffer drives the internally terminated adjustable swing differential pair, TXP/TXN. Notice that the transmitter does not send a separate clock signal; instead, the receiver recovers the clock from the bitstream.

From the differential pair, RXP/RXN, the internally terminated receive buffer accepts a 1.0625 to 3.1875 Gbits/s serial bitstream. The receiver then deserializes the bitstream, recovers the embedded clock (RBC), recovers parallel data, optionally aligns data on a selectable synchronization pattern, and outputs the recovered parallel data 10 or 20 bits at a time on the RXDATA bus. The receiver outputs 20-bit parallel data at the RBC frequency or 10-bit parallel data at twice the RBC frequency. Control inputs to the receiver can select the synchronization pattern and the width of the recovered data. The complementary recovered clock outputs (RBC[0:1]) can be used by other logic to clock the output on the RXDATA bus.

To facilitate testing and system bring-up, the GigaBlaze SERDES transceiver includes:

- Two internal serial loopback paths from TXP/TXN to RXP/RXN
- An internal serial reverse loopback path from RXP/RXN to TXP/TXN
- An internal parallel wrapback from the transmitter's input parallel data to the receiver's data alignment unit (DAU)
- Full scan to achieve high fault coverage in the transceiver's digital section
- A BIST unit that tests digital and analog sections

Through the internal loopback/wrapback or an external link, the BIST unit can transmit test patterns, compare them with received patterns, and alert external logic if they do not agree. With standard compliant

GigaBlaze SERDES transceivers, designers also benefit from the LSI Logic CoreWare library of link layer functions. The combination provides a low-risk route to enabling fully compliant 1 and 10 GigaBit Ethernet, Fibre Channel, and other applications.

In summary, the key features of the GigaBlaze SERDES transceiver are:

- 4, 8, or 12 per slice
- Serial transfer rates up to 3.1875 Gbits/s with BER of less than 1 in 10^{12}
- Standards support for Fibre Channel, Gigabit Ethernet, XAUI, SATA, SAS and InfiniBand
- Full-duplex operation: the transmitter and receiver can work at different data rates
- Internal serial loopback, digital parallel wrapback, BIST, and full scan to facilitate testing
- Adjustable differential output swing for driving coaxial and twinaxial cables, or a fiber-optic transmitter
- Low-swing differential input sensitivity
- Support for standard serial line impedances of 50 and 75 Ω (100 and 150 Ω differential) with internal termination

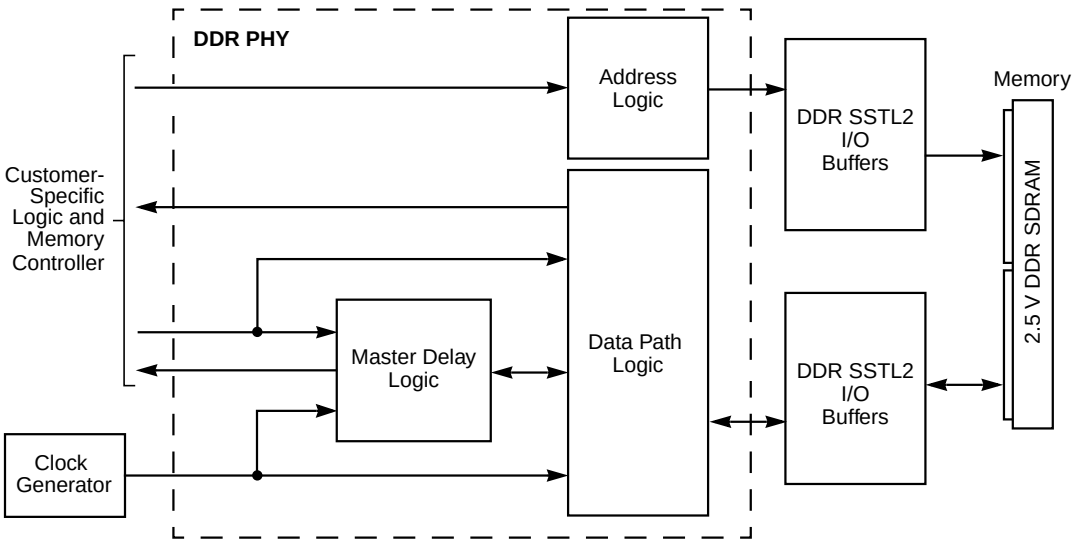
For more detailed information on this functional block, refer to the *GigaBlaze® G12™ Rev 1.0 Core Design Manual*.

2.3 Double-Data-Rate (DDR) PHY Support

In the RC1800 Foundation Slice Family, two DDR PHYs are available to designers: a 40-bit or an 80-bit wide data path. Both DDR PHYs perform 2:1 compression/decompression, alignment, and strobe forwarding of DQ/DQS signals. The DDR PHY contains a Data Path block and a Master Delay block. Figure 4 shows a simplified block diagram of the DDR PHY and its system interconnections.

The memory address signals, memory control signals, and differential clock signals are generated outside the DDR PHY as part of the customer-specific logic.

Figure 4 DDR PHY Simplified Block Diagram



2.3.1 DDR PHY Resources Key Features

In summary, the key features of the RC1800 DDR PHY resources are:

- Choice of 40-bit or 80-bit wide DDR PHY data path
- 166 MHz operation for data transfer rates up to 333 Mbits/s
- Internal scan
- Memory controller interfaces for ×4, ×8, ×16, and ×32 DDR SDRAM/FCRAM configurations
- Burst lengths of 2, 4, and 8
- Self-test
- Programmable delay of data strobe for read operations
- Digital Delay Locked Loop (DDLL) to maintain constant programmable delay over PVT
- 2X clock architecture to ensure 90-degree phase shift for DQS during write cycle

For more detailed information on this functional block, refer to the *G12 DDR Core (cw000701_2_0) Design Manual*.

2.3.2 Memory I/O Types

Table 4 lists the memories that can be configured for use with the DDR-specific resources available in RC1800 family slices. FCRAM memories typically are used for networking applications. Such memories support bit widths up to 16 and speeds up to 154 MHz.

Table 4 Supported DDR Memories

Memory Type	DC Levels	Density	Clock Speeds (MHz)	Organization (bits)
DDR1 SDRAM	SSTL-2 @ 2.5V	64 Mb	150, 167	x32
		128 Mb	167	x4, x8, x16
		256 Mb	167	x4, x8, x16
		512 Mb	167	x4, x8, x16
FCRAM	SSTL2 @ 2.5V, 2.5V Vdd	256 Mb	154	x8, x16

2.4 Embedded Microprocessor Support

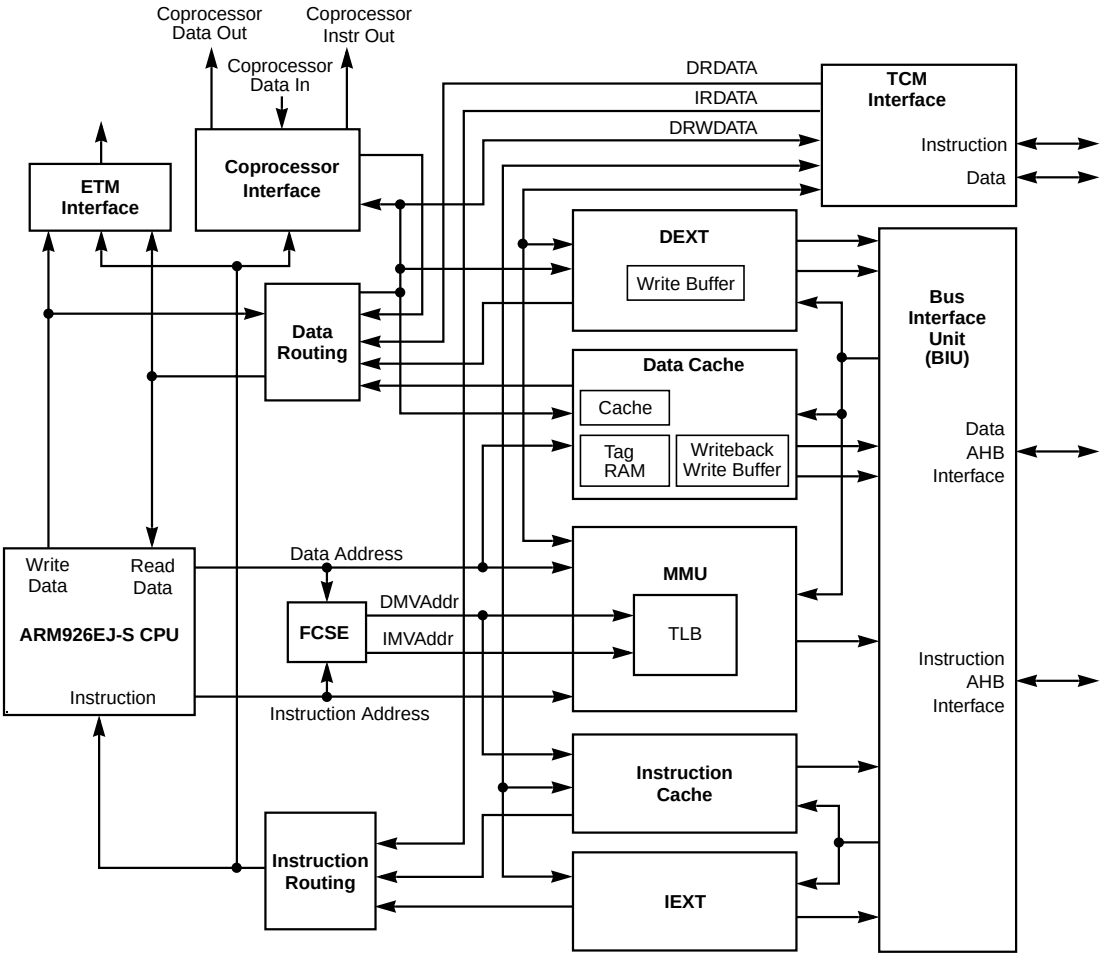
All RC1800 Foundation Slices support Firm and Soft implementations of LSI Logic ARM, MIPS, and ZSP processor families. Standardized support of the AMBA bus protocol with all three architectures simplifies reuse of peripherals and broadens access to leading third-party IP providers. Firm and Soft processor implementations use the memory and Transistor Fabric resources of an RC1800 Foundation Slice.

In addition, designers have the option of using a performance-optimized ARM926 processor. The diffused ARM926 processor operates at speeds up to 200 MHz and implements ARM architecture version 5TEJ. This processor supports the 32-bit ARM and 16-bit THUMB instruction sets and can execute 8-bit JAVA byte codes.

The ARM926 processor implemented in the RC1800 Foundation Slices contains an 8-Kbyte instruction cache and an 8-Kbyte data cache. The ARM926 incorporates an integer core and a memory management unit (MMU). It provides separate instruction and data buses for the AMBA AHB and Tightly Coupled Memory (TCM) interfaces. Designers have the option of defining some of the host slice's 111-type memory resources as TCMs. Up to 32 Kbytes each of zero wait-state instruction and data

TCMs can be supported this way. The ARM926 processor also includes support for external coprocessors.

Figure 5 ARM926 Processor Block Diagram



In summary, the key features of the diffused ARM926 processor are:

- Up to 200 MHz operation
- 8 Kbytes each Instruction Cache and Data Cache
- ARM Advanced High Performance Bus (AHB) interface unit with write buffer. Chose of 2:1 or 1:1 CPU-to-bus clock ratios for AHB bus operation (subject to a maximum user AHB speed limit of 166 MHz).

- Support for up to 32 Kbytes each Instruction and Data Tightly Coupled Memories (TCMs)

For more detailed information on this functional block, refer to the *ARM 926EJ-S Technical Reference Manual* from Arm Limited.

2.4.1 MMU

The ARM926 MMU implements ARM architecture v5. It provides an MMU and TLB resources to cache frequently used instructions and data accesses in external page tables. The TLB entries can be locked to ensure that a memory access to a specific region does not incur a page-table-walk penalty. Virtual memory and protected memory spaces are features of operating systems. Through its partner program, ARM provides designers with access to a wide range of OS solutions, including Linux, which can be implemented on MMU-enabled ARM processors, such as the ARM 926, available in the RC1800 slice family.

2.4.2 Caches and Write Buffer

The ARM926 processor contains separate instruction and data caches; it also contains a write buffer. The cache sizes are fixed at 8 Kbytes.

Both caches are virtual index, virtual tag. They are addressed using the Modified Virtual Address (MVAddr). Both caches are four-way set associative. A cache line is eight words in length (32 bytes per line). The DCache has two dirty bits and supports write-through and write-back cache operations for zero wait-state access.

2.4.3 Bus Interface Unit (BIU)

The BIU arbitrates and schedules AHB requests. It contains separate masters to handle both instruction and data accesses. Write buffers are used to prevent stalls from occurring during AHB writes.

2.4.4 Tightly Coupled Memory (TCM) Interface

The ARM926 processor contains a TCM controller that schedules requests to the TCM interface, provides handshake signals with the ARM926 memory system controller, and returns TCM read data to the ARM926 processor.

TCMs store real-time and performance critical code because accesses to these memories are deterministic and do not incur access penalties, such as the AHB access required for a cache miss.

TCMs support zero wait-state access. Only single-cycle access RAM can be used, which excludes the possibility of DMA access.

Depending on requirements, designers can specify either no TCM or implement up to 32 Kbytes each of Instruction TCM and Data TCM.

2.5 Memory Integration

Memory is implemented in the RC1800 Family of slices by configuring either Hard (Diffused) or Firm (fixed metal R-Cell) bit cell storage arrays. Under control of the GenMem tool, designers configure slice-specific memory resources and can logically combine Hard and Firm storage arrays in order to vary word width and address range. This section describes in more detail the Diffused and R-cell memories and their configurations.

2.5.1 Diffused Memories

The RC1800 Foundation Slices provide three types of Hard memory arrays, which implement 111-, 211-, and 222-type architectures. The key features of these memories are listed below.

- High-Density Single Port, 111 Type
  - One independent address
    - Read or write access to the storage array
  - Flexible 144-Kbit storage array reconfigurable as:
    - 2 Kwords by 72 bits
    - 4 Kwords by 36 bits
    - etc.
  - Bit-level write enable mask
  - Synchronous operation
- Simple Dual Port, 211 Type (36 Kbit)
  - Two independent addresses
    - One independent read address to the storage array

    - ◊ One independent write address to the storage array
  - Flexible 36-Kbit storage array, reconfigurable as:
    - ◊ 1024 words by 36 bits
    - ◊ 2048 words by 18 bits
    - ◊ etc.
  - Bit-level write enable mask
  - Synchronous operation
  - Efficient for creating large buffers and deep FIFOs
- Simple Dual Port, 211 Type (9 Kbit)
  - Two independent addresses
    - ◊ One independent read address to the storage array
    - ◊ One independent write address to the storage array
  - Flexible 9-Kbit storage array, reconfigurable as:
    - ◊ 256 words by 36 bits
    - ◊ 512 words by 18 bits
    - ◊ etc.
  - Bit-level write enable mask
  - Synchronous operation
- True Dual Port, 222 Type (9 Kbit)
  - Two fully independent addresses
    - ◊ One independent read or write address
    - ◊ Second independent read or write address
  - Flexible 9-Kbit storage array, reconfigurable as:
    - ◊ 256 words by 36 bits
    - ◊ 512 words by 18 bits
    - ◊ etc.
  - Partitionable address map to implement two smaller single-port 111-type RAMs
  - Write ports with independent bit-level enable masks
  - Synchronous operation

2.5.2 R-Cell Memories

R-Cell memories are created by the GenMem dedicated compiler tool, which generates metal interconnect for regions of R-Cells—the base units of a slice's Transistor Fabric.

The GenMem R-Cell RAM compiler supports the 211-type simple dual-port memory architecture. The key features of R-Cell memories are:

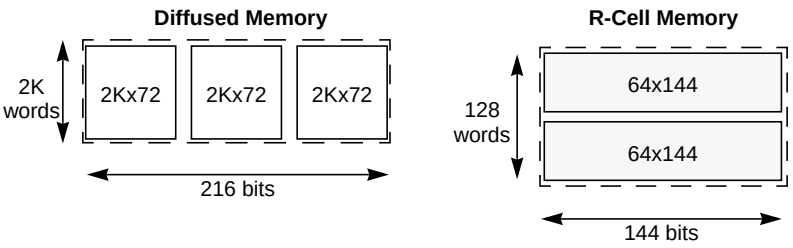
- R-Cell compiler
  - Flexible storage arrays up to 9,216 bits per array
    - ◊ Arbitrary word size from 4 bits to 144 bits per word
    - ◊ Arbitrary number of words from 8 words to 64 words per RAM
  - Dual-port 211-type architectures
  - Write ports with independent bit-level enable masks
  - Synchronous operation
  - Ideal for line buffers and small storage arrays that otherwise would make inefficient use of diffused RAMs

2.5.3 Configuration of Memories

The LSI Logic GenMem tool allows designers to specify configurations that flexibly combine Diffused and R-Cell memories to create single logical storage arrays.

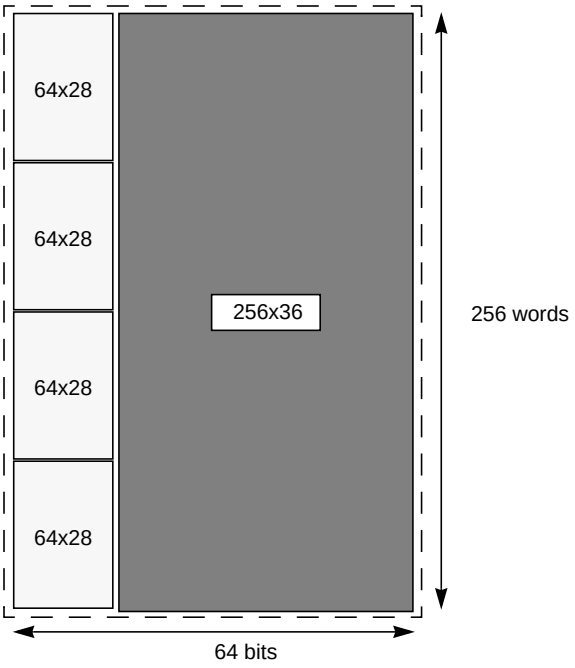
Diffused and R-Cell memories can be tiled together (see Figure 6). For example, a single-port 2K x 72 memory can be combined with two others to form a 2Kx216 memory. A 64x144 R-Cell memory can be combined with a second one to form a larger 128x144 memory.

Figure 6 Tiling of Memories



Diffused and R-Cell memories also can be mixed together. Figure 7 shows four tiled 64x28 R-Cell memories joined with a 256x36 Diffused memory to implement a single logical array of 256x64.

Figure 7 Memory Mixing



2.6 PLLs and Clocks

RapidSlice platforms provide designers with a number of options for implementing and managing clock networks. Clocks typically are derived from sources such as:

- External inputs, for example, crystal oscillators or direct inputs
- Customer-accessible PLLs
- PLLs included within diffused IP blocks
- Recovered clocks from data streams

In all cases, customer clock networks are implemented using *clock factories* and can be specified to operate at up to 166 MHz. Clock factories are created based on user specifications processed by the

GenClock tool. GenClock allows designers to manage skew and other clock net attributes with a consistent approach to clock domain reset and scan chain control, which simplifies test.

Designers can specify any number of clock factories (that is, clock domains) in an application. However, the number of different tunable clock networks (where edge alignment must be within a given tolerance) is limited by the available customer PLL resources. The RC1800 Foundation Slices each have four PLLs, so all slices can have a maximum of four tuned clocks.

System clock speeds of up to 166 MHz for RC1800 slices ensure that designers can work with realistic ASIC-like logic depths while staying close to the performance limits of the 0.18µ G12 technology. This in turn ensures that design closure after detailed place and route is predictable and results in significantly faster turnaround times.

In the case of specific performance critical Firm IP blocks, LSI Logic offers version of them with optimized layouts that exceed the 166 MHz constraint. Higher frequency blocks of customer logic, although possible, cannot be done with predictable turnaround time guarantees or fixed NRE.

The following subsections provide more information on the slice PLLs, clock generation, and clock testing. These subsections define a clock factory, which is comprised of a series of clock elements, and describe how the clock elements are handled in the design.

2.6.1 General-Purpose PLL Resources

Each RC1800 Foundation Slice contains four fully integrated, wide-range PLLs: one High-Range PLL and three Standard PLLs. The output frequency range of the Standard PLLs is 100 MHz to 500 MHz; the High Range PLL's output frequency range is 600 MHz to 1250 MHz. The external reference clock for each PLL can be either single-ended or differential and has dedicated impedance-controlled traces assigned within the slice's package.

Programmable charge pump settings allow stable operation and acceptable bandwidths to be achieved for frequency multiplication as high as M = 32 (Standard PLL) or M = 64 (High-Range PLL). Both PLL types employ a differential VCO powered by an integrated self-referenced

voltage regulator for reduced susceptibility to supply noise. They are powered through a 1.8V supply voltage.

Figure 8 shows a simplified block diagram of the PLLs. The Lock Detect macrocell determines whether or not the PLL is in lock.

Figure 8 PLL Block Diagram

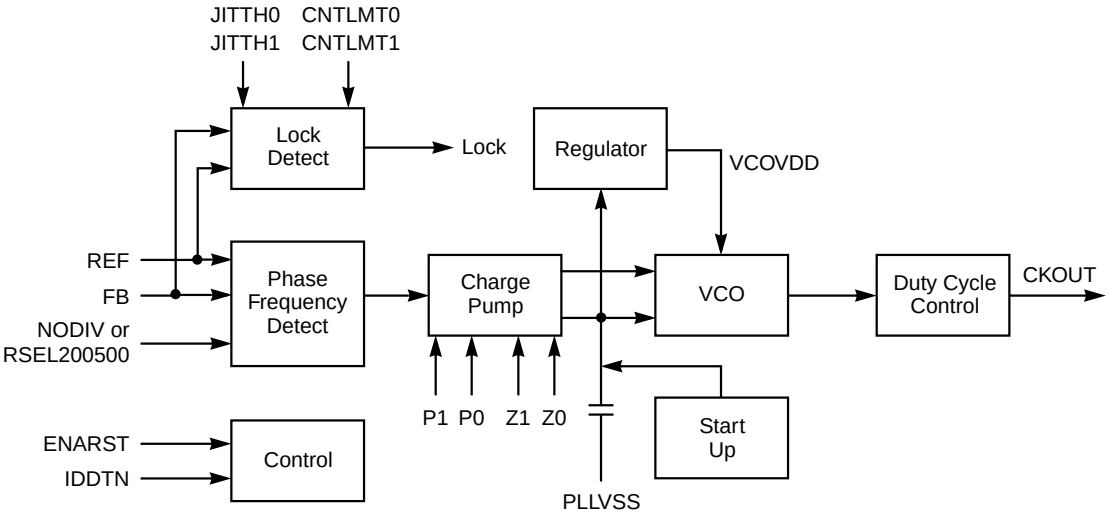


Table 5 defines the PLL signals.

Table 5 PLL Signal Descriptions

<table>
<tr><th>Signal</th><th>Type</th><th>Description</th></tr>
<tr><td>CKOUT</td><td>Output</td><td>PLL Output Clock.</td></tr>
<tr><td>CNTLMT0, CNTLMT1</td><td>Inputs</td><td>Counter settings.
<table>
<tr><th>CNTLMT1:CNTLMT0</th><th>Count</th></tr>
<tr><td>00</td><td>29</td></tr>
<tr><td>01</td><td>67</td></tr>
<tr><td>10</td><td>119</td></tr>
<tr><td>11[1]</td><td>253</td></tr>
</table>
1. Recommended setting.</td></tr>
<tr><td>ENARST</td><td>Input</td><td>This active-HIGH input enables auto reset.</td></tr>
<tr><td>FB</td><td>Input</td><td>Feedback Clock. This clock is active on the rising edge.</td></tr>
<tr><td>IDDTN</td><td>Input</td><td>IDD Test. This active-low signal disables the charge pump and drives VCO, CKOUT low.</td></tr>
<tr><td>JITTH0, JITTH1</td><td>Inputs</td><td>Jitter Threshold settings.
<table>
<tr><th>JITTH1:JITTH0</th><th>Min</th><th>Max</th></tr>
<tr><td>00</td><td>± 170 ps</td><td>± 530 ps</td></tr>
<tr><td>01</td><td>± 290 ps</td><td>± 860 ps</td></tr>
<tr><td>10</td><td>± 475 ps</td><td>± 1350 ps</td></tr>
<tr><td>11</td><td>± 725 ps</td><td>± 1950 ps</td></tr>
</table></td></tr>
<tr><td>LOCK</td><td>Output</td><td>A logic HIGH indicates LOCK. A logic LOW indicates no lock.</td></tr>
<tr><td>NODIV
(High-Range PLL only)</td><td>Input</td><td>This input sets the internal dividers. If M = 1, then NODIV is driven HIGH. If M > 1, then NODIV is driven LOW.</td></tr>
<tr><td>P1, P0</td><td>Input</td><td>These signals select the charge pump current.</td></tr>
</table>

Table 5 PLL Signal Descriptions (Cont.)

Signal	Type	Description
PLLVDD	Input	Analog VDD supply.
PLLVSS	Input	Analog VSS ground.
REF	Input	Reference Clock. This clock is active on the rising edge.
RESETN	Input	Active-LOW reset signal.
RSEL200500 (Standard PLL only)	Input	Range Select. When this input is LOW, the CKOUT range is 100 to 250 MHz. When this input is HIGH, the CKOUT range is 200 to 500 MHz.
Z1, Z0	Input	These signals select the feed forward current.

Tracking jitter is the difference in time between the rising edges of the REF and FB clocks. Tracking jitter can be positive or negative depending on whether the REF leads FB or vice versa. The PLL is “in-spec” when the Tracking jitter is within a certain threshold. This threshold can be changed by changing the JITTH0 and JITTH1 settings.

In order for the PLL to be in LOCK, the PLL needs to be in-spec for a certain number of consecutive cycles. The number of cycles can be changed by varying the CNTLMT0 and CNTLMT1 settings. If the Tracking jitter goes beyond the threshold for one or more cycles, then the LOCK signal is deasserted and the Tracking jitter must be in-spec for the specified number of cycles for the LOCK signal to be asserted. When the tracking jitter is no longer in-spec, then “lock” is asynchronously deasserted.

Table 6 shows the modes of operation that the PLLs support.

Table 6 PLL Modes of Operation

IDDTN[1]	ENARST[1]	RSEL200500	V(LP1)[2]	VCO	Description
Standard PLL					
H	H	H	V(LP1) > Vtn[3] V(LP1) < varst[4]	Active 200-500 MHz	Normal PLL Operation with Auto Reset. The PLL goes through an auto reset phase when a runaway condition is sensed on LP1. The PLL reacquires lock after t=TLOC after a runaway condition is detected.
		L		Active 100-250 MHz	
H	L	H	VDD+Vbe[5] >V(LP1)>Vtn	Active 200-500 MHz	Normal PLL Operation. Auto Reset circuitry is disabled. The user must detect a PLL runaway condition and reset the PLL when auto reset is disabled.
		L		Active 100-250 MHz	
L	X[6]	X	0	Output Low	IDD Test Mode. Charge pump and VCO operations are disabled, the integrated LP1 is discharged, CKOUT (clock tree input) is driven low, and the PLL is placed in a static quiescent state to support static IDD measurements or IDDQ vectors.
High-Range PLL					
H	H	N/A	V(LP1) > Vtn V(LP1) < varst	Active 600-1250 MHz	Normal PLL Operation with Auto Reset. The PLL goes through an auto reset phase when a runaway condition is sensed on LP1. The PLL reacquires lock after t=TLOC after a runaway condition is detected.
H	L	N/A	VDD+Vbe >V(LP1)>Vtn	Active 600-1250 MHz	Normal PLL Operation. Auto Reset circuitry is disabled. The user must detect a PLL runaway condition and reset the PLL when auto reset is disabled.
L	X[6]	N/A	0	Output Low	IDD Test Mode. Charge pump and VCO operations are disabled, the integrated LP1 is discharged, CKOUT (clock tree input) is driven low, and the PLL is placed in a static quiescent state to support static IDD measurements or IDDQ vectors.

1. IDDTN and ENARST are asynchronous.
2. V(LP1) = VCO control voltage.
3. Vtn = NMOS threshold voltage.
4. varst = Runaway threshold high.
5. Vbe = Bulk to drain diode threshold voltage.
6. VIN = PLLVDD or PLLVSS. Input pins not at the rail consume additional power.

2.6.2 Clock Factories

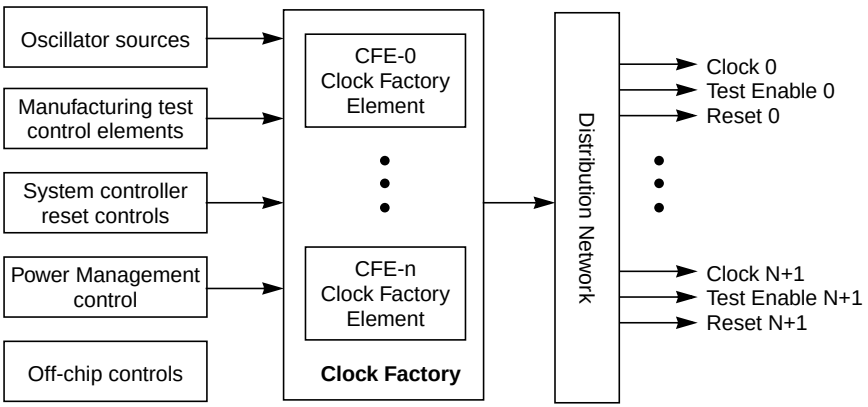
A clock factory is an encapsulation of clocking elements in a controlled and controllable fashion. The RTL code for a clock factory is generated by the LSI Logic GenClock tool, which takes into account user requirements and RapidChip specific design rules for clock networks. To be controlled, reasonable bounds must be placed on implementation variations. At the same time, controls/facilities are inserted into the clocking structures to make them flexible and extensible across a broad range of uses. Thus a clock factory can exploit known good code both logically and physically. The clock factory also includes the required hooks for DFT operation.

The primary input to a clock factory is an oscillator. This oscillator can be:

- an external crystal oscillator on a board,
- the output of a PLL, or
- the clock signal recovered from a communications data stream.

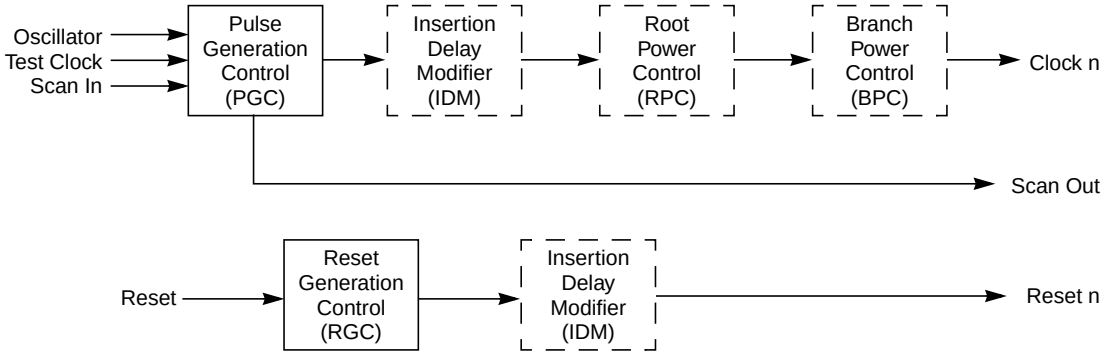
Where possible, all oscillators should be intercepted prior to their use as clocks and run through the known good structures of the clock factories. An oscillator that is not run through a clock factory to create a qualified clock requires special treatment. Figure 9 shows a block diagram of a sample clock factory module.

Figure 9 Clock Factory Block Diagram



The elements within a clock factory are shown in more detail in Figure 10.

Figure 10 Clock Factory Elements



The PGC contains stackable dividers with divisors ranging from 1 to 8. The IDM provides an insertion delay in order to match across clock domains. The insertion delay ranges from 0 to 2 ns with a 50 ps granularity. The RPC provides power control management. The BPC provides buffer tree management. The RGC provides reset generation control for the PGC clock domain. Clock n is the predistributed clock or clock legs, if BPC is used. Reset n is the reset signal for clock domain n.

The GenClock tool facilitates the fulfillment of specific clocking requirements using the clock factory component elements, and also facilitates accounting for the effects that occur when specific clocking options are specified. The key features of the GenClock tool are:

- Fixed 50/50 duty cycle output
- Fixed active edge (positive)
- No user-varied insertion delay/skew relationships
- Fixed reset scheme
  - Asynchronous assert/synchronous removal
  - Logic or external pin triggered

GenClock collects the set of clock factory elements that are requested in the customer configuration specification and assembles the elements so that they can be independently floorplanned and placed.

3 Library Elements

The principal goal of the RapidChip technology is to ensure a repeatable and predictable design flow that accelerates the design process and avoids the common pitfalls of deep submicron design. In common with ASIC design practices, design source files for a RapidChip project are captured in RTL form. The RTL is synthesized from a library of primitives using EDA tools to create a netlist that conforms to timing and certain other constraints.

The G12R library of logic primitives extends to over 400 members, covering simple and complex gates, multiplexers, and flip-flops. It is not within the scope of this document to detail the characteristics of the library itself.

However, to ensure the goals are met, certain constraints are placed on the performance scope of customer logic. RapidSlice platforms that use the G12R library have a predetermined maximum clock speed of 166 MHz for user logic. At this frequency, synthesis tools can implement approximately 20 levels of logic between successive clock edges. Faster operation is possible, for example, with Firm IP block layouts. However, for user logic, this approach comes at the expense of less predictable design time (because the block requires optimization and a dedicated layout) and increased NRE.

3.1 Complementary CoreWare Library

The goal of custom IC design is to create specific circuitry that meets unique system requirements. However, many functions within a custom IC, such as memory interfaces, link layers, controllers, and embedded microprocessors, can be standardized to ensure hardware/software interoperability within a system. Such functions are available through the LSI Logic CoreWare library of standardized IP blocks.

The LSI Logic RapidChip program offers productized bundles of CoreWare functions that address the implementation needs for many target applications. These provide IC designers with a substantial head start on a custom IC design by eliminating the burden of designing and integrating multiple CoreWare blocks that might not provide unique differentiation to a system but are still essential to its operation.

4 Design Tools

This section describes the design flow process for creating a RapidChip device and defines the RTL generation tools that are used in this process.

4.1 Design Flow

The following steps summarize the flow required to create a RapidChip device from an RC1800 Foundation Slice.

Step 1. Select the slice that most closely meets the end-system requirements. If the required slice does not exist, LSI Logic Corporation can work with the customer to develop a customer-specific slice.

Step 2. Select the application-specific CoreWare functions that meet the end-system requirements. Additional configurations of application-optimized CoreWare functions can be developed if the available RapidSlice options do not meet the end-system needs.

Step 3. Complete the design by adding customer-specific functionality.

The design flow described above is supported by its own methodology and tools, which accelerate design times using a predictable design process. This incorporates best-in-class third-party EDA tools and RapidChip specific automation tools for the generation of design structures. Rules and constraints guide designers through the RapidChip design process to ensure predictable results and reduced design times when compared to fully optimized ASICs.

4.2 RTL Generation Tools

The RapidChip technology uses RTL generation tools to create design structures for the implementation of a custom IC design. Based on user inputs, these tools automatically generate clock, memory, test, and I/O structures, relieving the design team from more mundane design tasks and dramatically reducing the overall manpower resource required for the design of custom high-performance ICs. Additionally, these structures are

"correct by construction" and are optimized to ensure ease of implementation during the physical design phase.

A brief description of the key generation tools is provided below:

- *GenMem* implements the memory on RapidSlice platforms based on user requirements. It uses a combination of R-Cell and diffused memories. In addition to allocating diffused memories, GenMem creates memories using Transistor-Fabric R-Cells where needed (typically for smaller memory blocks). GenMem also creates the necessary BIST test structures for all memories in the design.
- *GenIO* implements the I/Os on a RapidSlice platform based on the user-defined requirements. GenIO also adds the JTAG structures for boundary test and provides SSO analysis.
- *GenClock* creates user-defined clock networks based on sets of requirements. Clock circuits are the most timing-critical, layout-sensitive structures within any custom logic design. Automated creation of clock factory structures also takes into account the requirements for controlling the clock during the testing of the device.
- *GenTest* implements the test structures for the logic design and connects the MemBIST, JTAG, and clock factory structures to the TAP controller.

5 Packaging

All RC1800 Foundation Slices are available with the option of a high-performance, multilayer flip-chip package. These packages use a 1 mm pitch solder ball array to maximize I/O count while reducing package body size.

The design and construction of these packages provide a highly optimized electrical environment and excellent thermal characteristics for the most demanding of applications. With multiple independent low-inductance power and ground domains, these packages are optimized to reduce VDD/VSS path inductance, signal I/O path inductance, and signal-to-signal crosstalk, resulting in superior signal integrity. 100% differential pair routing for I/Os with a Z_0 of 50-55 ohms provides a "no compromises" environment for operating multiple high-performance SERDES at the maximum data rates of 3.1875 GHz. Configurable I/O

logic also can utilize differential pairs as single-ended transmission lines with a Z_0 of 100 ohms

To simplify the task of PCB design, solder ball layouts have been optimized by placing the I/Os in columns between VDD/VSS, which allows for efficient escape routing with fewer signal layers when using conventional PCB geometries.

5.1 Thermal Design Considerations

Packaging solutions for RC1800 Foundation Slices also are specified for maximum thermal performance. With the die attached directly to an integrated copper heat spreader, the lower junction-to-case thermal resistances ensure that RC1800 applications can maximize thermal dissipation and reduce constraints on airflow or heat-sink performance. Table 7 lists the thermal data for the seven slice FC-BGA packages.

Table 7 Slice Package Thermal Characteristics

Slice	Ball Count	Body Size	Theta JC[1]	Theta JA (0 m/s)	Theta JMA (1 m/s)	Theta JMA (2 m/s)
RC1810-FC544	544	27 mm	1.14	11.3	9.0	7.9
RC1820-FC736	736	31 mm	0.90	10.5	8.4	7.4
RC1830-FC788	788	31 mm	0.84	10.5	8.3	7.4
RC1840-FC960	960	35 mm	0.70	9.7	7.7	6.8
RC1845-FC960	960	35 mm	0.71	9.6	7.7	6.8
RC1850-FC1157/ RC1860-FC1157	1157	40 mm	0.60	8.7	7.0	6.2

1. Thermal data generated using EIA/JESD51 specifications.

Under standard conditions, the power that a package can dissipate (P) is calculated from:

- $P = (T_{Junction} - T_{Ambient}) / \theta_{JA}$ At natural convection, $V_{air} = 0$ m/s
- $P = (T_{Junction} - T_{Ambient}) / \theta_{JMA}$ At forced convection, $V_{air} > 0$m/s

P_{max} increases as θ_{JA} decreases and as the difference between $T_{Junction}$ and $T_{Ambient}$ increases. The maximum recommended $T_{Junction}$ for customer applications is 115 ˚C. Increasing the airflow across a package

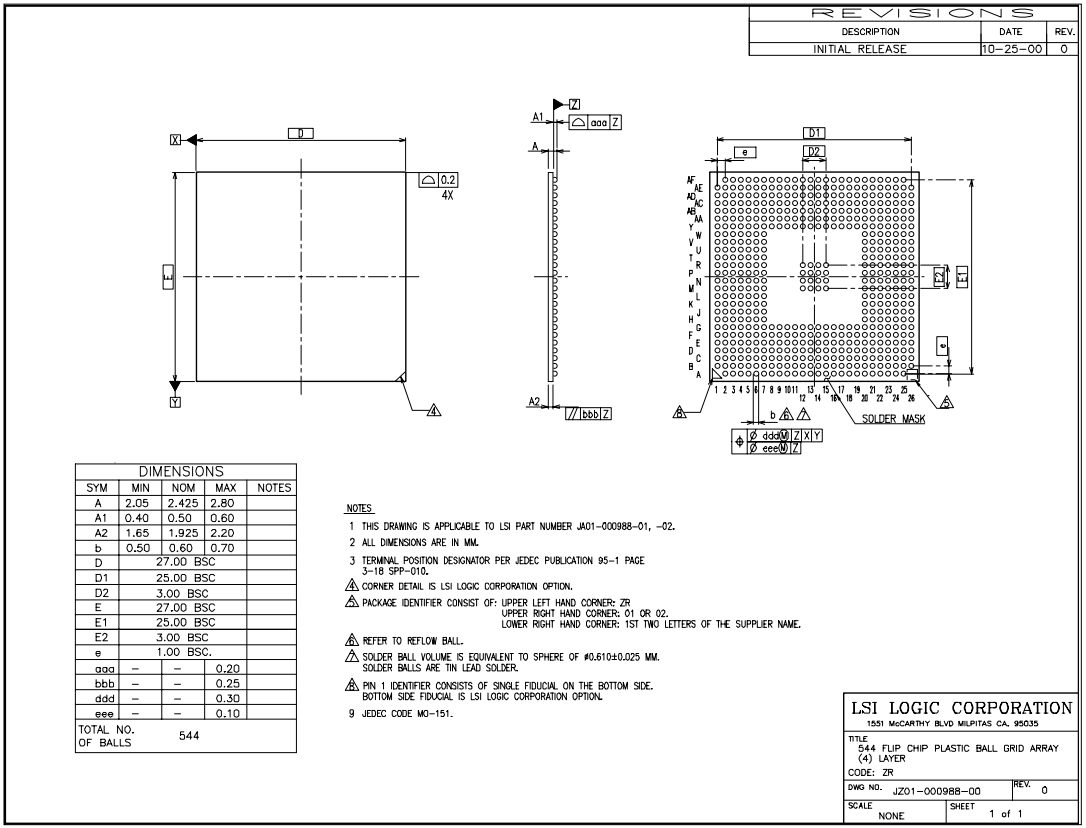
lowers its θ_{JMA} value. θ_{JMA} can be further reduced by attaching a heat sink to the surface of the package.

5.2 Package Outline Drawings

The following figures provide outline drawings of the available FC-BGA packages for the RC1800 Foundation Slices:

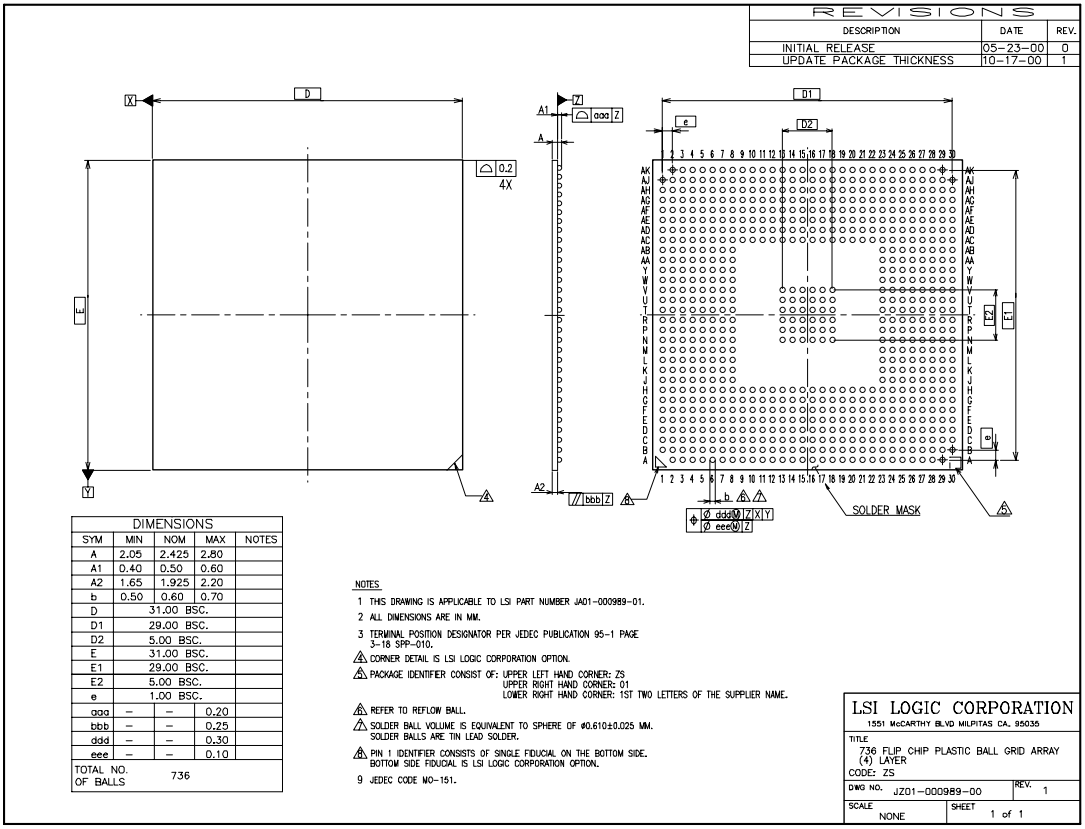
- Figure 11, RC1810-FC544 544-pin FPBGA Mechanical Drawing
- Figure 12, RC1820-FC736 736-pin FPBGA Mechanical Drawing
- Figure 13, RC1830-FC788 788-pin FPBGA Mechanical Drawing
- Figure 14, RC1840-FC960 960-pin FPBGA Mechanical Drawing
- Figure 15, RC1845-FC960 960-pin FPBGA Mechanical Drawing
- Figure 16, RC1850-FC1157/RC1860-FC1157 1157-pin FPBGA Mechanical Drawing

Figure 11 RC1810-FC544 544-pin FPBGA Mechanical Drawing



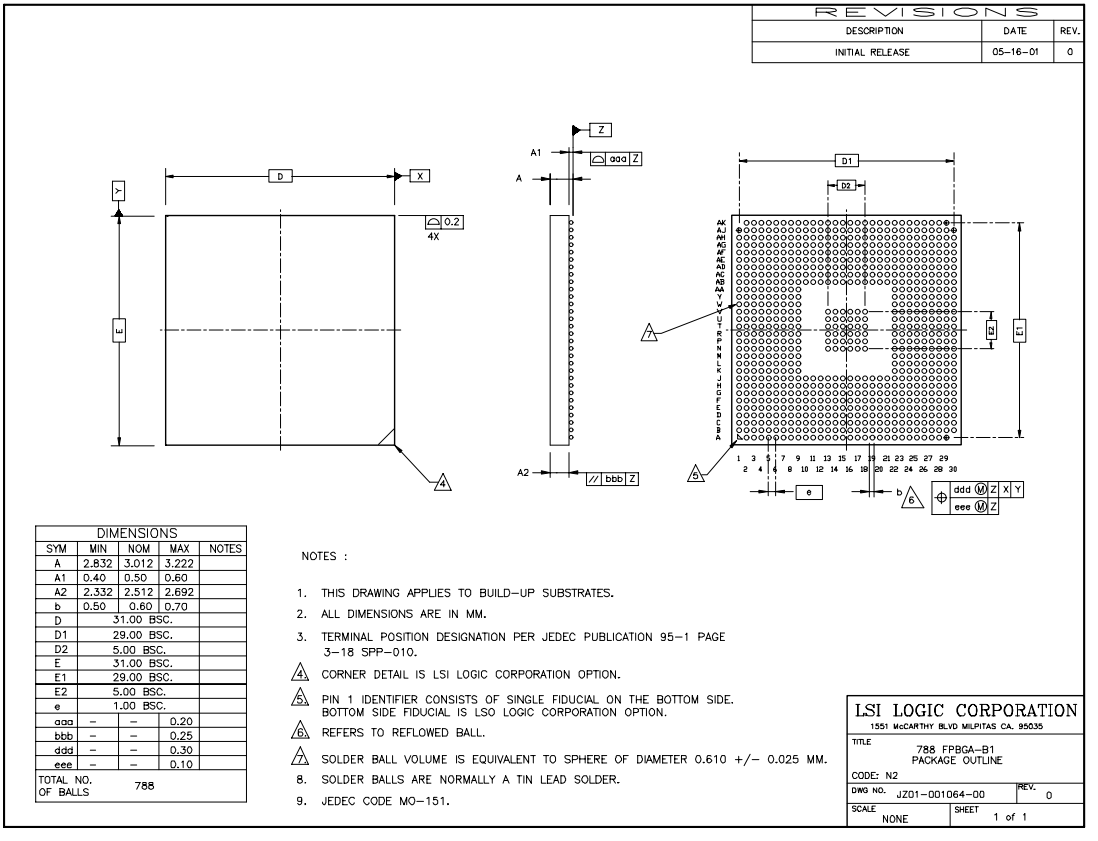
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic sales representative.**

Figure 12 RC1820-FC736 736-pin FPBGA Mechanical Drawing



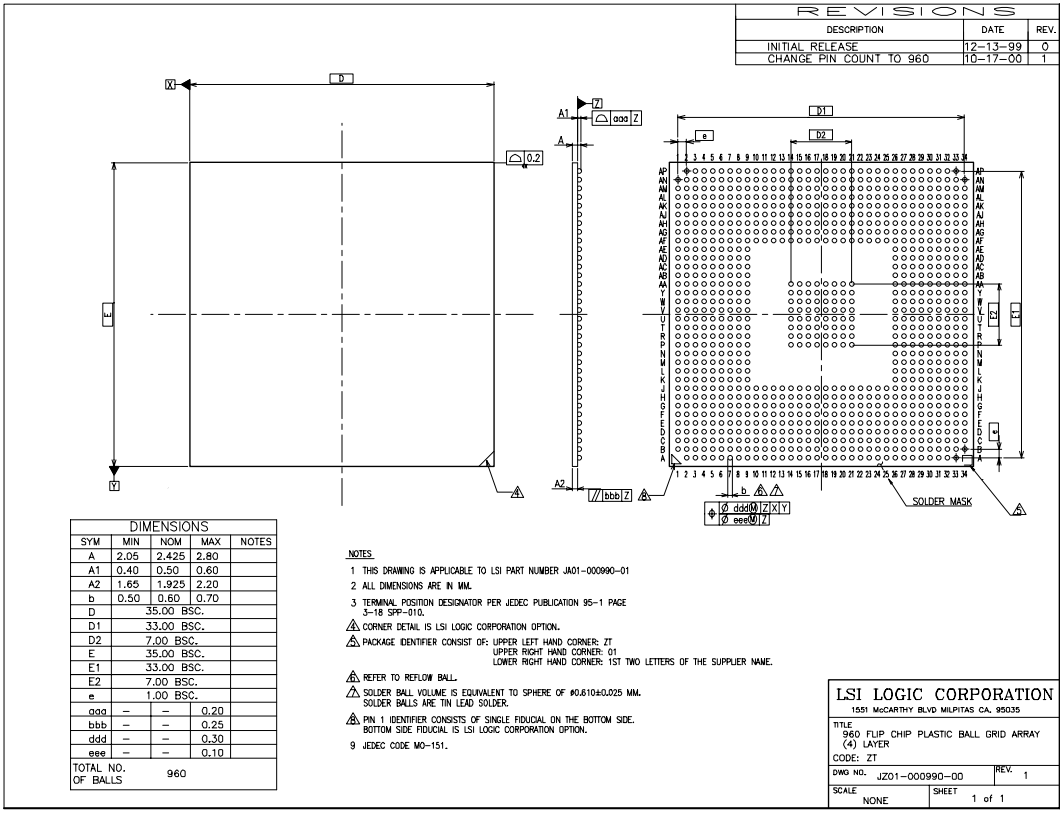
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic sales representative.**

Figure 13 RC1830-FC788 788-pin FPBGA Mechanical Drawing



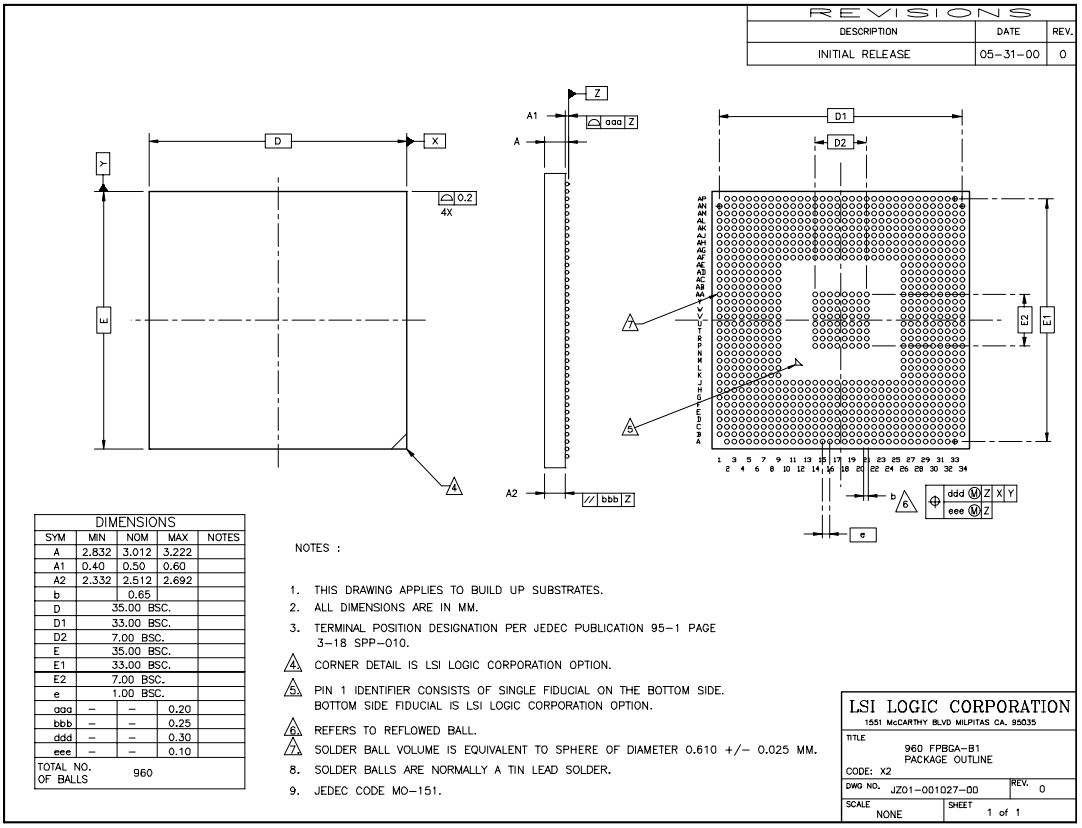
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic sales representative.**

Figure 14 RC1840-FC960 960-pin FPBGA Mechanical Drawing



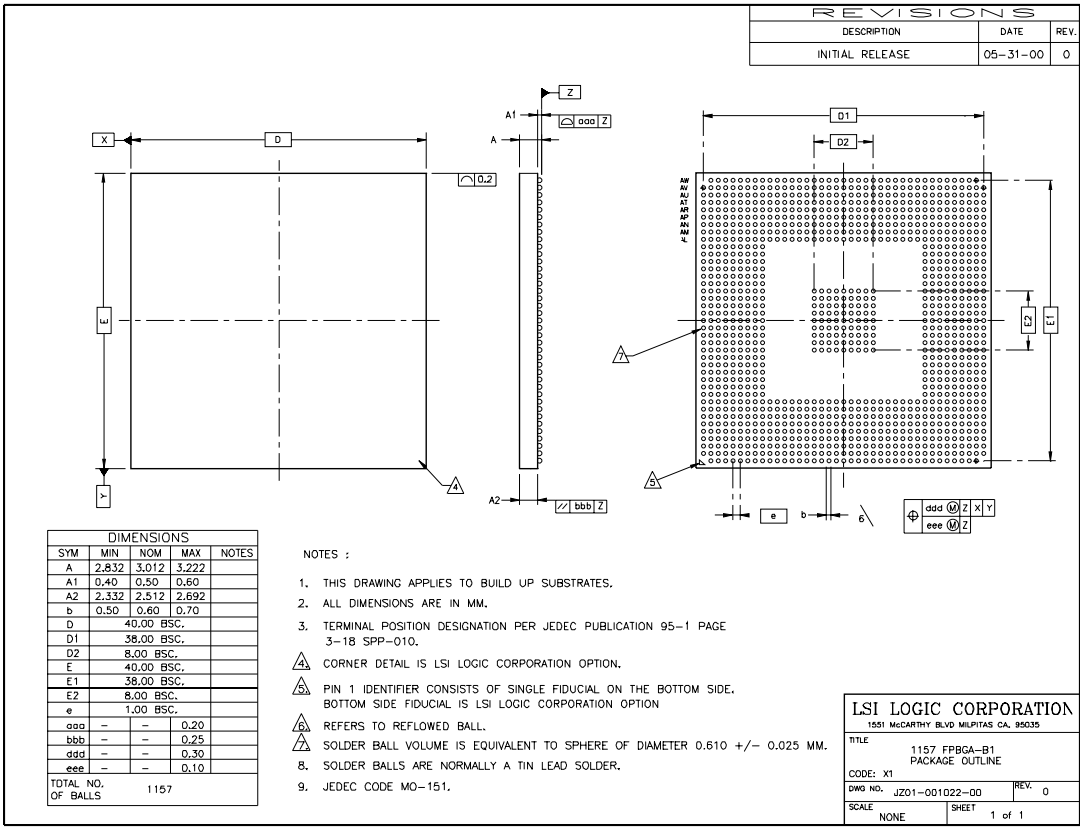
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic sales representative.**

Figure 15 RC1845-FC960 960-pin FPBGA Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic sales representative.**

Figure 16 RC1850-FC1157/RC1860-FC1157 1157-pin FPBGA Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic sales representative.**

6 Specifications

6.1 Recommended Operating Conditions

Table 8 gives the recommended operating conditions for the RC1800 slices. Operation beyond these limits may impair the useful life of the device.

Table 8 Recommended Operating Conditions

Parameter	Symbol	Limits[1]			Unit
		Min	Typ	Max	
DC supply voltage[2]	V_{DD}	1.62	1.80	1.89	V
Operating junction temperature range	T_J	-40	25	+115	˚C
GigaBlaze SERDES Transceiver					
DC supply voltage	V_{DDG}	1.71	1.80	1.89	V
Operating junction temperature range	T_{JG}	0[3]			˚C

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, may result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions.
2. Core supply voltage (1.8 V nominal).
3. GigaBlaze SERDES transceivers are specified for a minimum T_{JG} of 0 ˚C. Upper limits are per RC1800 general recommendations above.

6.2 DC Electrical Characteristics

TBD

6.3 AC Timing

TBD