

**128K x 32, 128K x 36 and 256K x 18
 PIPELINE 'NO WAIT' STATE BUS SRAM**

NOVEMBER 2002

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining for TQFP
- Power Down mode
- Common data inputs and data outputs
- $\overline{\text{CKE}}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP and 119 PBGA packages
- Single +3.3V power supply ($\pm 5\%$)
- NP Version: 3.3V I/O Supply Voltage
- NLP Version: 2.5V I/O Supply Voltage
- Industrial temperature available

DESCRIPTION

The 4 Meg 'NP' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for network and communications customers. They are organized as 131,072 words by 32 bits, 131,072 words by 36 bits and 262,144 words by 18 bits, fabricated with *ISSI's* advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{\text{CKE}}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{\text{WE}}$ is LOW. Separate byte enables allow individual bytes to be written.

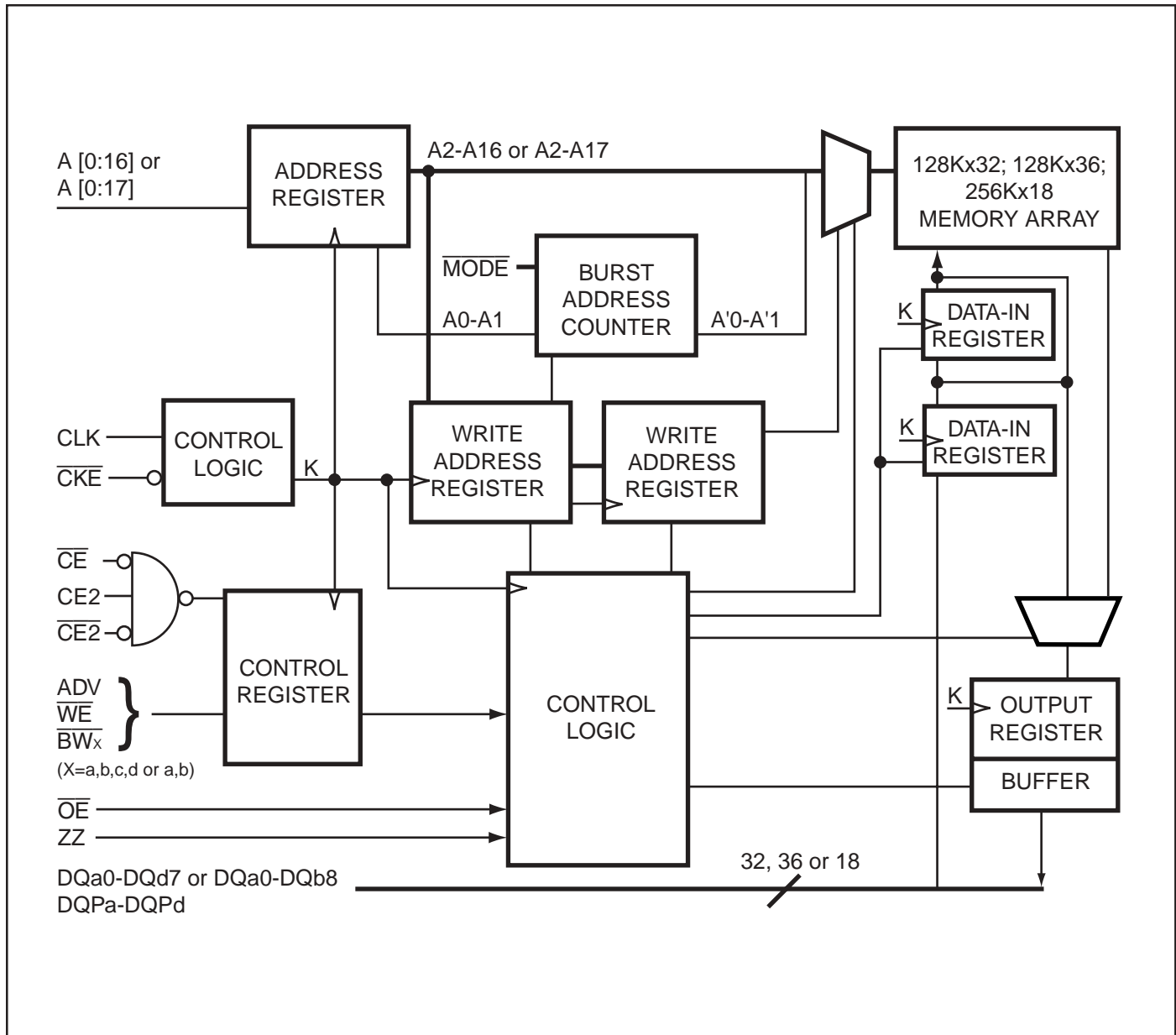
A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

Symbol	Parameter	-150	-133	-100	Units
t _{kQ}	Clock Access Time	3.8	4.2	5	ns
t _{kC}	Cycle Time	6.7	7.5	10	ns
	Frequency	150	133	100	MHz

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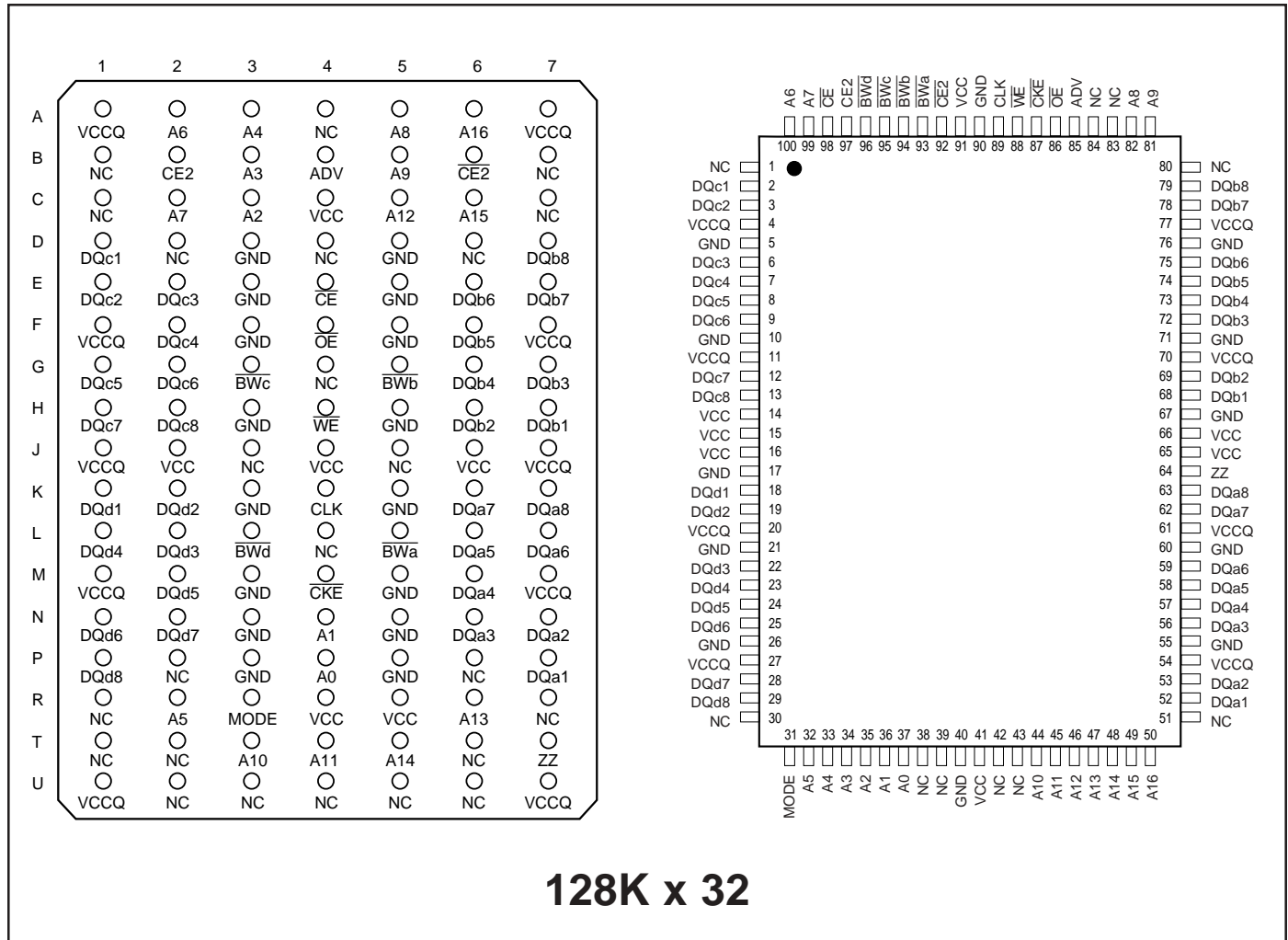
BLOCK DIAGRAM



PIN CONFIGURATION

119-pin PBGA (Top View)

100-Pin TQFP

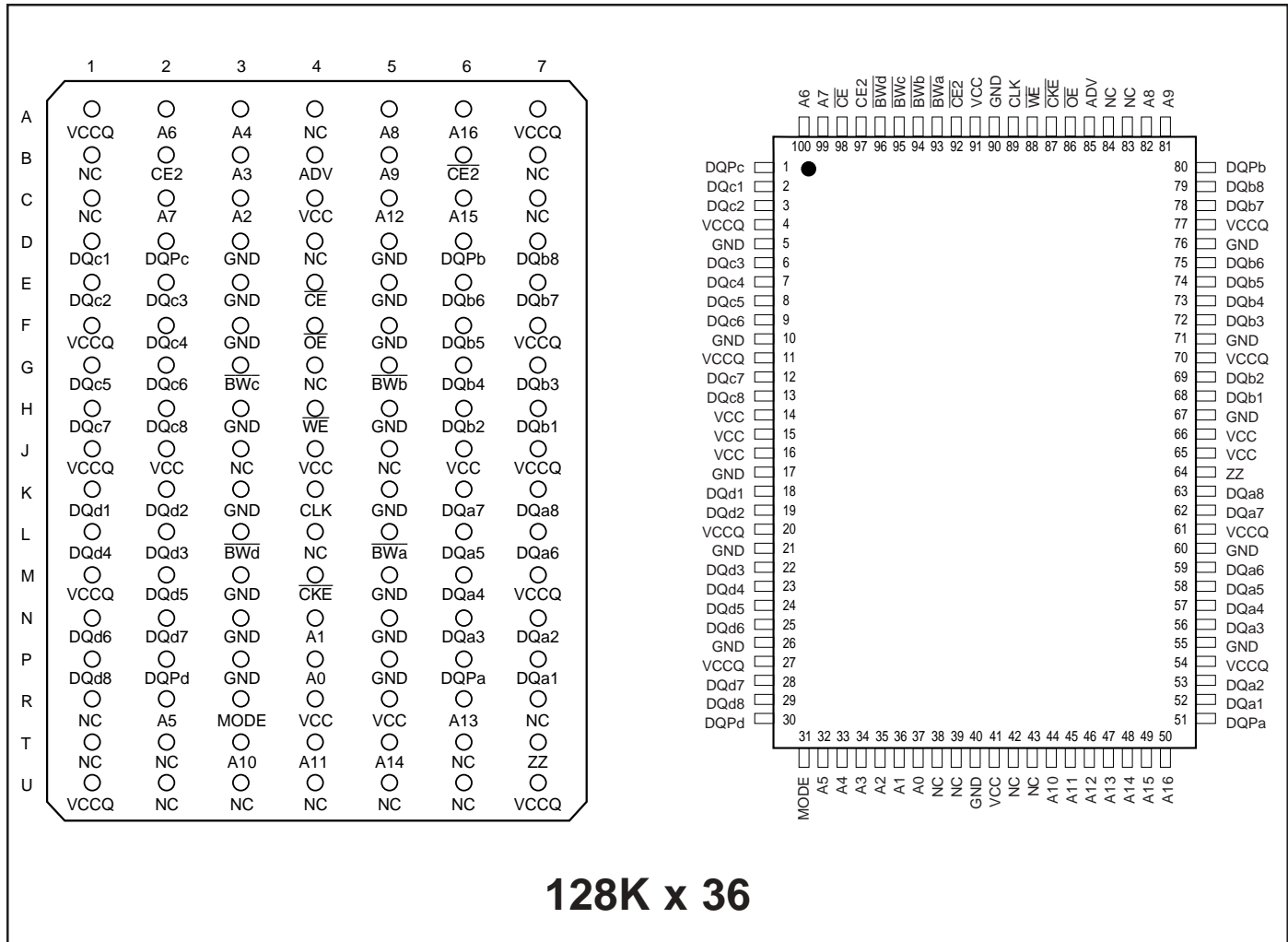


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.	\overline{CE} , $\overline{CE2}$, CE2	Synchronous Chip Enable
A2-A16	Synchronous Address Inputs	\overline{OE}	Output Enable
CLK	Synchronous Clock	DQa-DQd	Synchronous Data Input/Output
ADV	Synchronous Burst Address Advance	MODE	Burst Sequence Mode Selection
\overline{BWA} - \overline{BWD}	Synchronous Byte Write Enable	Vcc	+3.3V Power Supply
\overline{WE}	Write Enable	GND	Ground
\overline{CKE}	Clock Enable	Vccq	Isolated Output Buffer Supply: +3.3V/2.5V
		ZZ	Snooze Enable

PIN CONFIGURATION
119-pin PBGA (Top View)

100-Pin TQFP



128K x 36

PIN DESCRIPTIONS

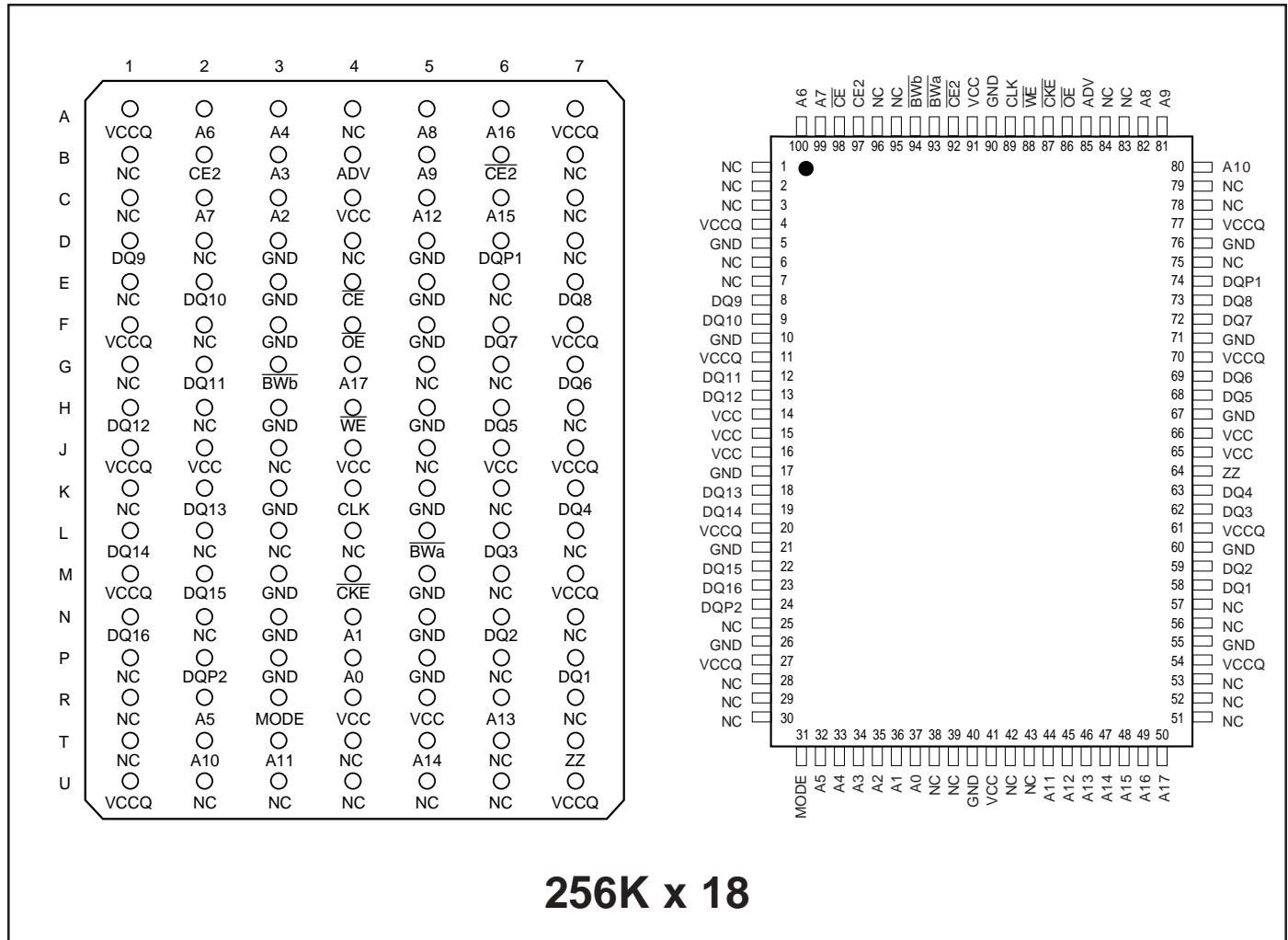
A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A16	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
\overline{BWA} - \overline{BWD}	Synchronous Byte Write Enable
\overline{WE}	Write Enable

\overline{CKE}	Clock Enable
\overline{CE} , $\overline{CE2}$, $\overline{CE2}$	Synchronous Chip Enable
\overline{OE}	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

119-pin PBGA (Top View) (B)

100-Pin TQFP

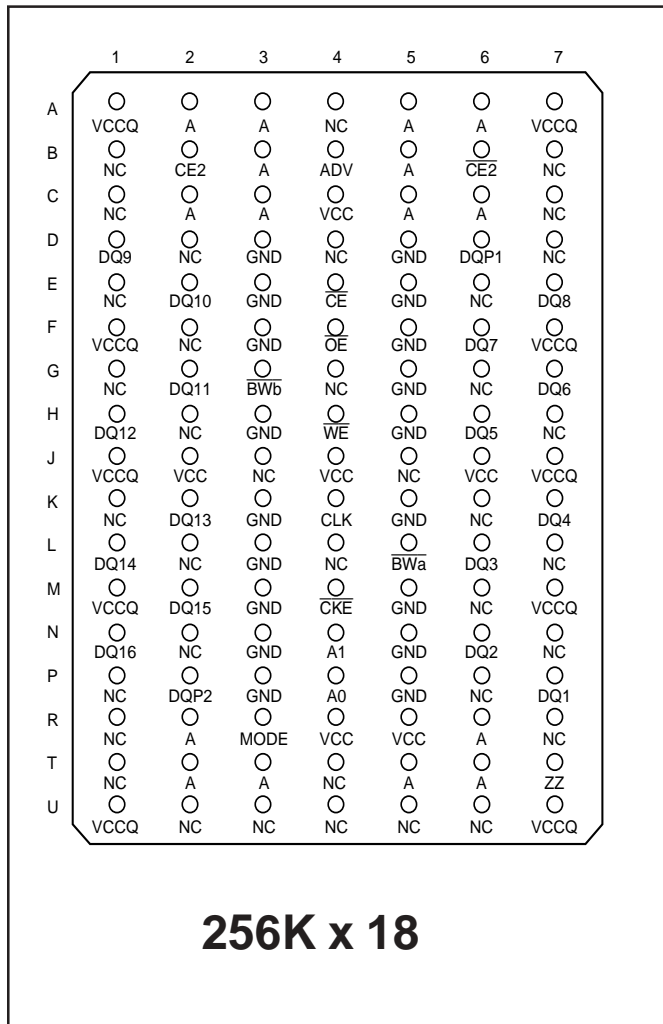


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.	\overline{CE} , CE2, $\overline{CE2}$	Synchronous Chip Enable
A2-A17	Synchronous Address Inputs	\overline{OE}	Output Enable
CLK	Synchronous Clock	DQ1-DQ16	Synchronous Data Input/Output
ADV	Synchronous Burst Address Advance	MODE	Burst Sequence Mode Selection
\overline{BWA} - \overline{BWB}	Synchronous Byte Write Enable	Vcc	+3.3V Power Supply
\overline{WE}	Write Enable	GND	Ground
\overline{CKE}	Clock Enable	Vccq	Isolated Output Buffer Supply: +3.3V/2.5V
		ZZ	Snooze Enable
		DQP1-DQP2	Parity Data I/O DQP1 is parity for DQ1-8; DQP2 is parity for DQ9-16

PIN CONFIGURATION

119-pin PBGA (Top View) (B2)

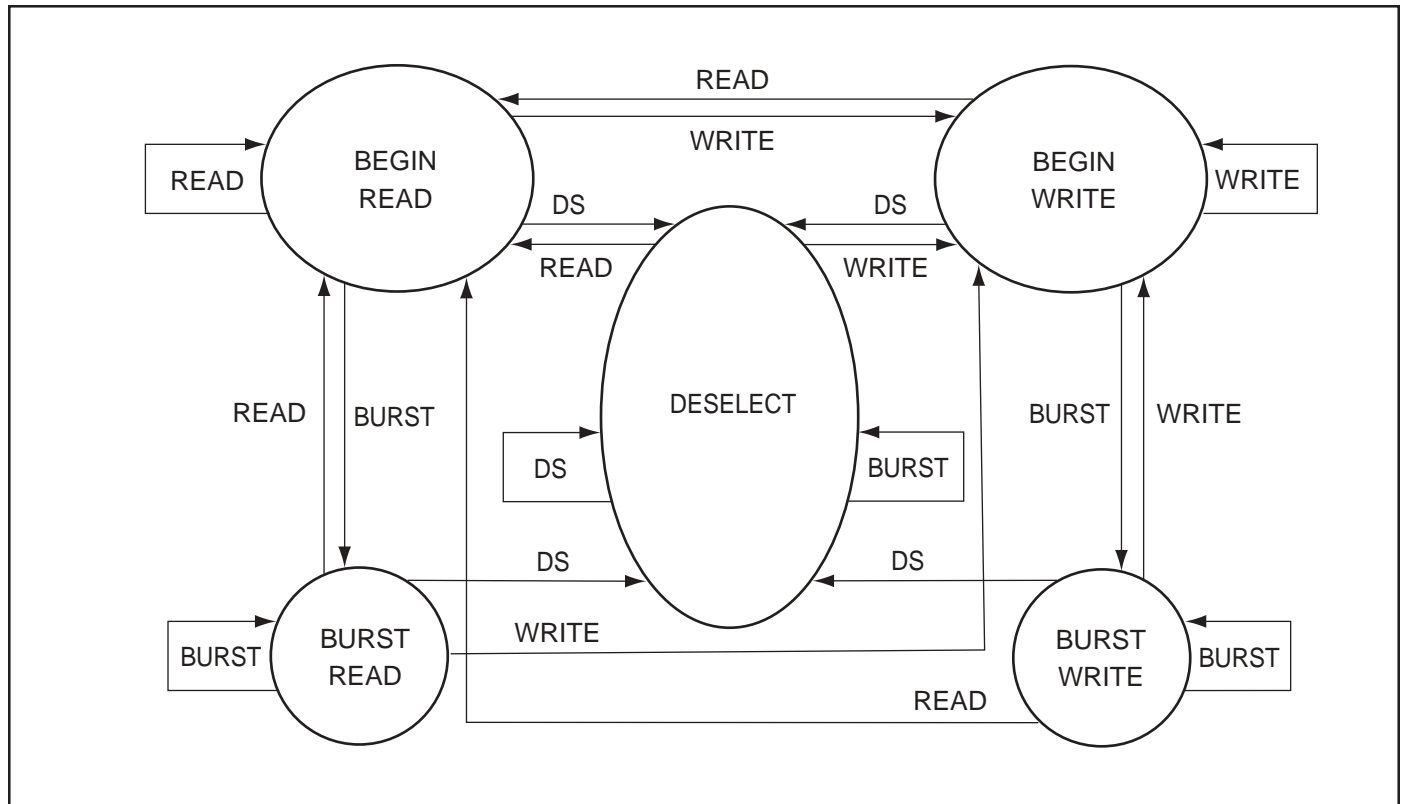


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
ADV	Synchronous Burst Address Advance
BW \bar{a} -BW \bar{b}	Synchronous Byte Write Enable
WE	Write Enable
CKE	Clock Enable

CE, CE2, CE $\bar{2}$	Synchronous Chip Enable
OE	Output Enable
DQ1-DQ16	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
Vcc	+3.3V Power Supply
GND	Ground
Vccq	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable
DQP1-DQP2	Parity Data I/O DQP1 is parity for DQ1-8; DQP2 is parity for DQ9-16

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE⁽¹⁾

Operation	Address Used	$\overline{CS1}$	CS2	$\overline{CS2}$	ADV	\overline{WE}	\overline{BWx}	\overline{OE}	\overline{CKE}	CLK
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:

- "X" means don't care.
- The rising edge of clock is symbolized by ↑
- A continue deselect cycle can only be entered if a deselect cycle is executed first.
- $\overline{WE} = L$ means Write operation in Write Truth Table.
 $\overline{WE} = H$ means Read operation in Write Truth Table.
- Operation finally depends on status of asynchronous pins (ZZ and \overline{OE}).

ASYNCHRONOUS TRUTH TABLE⁽¹⁾

Operation	ZZ	\overline{OE}	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with \overline{OE} , otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	\overline{WE}	\overline{BWa}	\overline{BWb}
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTEs	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x32/x36)

Operation	\overline{WE}	\overline{BWa}	\overline{BWb}	\overline{BWc}	\overline{BWd}
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

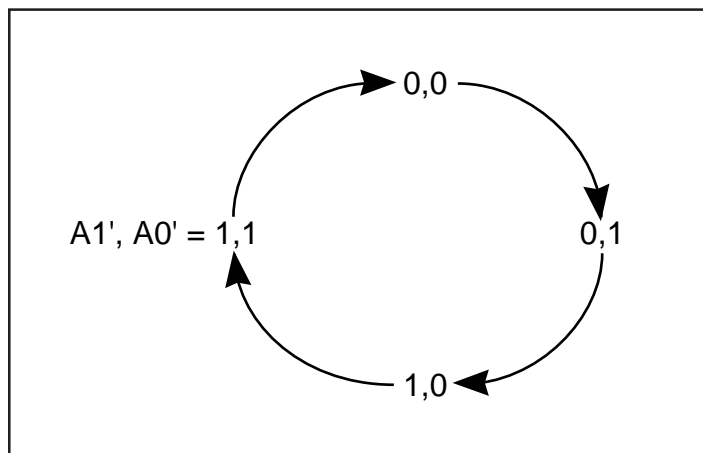
Notes:

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CC})

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾ (MODE = GND)

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	-0.5 to V _{CCQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	-0.3 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	DEVICE	V _{CC}	V _{CCQ}
Commercial	0°C to +70°C	61NPXXXXX	3.3V ± 5%	3.3V ± 5%
		61NLPXXXXX	3.3V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	61NPXXXXX	3.3V ± 5%	3.3V ± 5%
		61NLPXXXXX	3.3V ± 5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	2.5V		3.3V		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0 mA (3.3V V _{CCQ}) I _{OH} = 1.0 mA (2.5V V _{CCQ})	2.0	—	2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA (3.3V V _{CCQ}) I _{OL} = 1.0 mA (2.5V V _{CCQ})	—	0.4	—	0.4	V
V _{IH}	Input HIGH Voltage		1.7	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.7	-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC} ⁽¹⁾	-5	5	-5	5	µA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CCQ} , $\overline{OE} = V_I$	-5	5	-5	5	µA

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-150 MAX		-133 MAX		-100 MAX		Unit
			x18	x32/36	x18	x32/36	x18	x32/36	
I _{CC}	AC Operating Supply Current	Device Selected, Com. $\overline{OE} = V_{IH}$, ZZ ≤ V _{IL} , Ind. All Inputs ≤ 0.2V OR ≥ V _{CC} - 0.2V, Cycle Time ≥ t _{CC} min.	305	305	290	290	275	275	mA
I _{SB}	Standby Current TTL Input	Device Deselected, Com. V _{CC} = Max., Ind. All Inputs ≤ 0.2V OR ≥ V _{CC} - 0.2V, ZZ ≤ V _{IL} , f = Max.	90	90	80	80	70	70	mA
I _{SBI}	Standby Current CMOS Input	Device Deselected, Com. V _{CC} = Max., Ind. V _{IN} ≤ GND + 0.2V OR ≥ V _{CC} - 0.2V f = 0	10	10	10	10	10	10	mA

Note:

- MODE pin has an internal pullup and should be tied to V_{CC} or GND. It exhibits ±30 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{CC} - 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

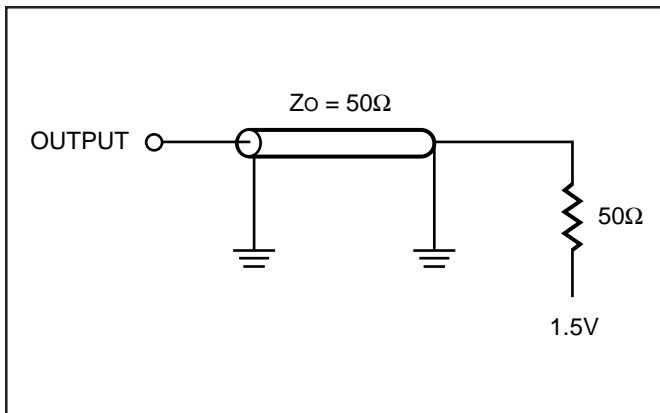


Figure 1

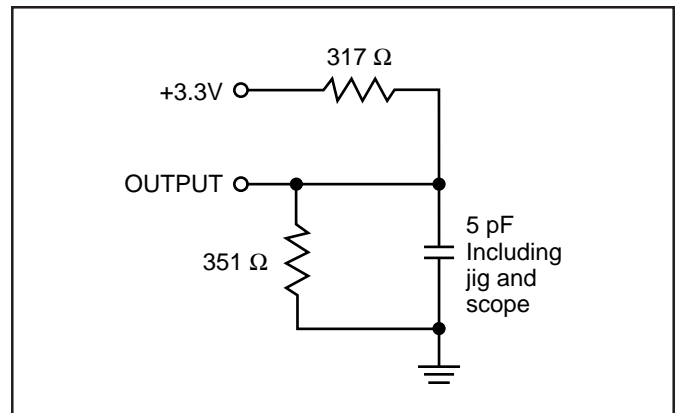


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

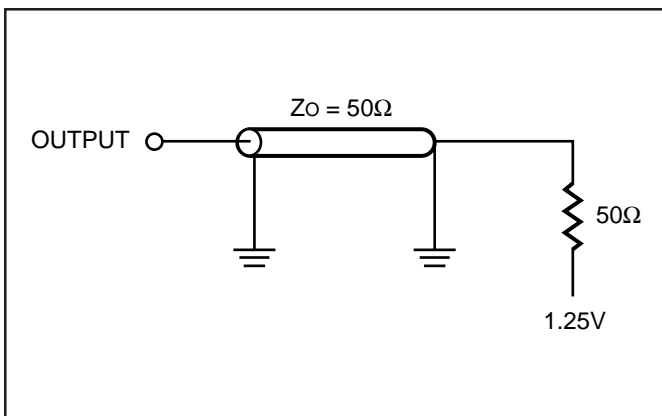


Figure 3

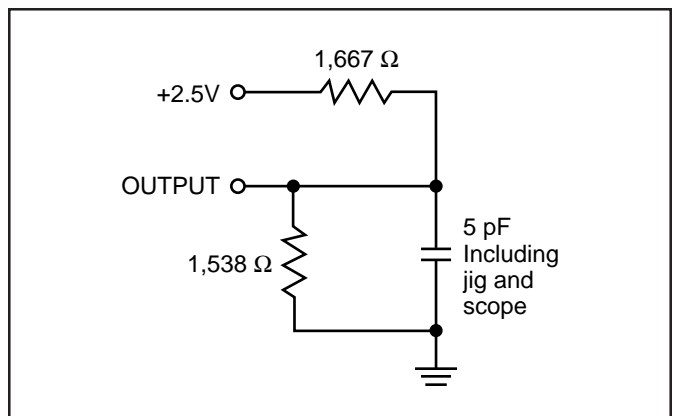


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-150		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fmax	Clock Frequency	—	150	—	133	—	100	MHz
t _κ	Cycle Time	6.7	—	7.5	—	10	—	ns
t _{κH}	Clock High Time	2.5	—	3	—	3	—	ns
t _{κL}	Clock Low Time	2.5	—	3	—	3	—	ns
t _{κQ}	Clock Access Time	—	3.8	—	4.2	—	5	ns
t _{κQX} ⁽²⁾	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	ns
t _{κQLZ} ^(2,3)	Clock High to Output Low-Z	0	—	0	—	0	—	ns
t _{κQHZ} ^(2,3)	Clock High to Output High-Z	—	3	—	3.5	—	3.5	ns
t _{OEQ}	Output Enable to Output Valid	—	3.8	—	4.2	—	5	ns
t _{OELZ} ^(2,3)	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t _{OEHZ} ^(2,3)	Output Disable to Output High-Z	—	3.5	—	3.5	—	3.5	ns
t _{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	ns
t _{WS}	Read/Write Setup Time	1.5	—	1.5	—	1.5	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	ns
t _{SE}	Clock Enable Setup Time	1.5	—	1.5	—	1.5	—	ns
t _{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	ns
t _{DS}	Data Setup Time	2.0	—	2.0	—	2.0	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{ADVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{DH}	Data Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{PDS}	ZZ High to Power Down	—	2	—	2	—	2	cyc
t _{PUS}	ZZ Low to Power Down	—	2	—	2	—	2	cyc

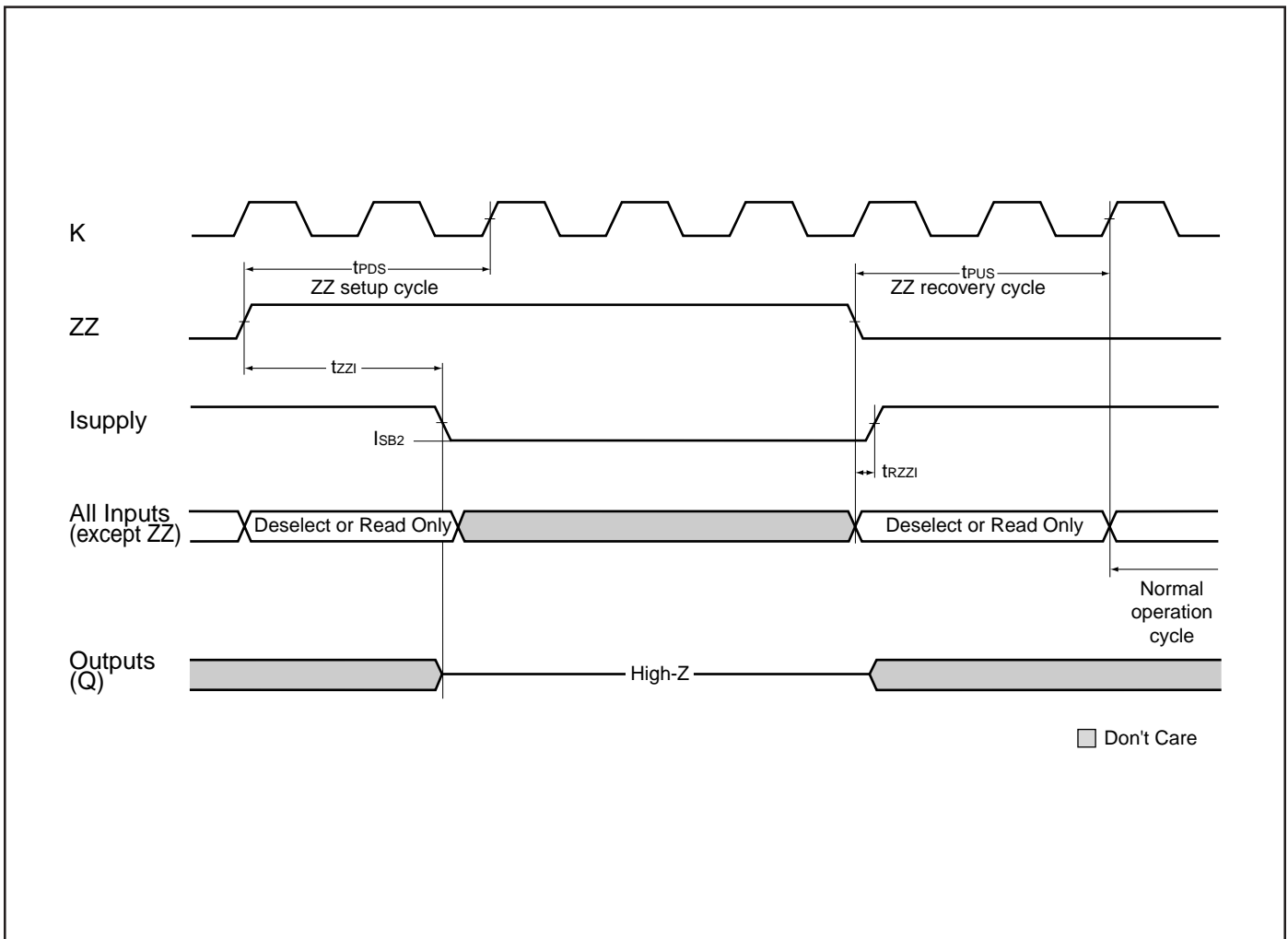
Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

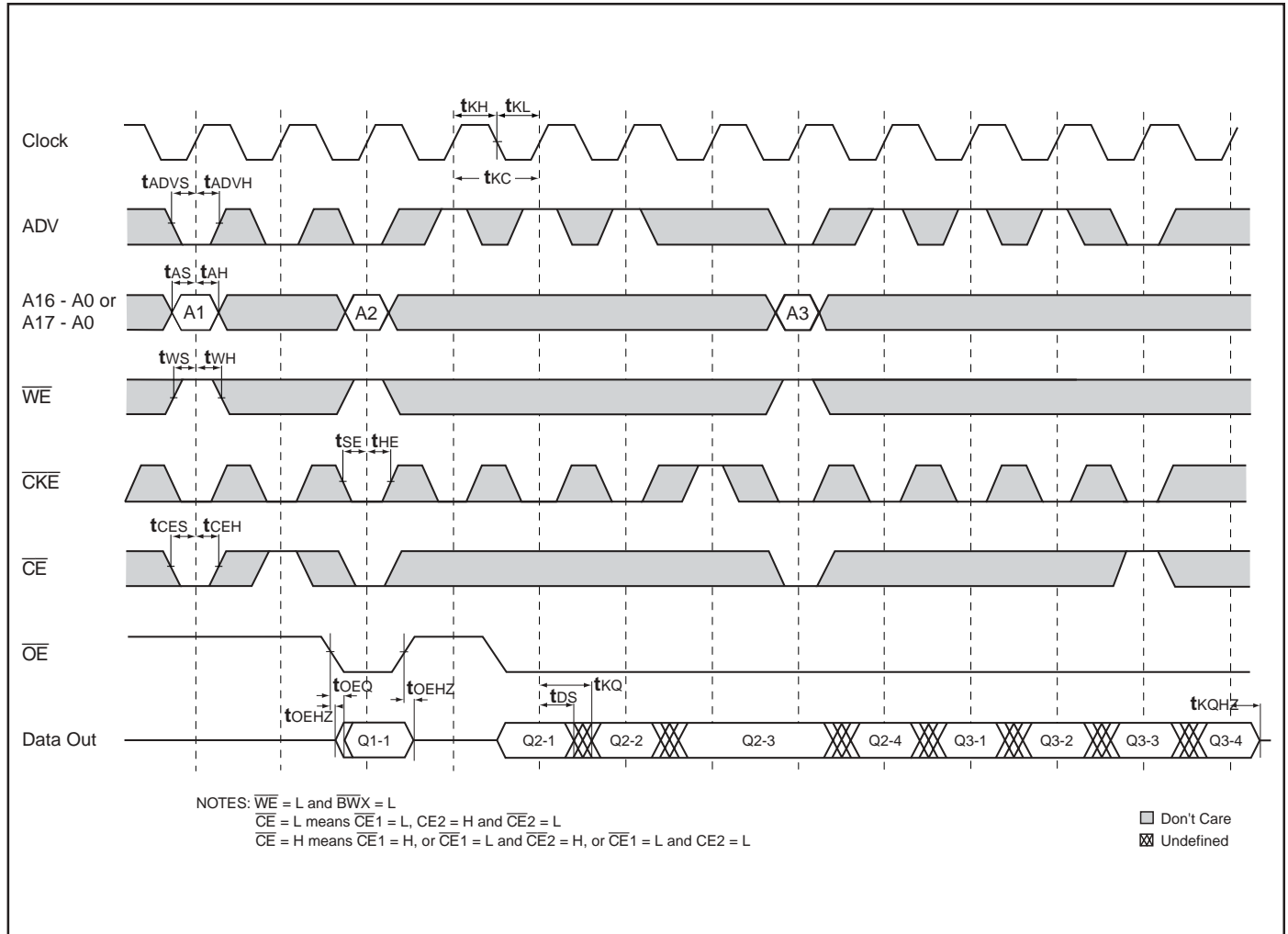
SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
ISB2	Current during SLEEP MODE	ZZ ≥ Vih		10	mA
tPDS	ZZ active to input ignored		2		cycle
tPUS	ZZ inactive to input sampled		2		cycle
tZZI	ZZ active to SLEEP current		2		cycle
tRZZI	ZZ inactive to exit SLEEP current		0		ns

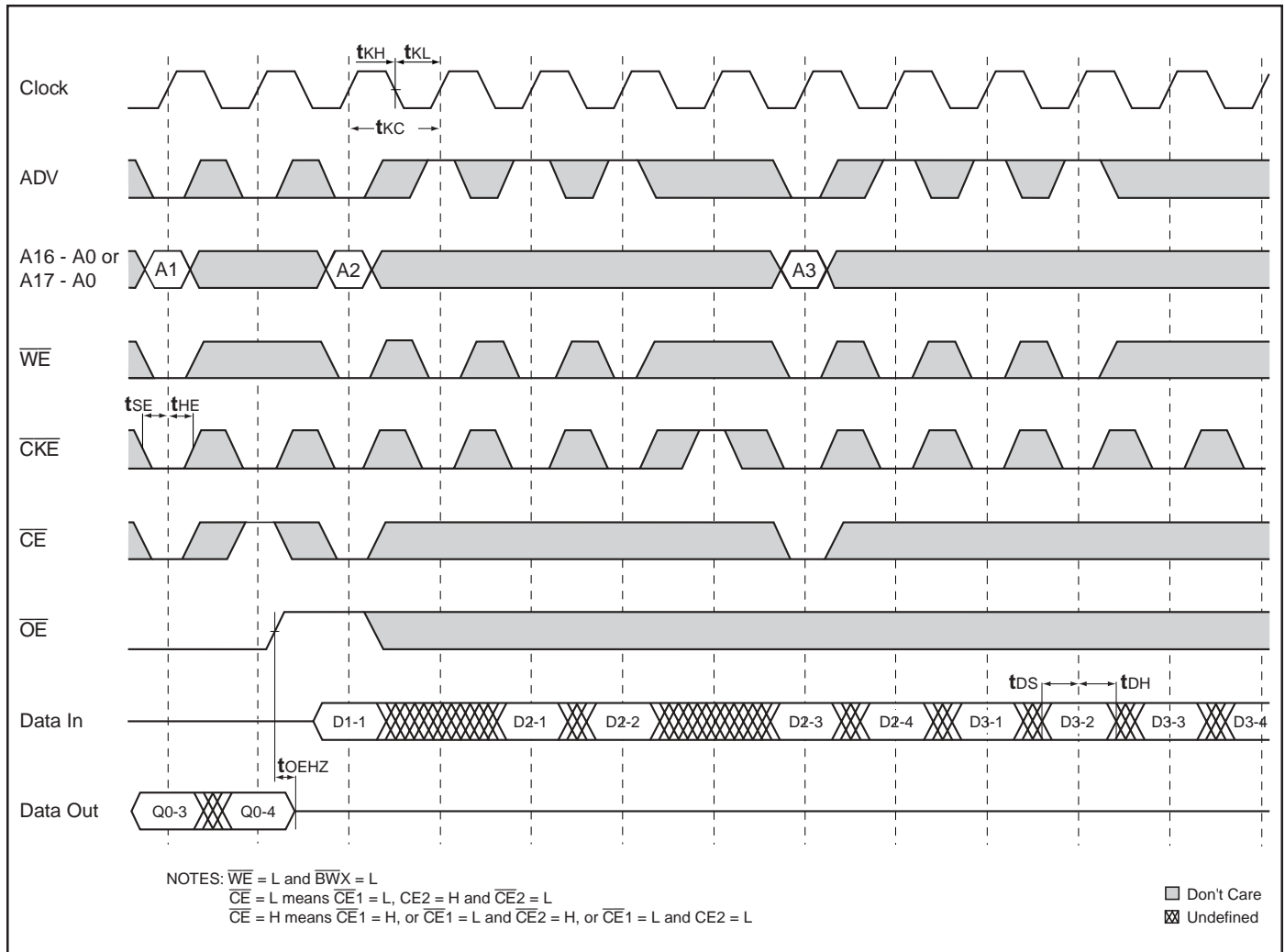
SLEEP MODE TIMING



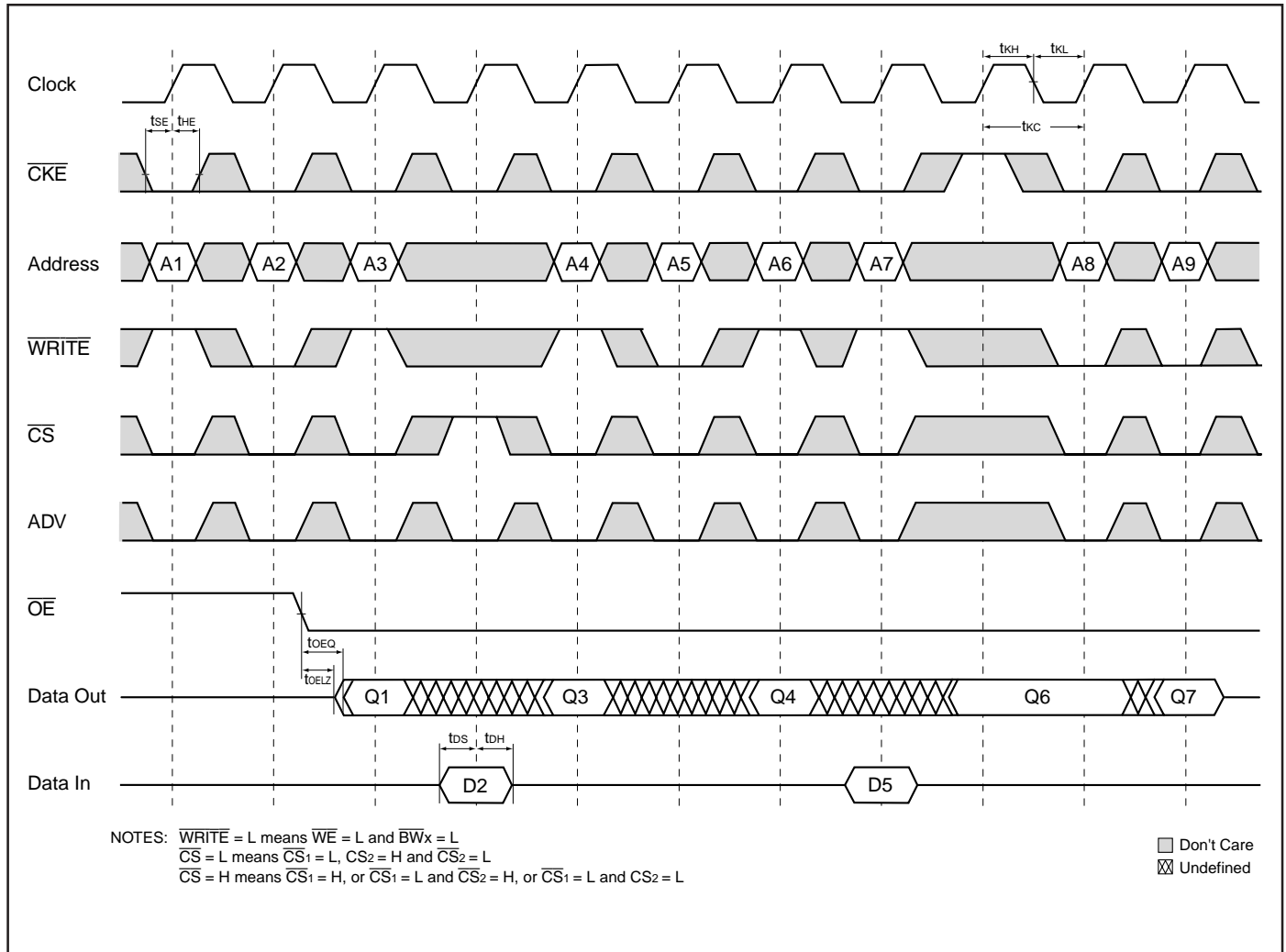
READ CYCLE TIMING



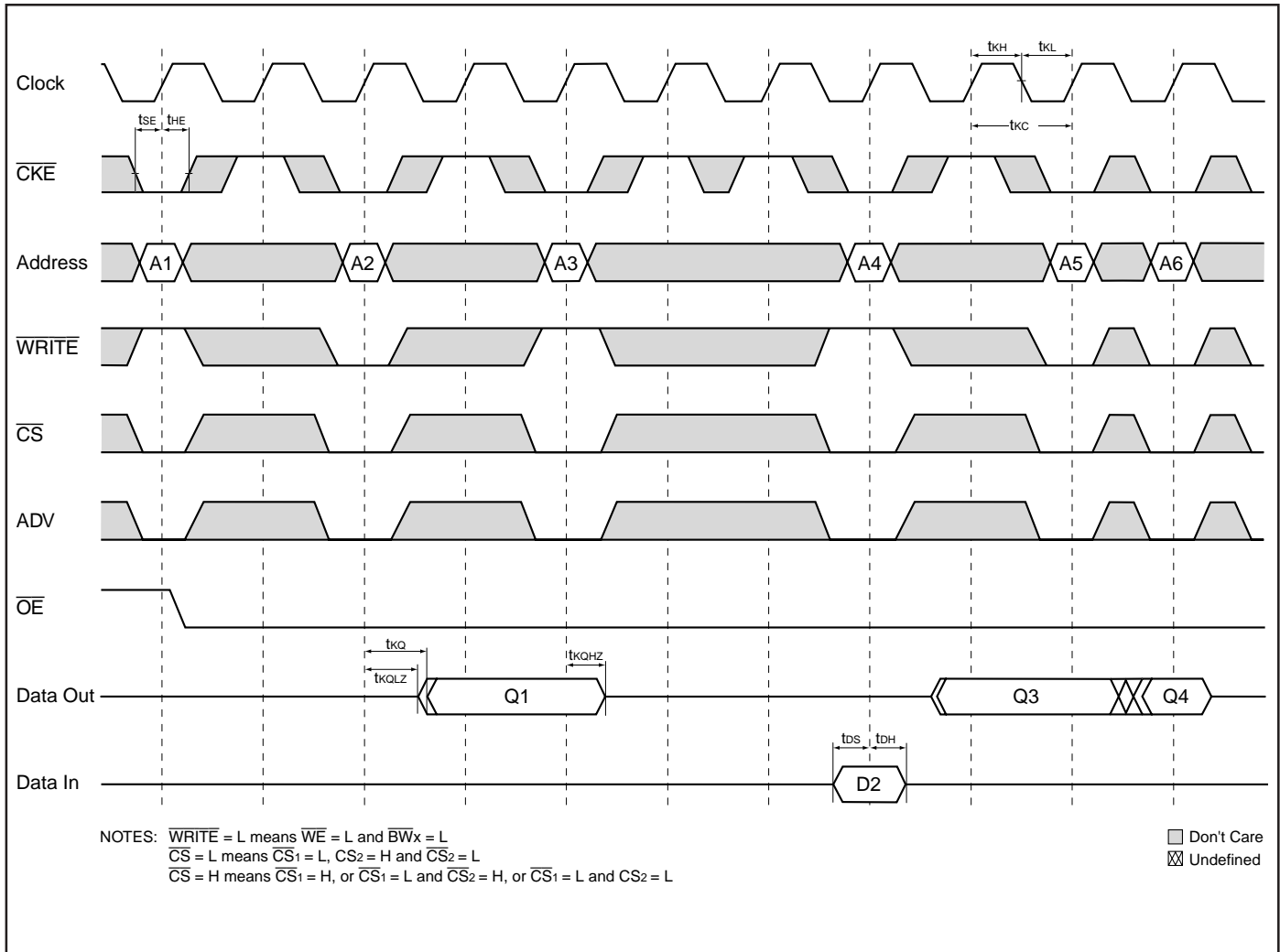
WRITE CYCLE TIMING



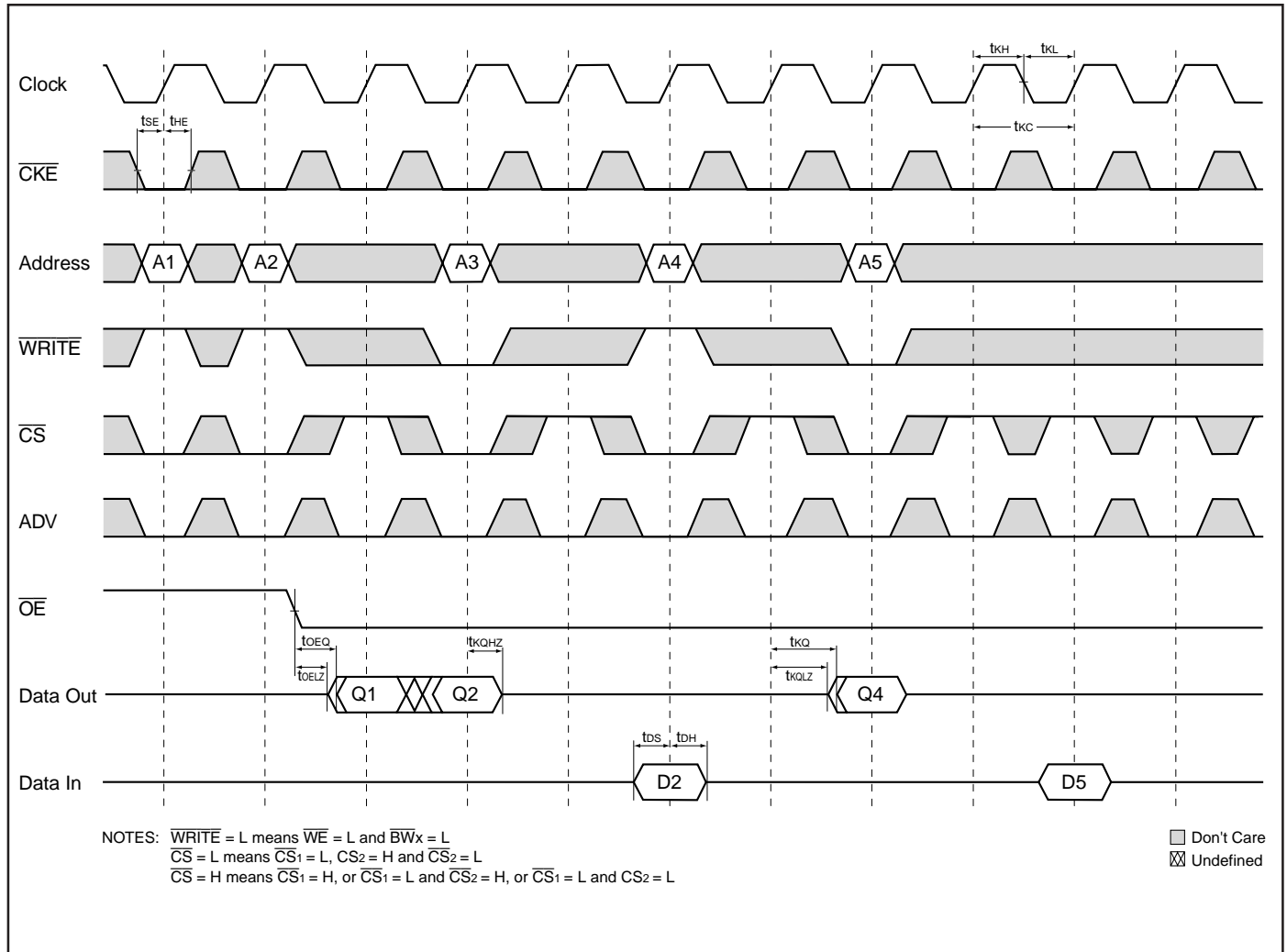
SINGLE READ/WRITE CYCLE TIMING



$\overline{\text{CKE}}$ OPERATION TIMING



\overline{CS} OPERATION TIMING



**ORDERING INFORMATION
 (61NPXXXXX)**

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
128Kx32		
150	IS61NP12832-150TQ	TQFP
133	IS61NP12832-133TQ	TQFP
100	IS61NP12832-100TQ	TQFP
128Kx36		
150	IS61NP12836-150TQ IS61NP12836-150B	TQFP PBGA
133	IS61NP12836-133TQ IS61NP12836-133B	TQFP PBGA
100	IS61NP12836-100TQ	TQFP
256Kx18		
150	IS61NP25618-150TQ IS61NP25618-150B2	TQFP PBGA
133	IS61NP25618-133TQ IS61NP25618-133B2	TQFP PBGA
100	IS61NP25618-100TQ	TQFP

Industrial Range: -40°C to +85°C

Frequency	Order Part Number	Package
128Kx32		
133	IS61NP12832-133TQI	TQFP
133	IS61NP12832-133BI	PBGA
128Kx36		
133	IS61NP12836-133TQI	TQFP
133	IS61NP12836-133BI	PBGA
256Kx18		
133	IS61NP25618-133TQI	TQFP
133	IS61NP25618-133B2I	PBGA

**ORDERING INFORMATION (61NL
 PXXXXX)**

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
128Kx32		
133	IS61NLP12832-133TQ IS61NLP12832-133B	TQFP PBGA
128Kx36		
133	IS61NLP12836-133TQ IS61NLP12836-133B	TQFP PBGA
150	IS61NLP12836-150TQ IS61NLP12836-150B	TQFP PBGA
256Kx18		
133	IS61NLP25618-133TQ IS61NLP25618-133B IS61NLP25618-133B2	TQFP PBGA PBGA
150	IS61NLP25618-150TQ IS61NLP25618-150B2	TQFP PBGA

Industrial Range: -40°C to +85°C

Frequency	Order Part Number	Package
128Kx32		
133	IS61NLP12832-133TQI	TQFP
128Kx36		
133	IS61NLP12836-133TQI	TQFP
133	IS61NLP12836-133BI	PBGA
256Kx18		
133	IS61NLP25618-133TQI	TQFP
133	IS61NLP25618-133B2I	PBGA