

256K x 32, 256K x 36, 512K x 18 SYNCHRONOUS FLOW-THROUGH STATIC RAM

OCTOBER 2002

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Power Supply
 - + 3.3V V_{DD}
 - + 3.3V or 2.5V V_{DDQ} (I/O)
- Snooze MODE for reduced-power standby
- T version (three chip selects)
- J version (PBGA Package with JTAG)
- D version (two chip selects)
- JTAG Boundary Scan for PBGA.

DESCRIPTION

The *ISSI* IS61LF25632, IS61LF25636, and IS61LF51218 are high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance and memories for communication and networking applications. The IS61LF25632 is organized as 262,144 words by 32 bits and the IS61LF25636 is organized as 262,144 words by 36 bits. The IS61LF51218 is organized as 524,288 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers that are controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable (BWE).input combined with one or more individual byte write signals (BWx). In addition, Global Write (GW) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either $\overline{\text{ADSP}}$ (Address Status Processor) or $\overline{\text{ADSC}}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{\text{ADV}}$ (burst address advance) input pin.

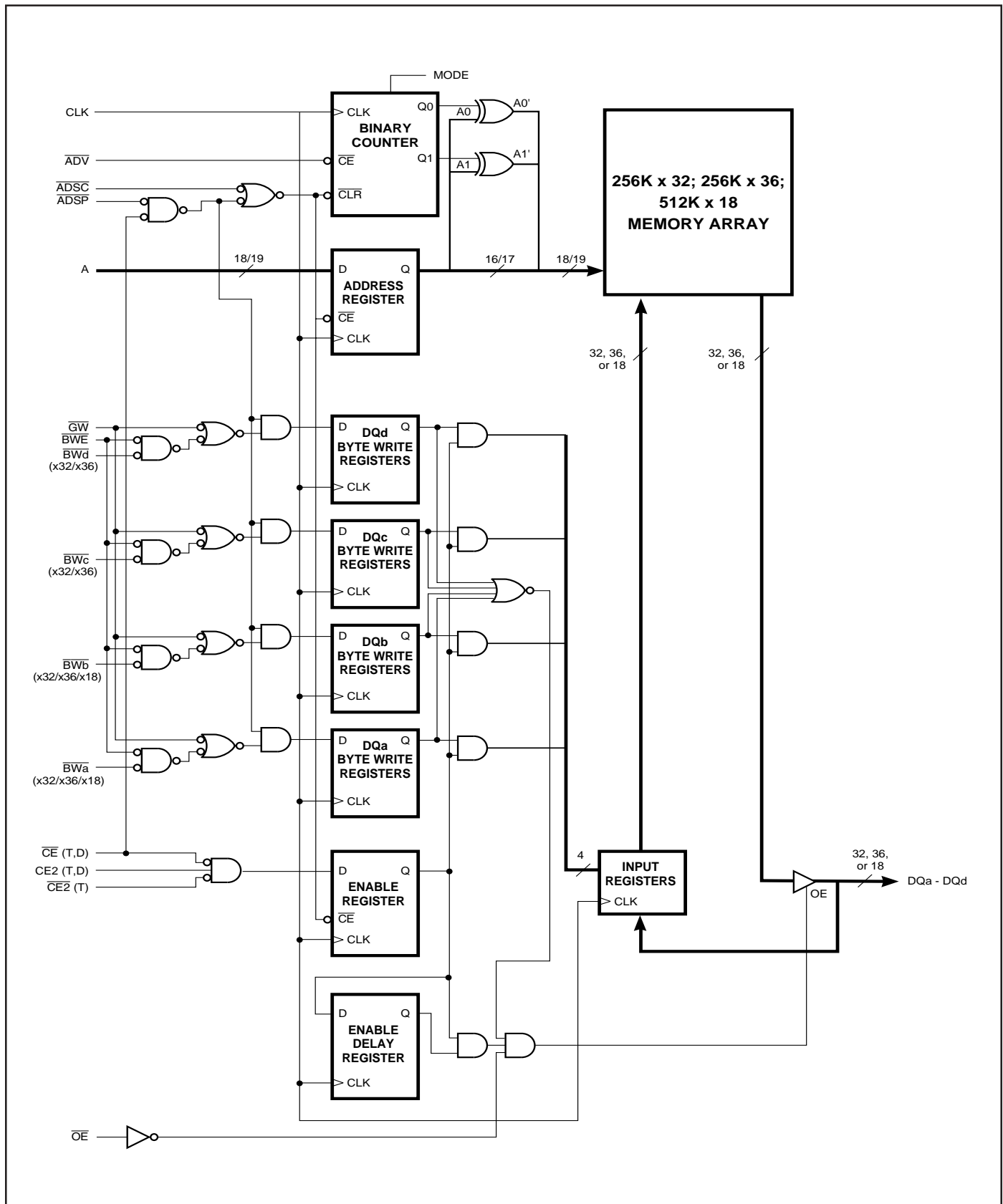
The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

Symbol	Parameter	6.5	7.5	Units
t _{KQ}	Clock Access Time	6.5	7.5	ns
t _{KC}	Cycle Time	7.5	8.5	ns
	Frequency	133	117	MHz

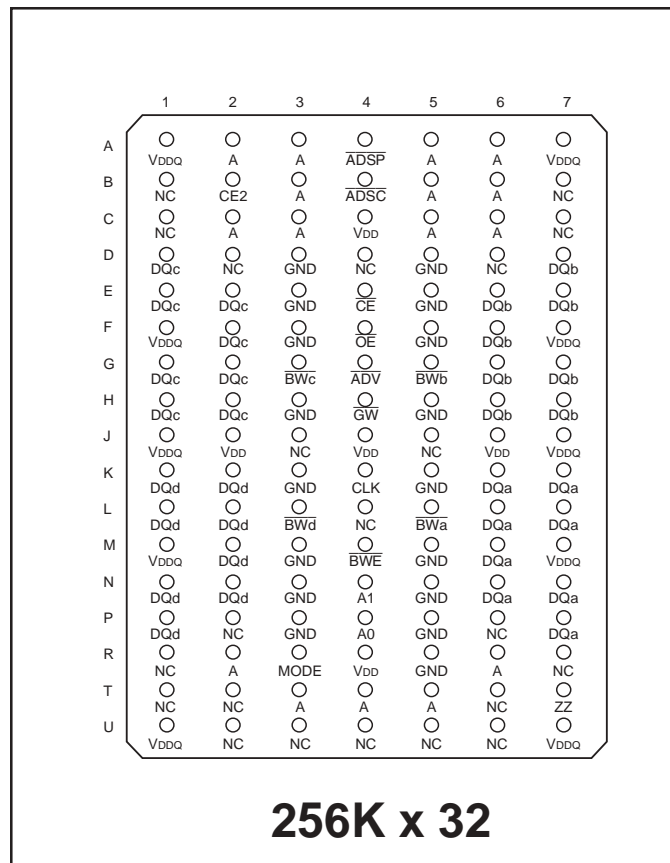
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BLOCK DIAGRAM

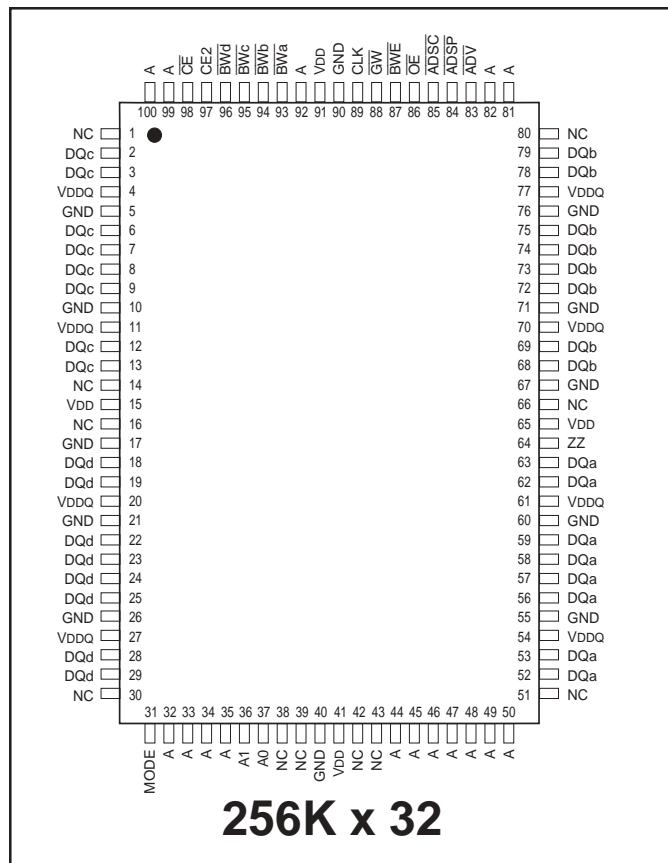


PIN CONFIGURATION

119-pin PBGA (Top View) (D Version)



100-Pin TQFP (D Version)

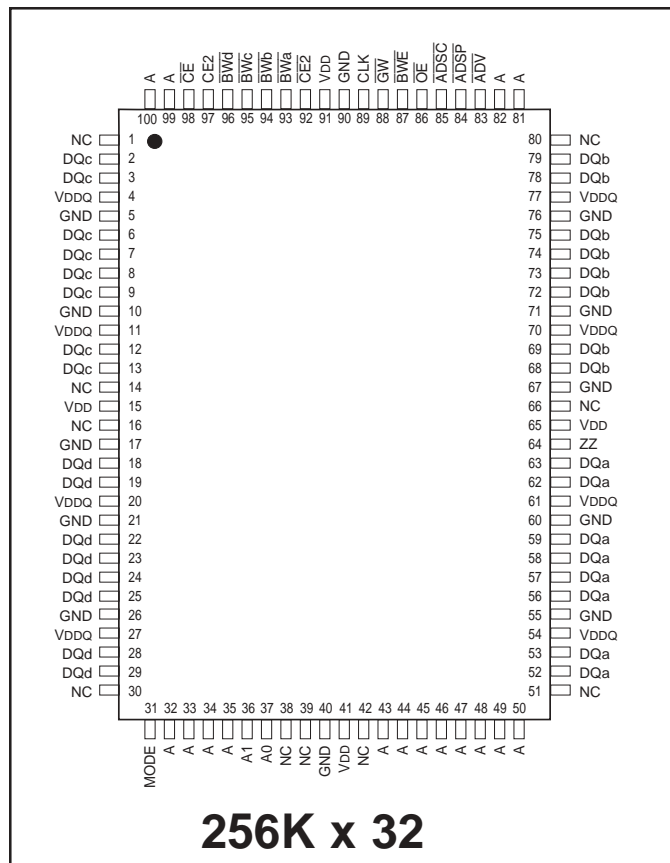


PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BW \bar{a} -BW \bar{d}	Synchronous Byte Write Enable
BWE	Synchronous Byte Write Enable

GW	Synchronous Global Write Enable
CE, CE2	Synchronous Chip Enable
OE	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
VDD	+3.3V Power Supply
GND	Ground
VDDQ	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION
100-Pin TQFP (T Version)

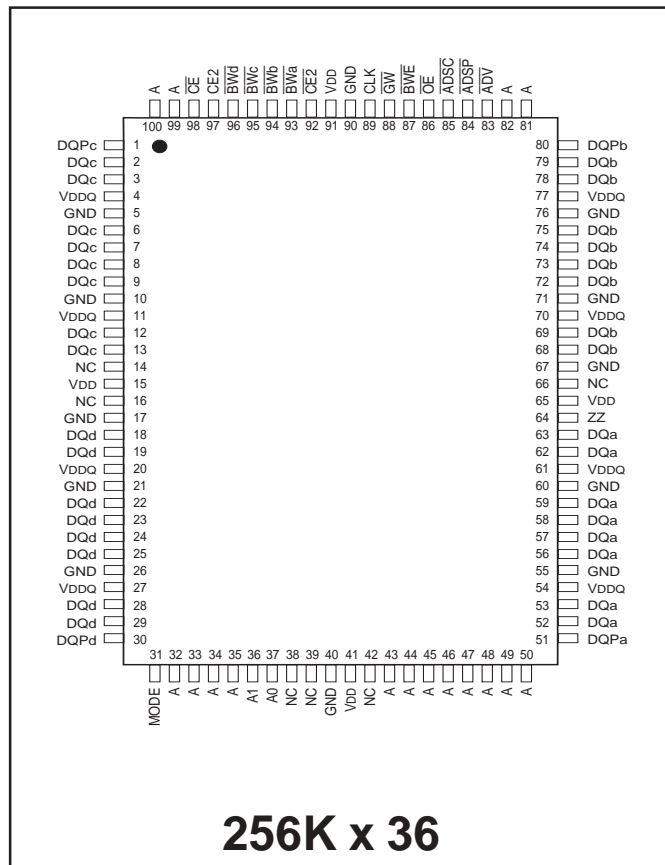


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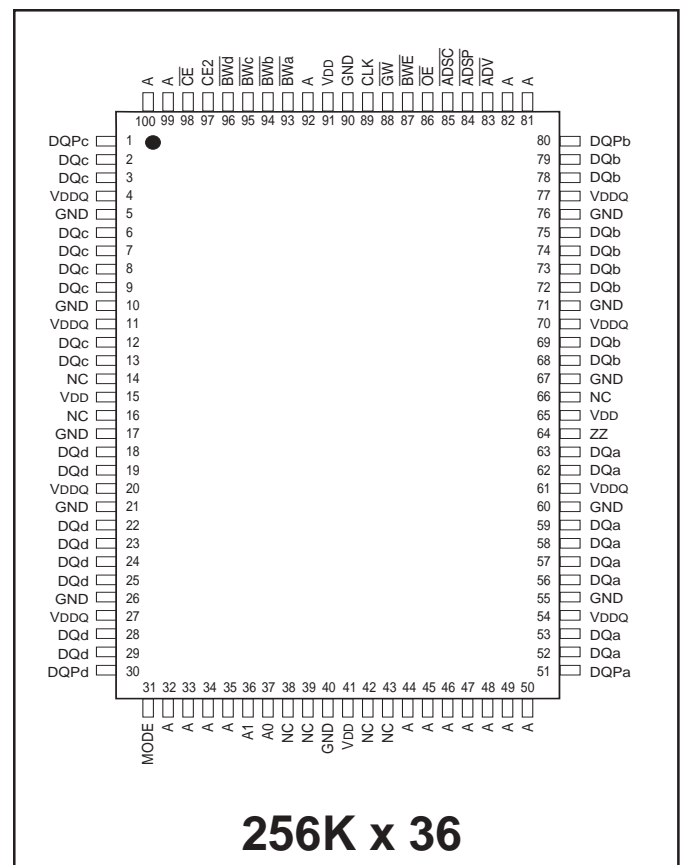
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CLK	Synchronous Clock
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$\overline{\text{ADSC}}$	Synchronous Controller Address Status
$\overline{\text{ADV}}$	Synchronous Burst Address Advance
$\overline{\text{BWA-BWd}}$	Synchronous Byte Write Enable
$\overline{\text{BWE}}$	Synchronous Byte Write Enable

$\overline{\text{GW}}$	Synchronous Global Write Enable
$\overline{\text{CE}}, \overline{\text{CE2}}, \text{CE2}$	Synchronous Chip Enable
$\overline{\text{OE}}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V _{DD}	+3.3V Power Supply
GND	Ground
V _{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION
100-pin TQFP (T Version)



100-Pin TQFP (D Version)

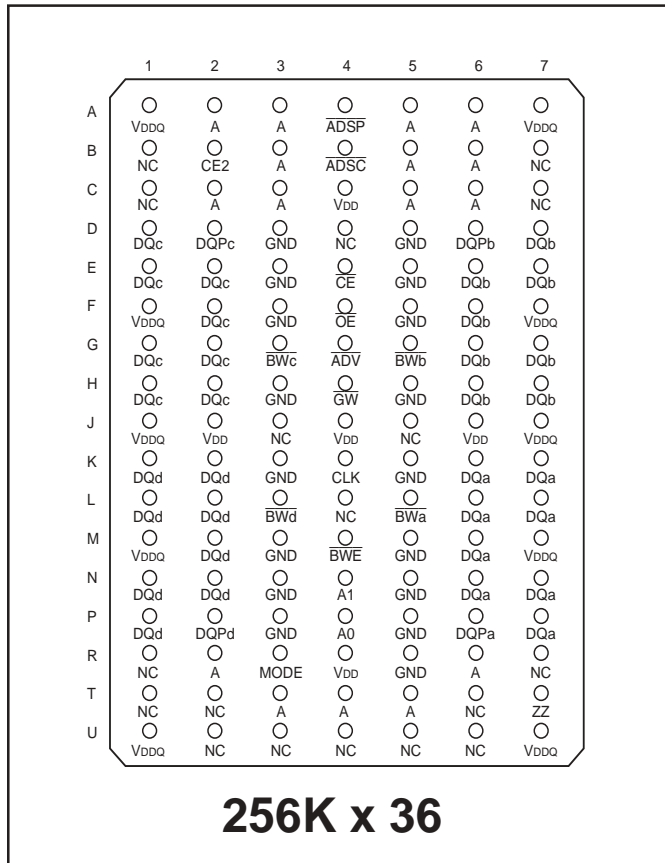


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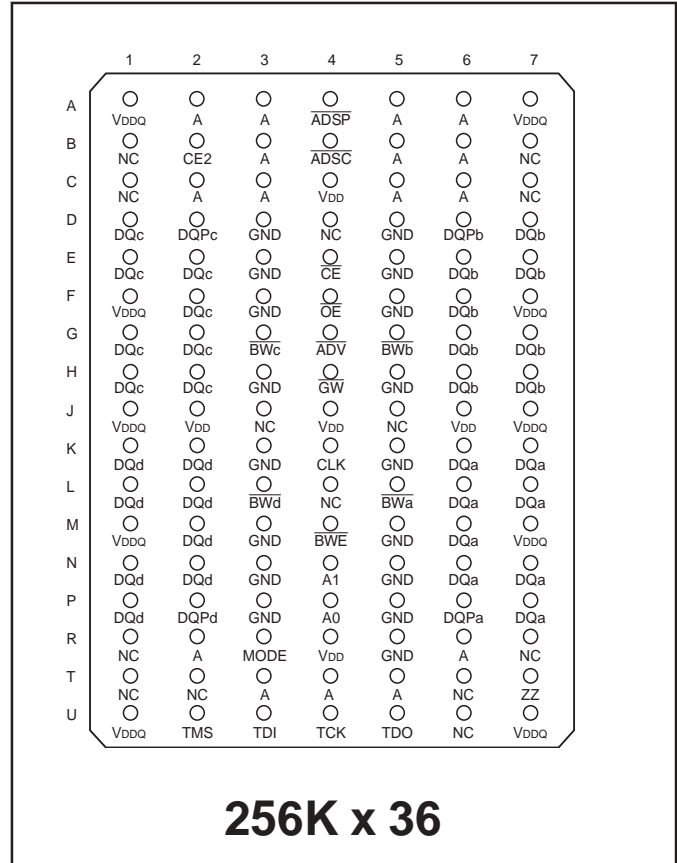
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ADV	Synchronous Burst Address Advance
BW _a -BW _d	Individual Byte Write Enable
BWE	Synchronous Byte Write Enable

TMS, TDI	JTAG Boundry Scan Pins
TCK, TDO	
GW	Synchronous Global Write Enable
CE, CE2	Synchronous Chip Enable
OE	Output Enable
DQ _a -DQ _d	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V _{DD}	+3.3V Power Supply
GND	Ground
V _{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQ _{Pa} -DQ _{Pd}	Parity Data I/O

PIN CONFIGURATION
 119-pin PBGA (Top View) (D Version)



PIN CONFIGURATION
 119-pin PBGA (Top View) (J Version)



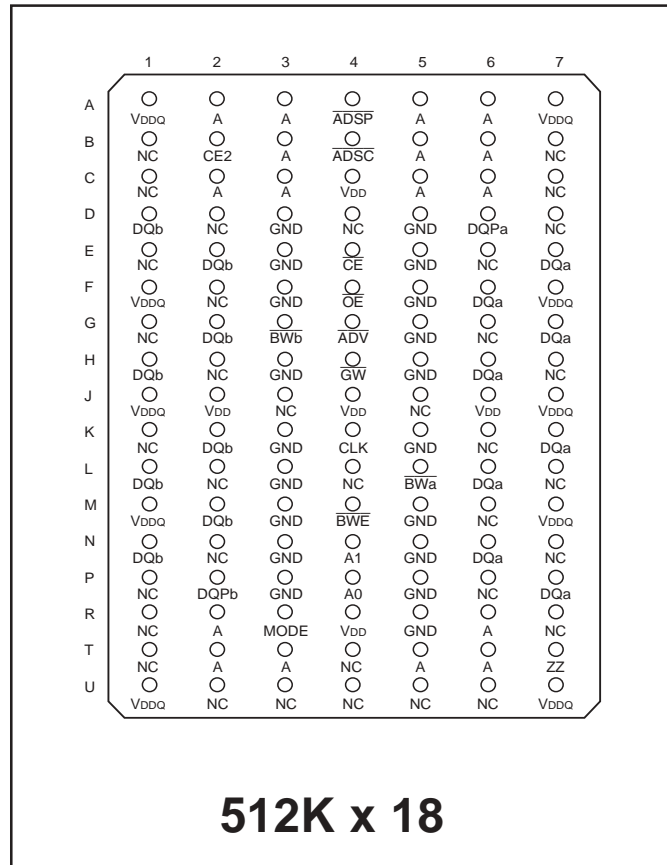
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BWE	Synchronous Byte Write Enable

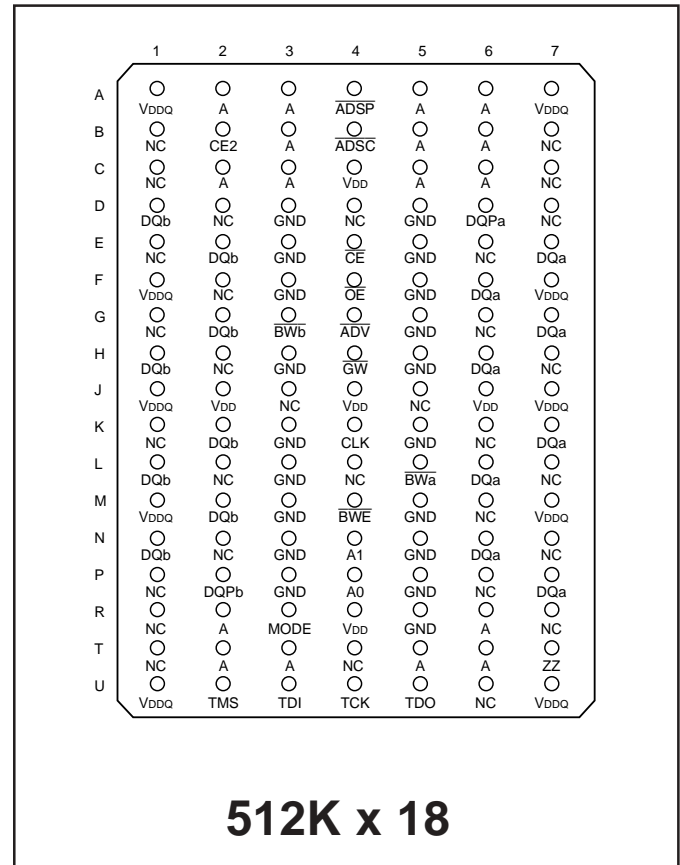
TMS, TDI TCK, TDO	JTAG Boundary Scan Pins
GW	Synchronous Global Write Enable
CE, CE2	Synchronous Chip Enable
OE	Output Enable
DQ _a -DQ _d	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V _{DD}	+3.3V Power Supply
GND	Ground
V _{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQ _{Pa} -DQ _{Pd}	Parity Data I/O

PIN CONFIGURATION

119-pin PBGA (Top View) (D Version)



119-pin PBGA (Top View) (J Version)

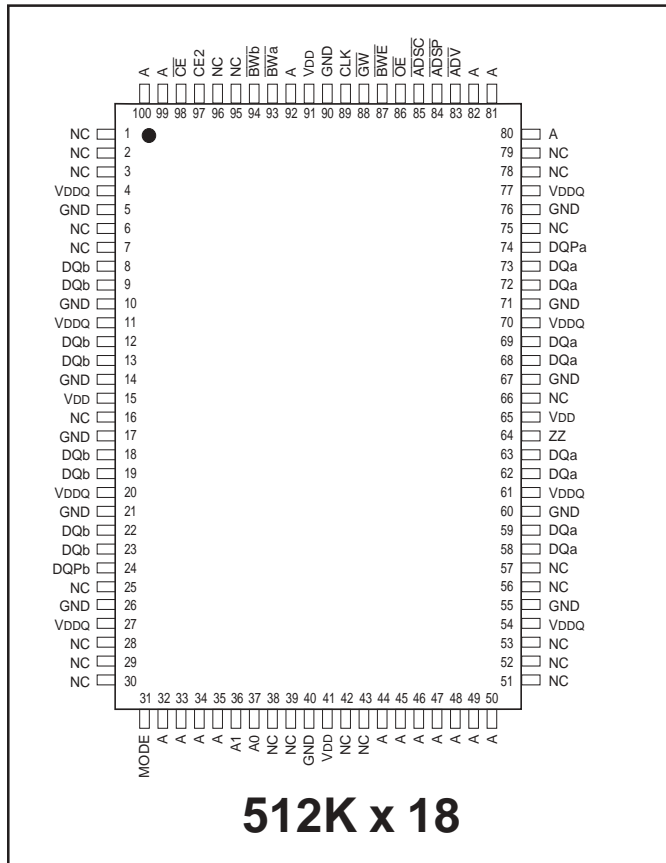


PIN DESCRIPTIONS

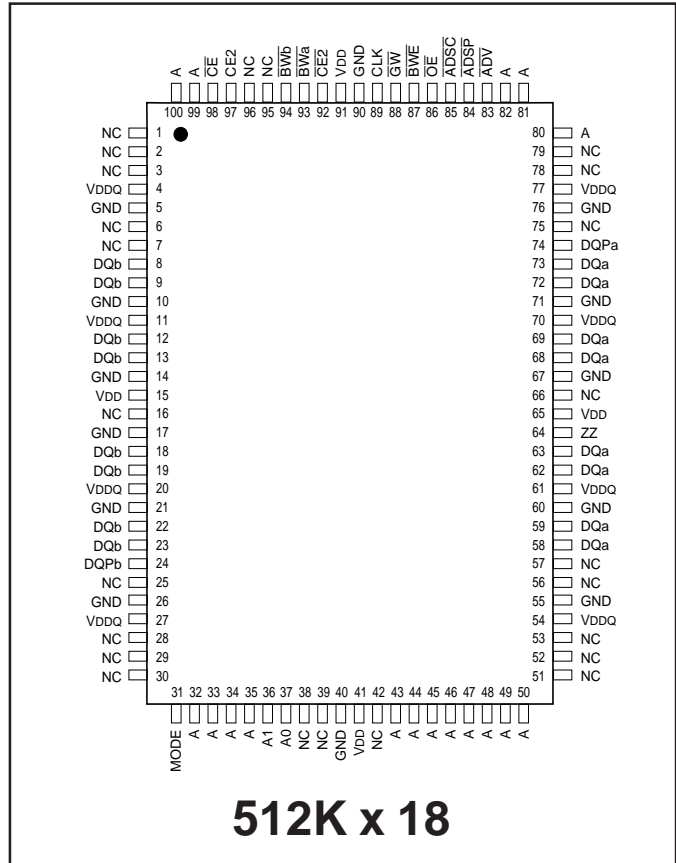
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TMS, TDI	JTAG Boundry Scan Pins
TCK, TDO	
GW	Synchronous Global Write Enable
CE, CE2	Synchronous Chip Enable
OE	Output Enable
DQ _a -DQ _d	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V _{DD}	+3.3V Power Supply
GND	Ground
V _{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQ _{Pa} -DQ _{Pd}	Parity Data I/O

PIN CONFIGURATION
100-Pin TQFP (D Version)



100-Pin TQFP (T Version)



PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
ADSP	Synchronous Processor Address Status
ADSC	Synchronous Controller Address Status
ADV	Synchronous Burst Address Advance
BWa-BWd	Individual Byte Write Enable
BWE	Synchronous Byte Write Enable

TMS, TDI	JTAG Boundary Scan Pins
TCK, TDO	
GW	Synchronous Global Write Enable
CE, CE2, CE2	Synchronous Chip Enable
OE	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
VDD	+3.3V Power Supply
GND	Ground
VDDQ	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

TRUTH TABLE

Operation	Address									
	Used	\overline{CE}	CE2	$\overline{CE2}$	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\overline{WRITE}	\overline{OE}	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

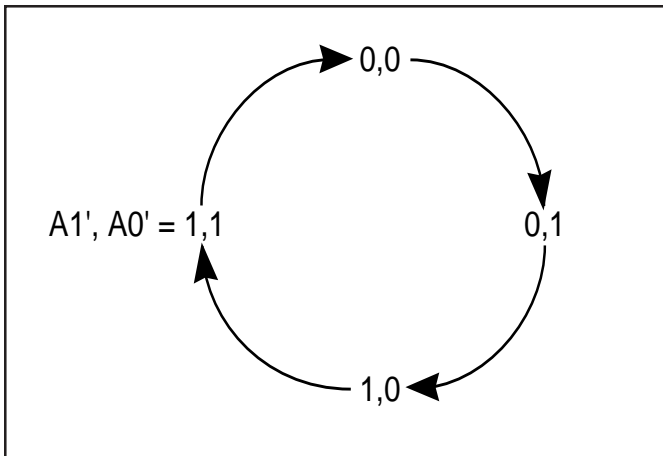
PARTIAL TRUTH TABLE

Function	\overline{GW}	\overline{BWE}	\overline{BWa}	\overline{BWb}	\overline{BWc}	\overline{BWd}
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DDQ} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-55 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to GND for I/O Pins	-0.5 to V _{DDQ} + 0.3	V
V _{IN}	Voltage Relative to GND for for Address and Control Inputs	-0.5 to V _{DD} + 0.5	V
V _{DD}	Voltage on V _{DD} Supply Relative to GND	-0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	3.3V, +10%, -5%	2.375-3.6V
Industrial	-40°C to +85°C	3.3V, +10%, -5%	2.375-3.6V

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA, V _{DDQ} = 2.5V	2.0	—	V
		I _{OH} = -4.0 mA, V _{DDQ} = 3.3V	2.4	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 1.0 mA, V _{DDQ} = 2.5V	—	0.4	V
		I _{OL} = 8.0 mA, V _{DDQ} = 3.3V	—	0.4	V
V _{IH}	Input HIGH Voltage	V _{DDQ} = 2.5V	1.7	V _{DD} + 0.3	V
		V _{DDQ} = 3.3V	2.0	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage	V _{DDQ} = 2.5V	-0.3	0.7	V
		V _{DDQ} = 3.3V	-0.3	0.8	V
I _{LI}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{DDQ} ⁽²⁾	Com. Ind.	-5 5	μA
I _{LO}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{DDQ} , $\overline{OE} = V_{IH}$	Com. Ind.	-5 5	μA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		6.5 Max.	7.5 Max.	Unit
I _{CC}	AC Operating Supply Current	Device Selected, All Inputs ≤ V _{IL} or ≥ V _{IH} $\overline{OE} = V_{IH}$, ZZ ≤ V _{IL} Cycle Time ≥ t _{kc} min.	Com.	110	100	mA
			Ind.	120	110	mA
I _{SB}	Standby Current	Device Deselected, V _{DD} = Max., All Inputs ≤ V _{IL} or ≥ V _{IH} ZZ ≤ V _{IL} , f = f _{max}	Com.	55	55	mA
			Ind.	60	60	mA
I _{SBI}	Standby Current CMOS Input	Device Deselected, V _{DD} = Max., V _{IN} ≤ GND + 0.2V or ≥ V _{DD} - 0.2V f = 0	Com.	30	30	mA
			Ind.	40	40	mA

Notes:

- The MODE pin should be tied to V_{DD} or GND. It exhibits ±30 μA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{DD} - 0.2V.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{dd} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

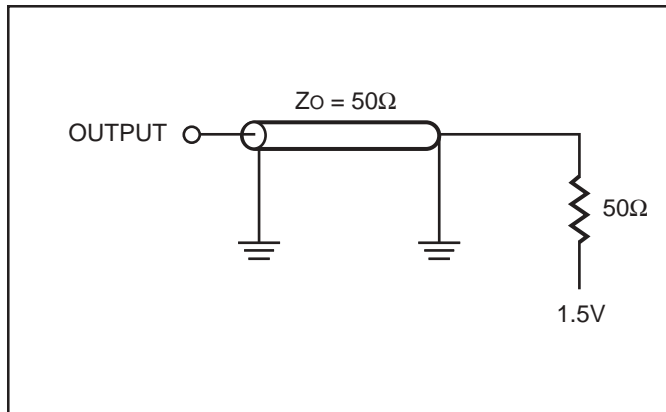


Figure 1

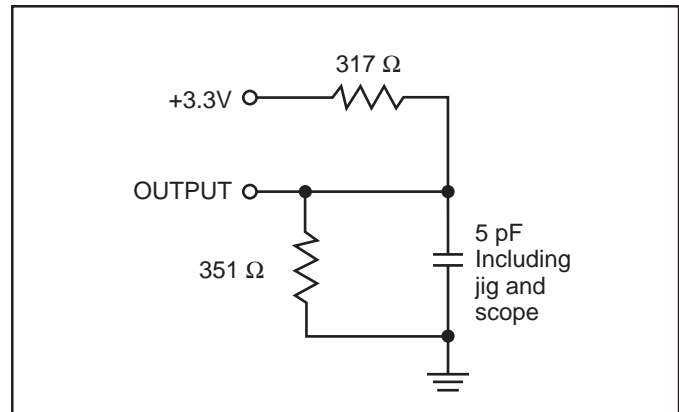


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

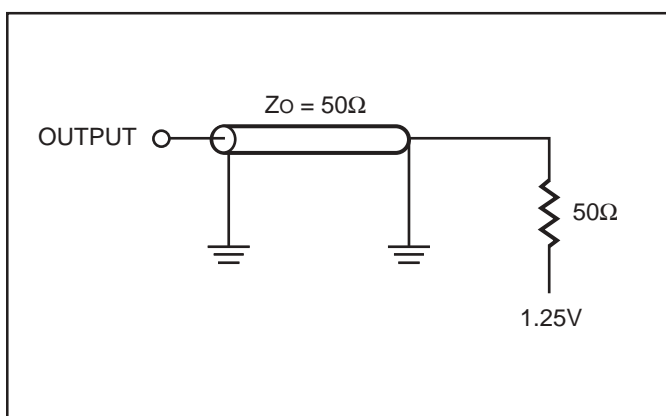


Figure 3

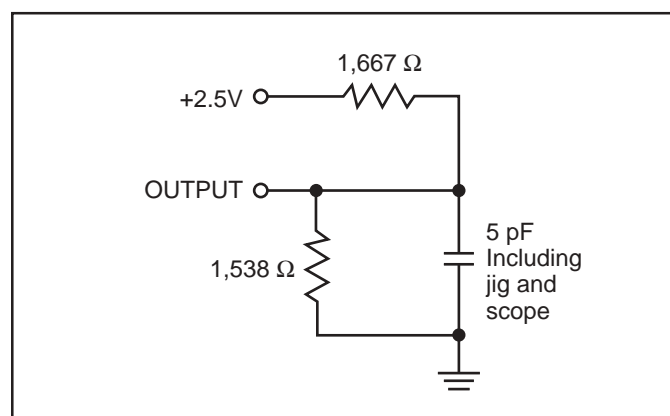


Figure 4

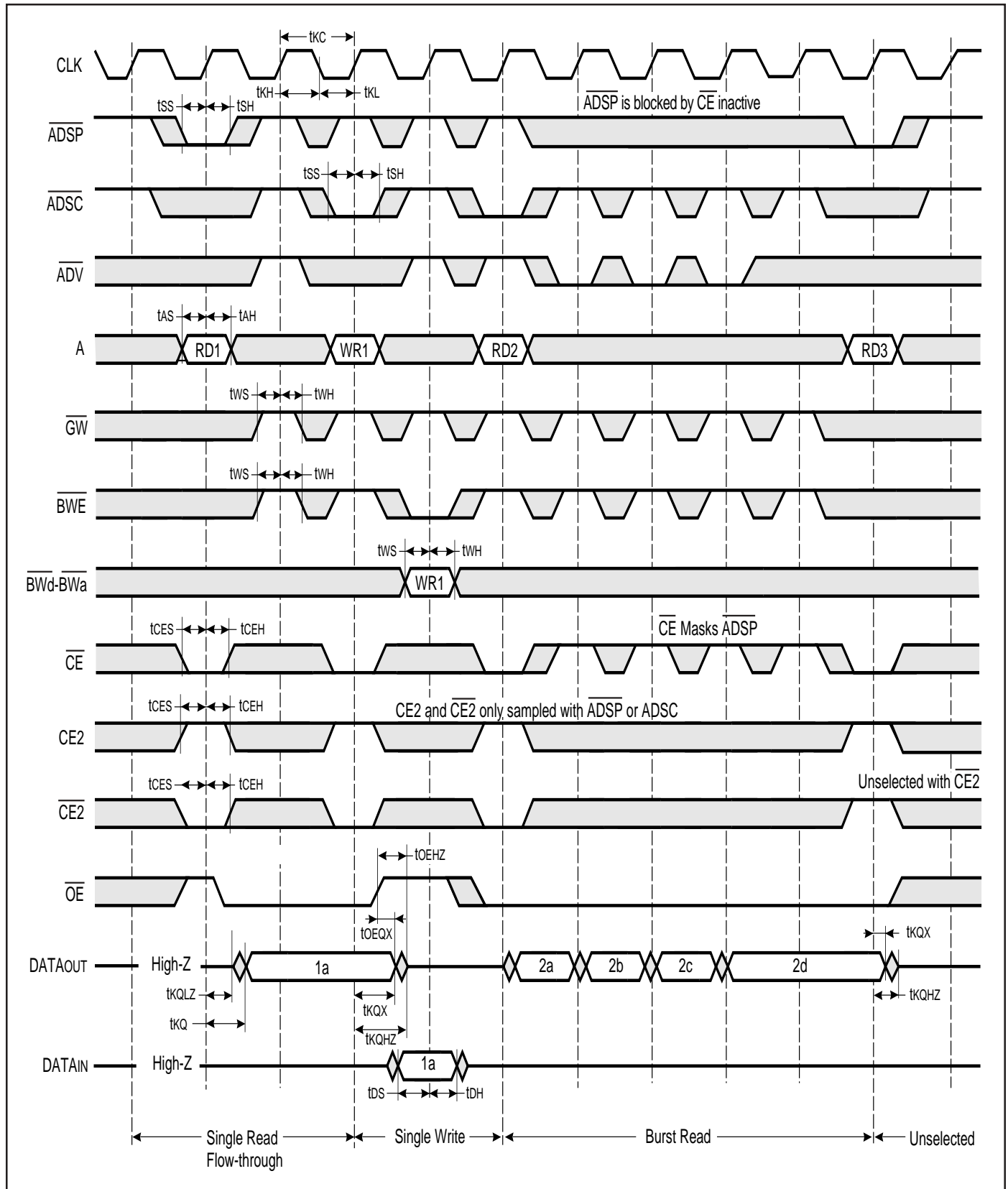
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	6.5		7.5		Unit
		Min.	Max.	Min.	Max.	
f _{MAX}	Clock Frequency	—	133	—	117	MHz
t _{KC}	Cycle Time	7.5	—	8.5	—	ns
t _{KH}	Clock High Pulse Width	2.2	—	2.5	—	ns
t _{KL}	Clock Low Pulse Width	2.2	—	2.5	—	ns
t _{KQ}	Clock Access Time	—	6.5	—	7.5	ns
t _{KQX} ⁽¹⁾	Clock High to Output Invalid	2	—	2	—	ns
t _{KQLZ} ^(1,2)	Clock High to Output Low-Z	0	—	0	—	ns
t _{KQHZ} ^(1,2)	Clock High to Output High-Z	—	3.5	—	3.5	ns
t _{OEQ}	Output Enable to Output Valid	—	3.5	—	3.5	ns
t _{OELZ} ^(1,2)	Output Enable to Output Low-Z	0	—	0	—	ns
t _{OEHZ} ^(1,2)	Output Enable to Output High-Z	—	3.5	—	3.5	ns
t _{AS}	Address Setup Time	1.5	—	1.8	—	ns
t _{SS}	Address Status Setup Time	1.5	—	1.8	—	ns
t _{WS}	Write Setup Time	1.5	—	1.8	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.8	—	ns
t _{AVS}	Address Advance Setup Time	1.5	—	1.8	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	ns

Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

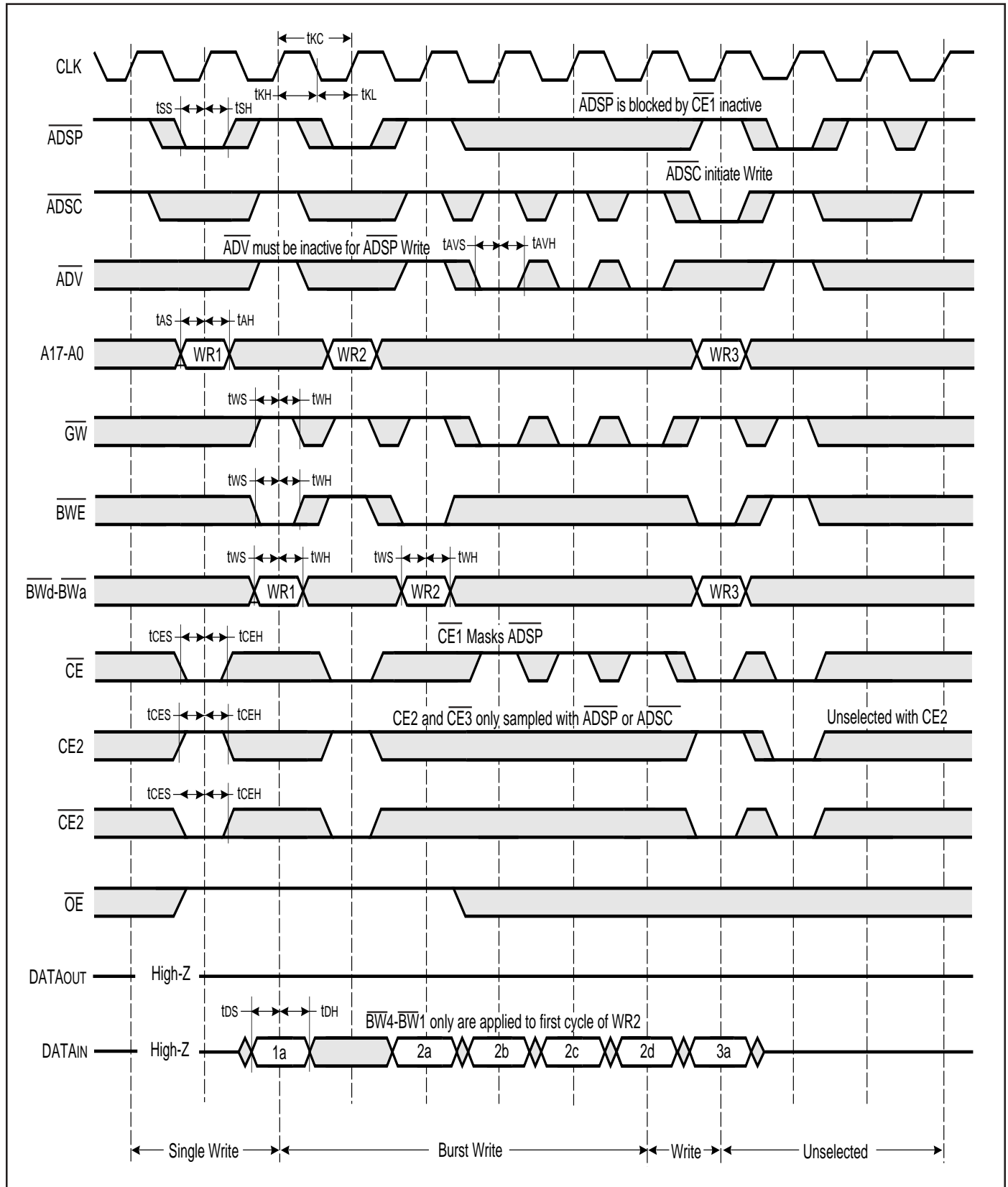
READ/WRITE CYCLE TIMING



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	6.5		7.5		Unit
		Min.	Max.	Min.	Max.	
t _{KC}	Cycle Time	7.5	—	8.5	—	ns
t _{KH}	Clock High Pulse Width	2.0	—	2.5	—	ns
t _{KL}	Clock Low Pulse Width	2.2	—	2.5	—	ns
t _{AS}	Address Setup Time	1.5	—	1.8	—	ns
t _{SS}	Address Status Setup Time	1.5	—	1.8	—	ns
t _{WS}	Write Setup Time	1.5	—	1.8	—	ns
t _{DS}	Data In Setup Time	1.5	—	1.8	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.8	—	ns
t _{AVS}	Address Advance Setup Time	1.5	—	1.8	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	ns
t _{SH}	Address Status Hold Time	0.5	—	0.5	—	ns
t _{DH}	Data In Hold Time	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t _{AVH}	Address Advance Hold Time	0.5	—	0.5	—	ns

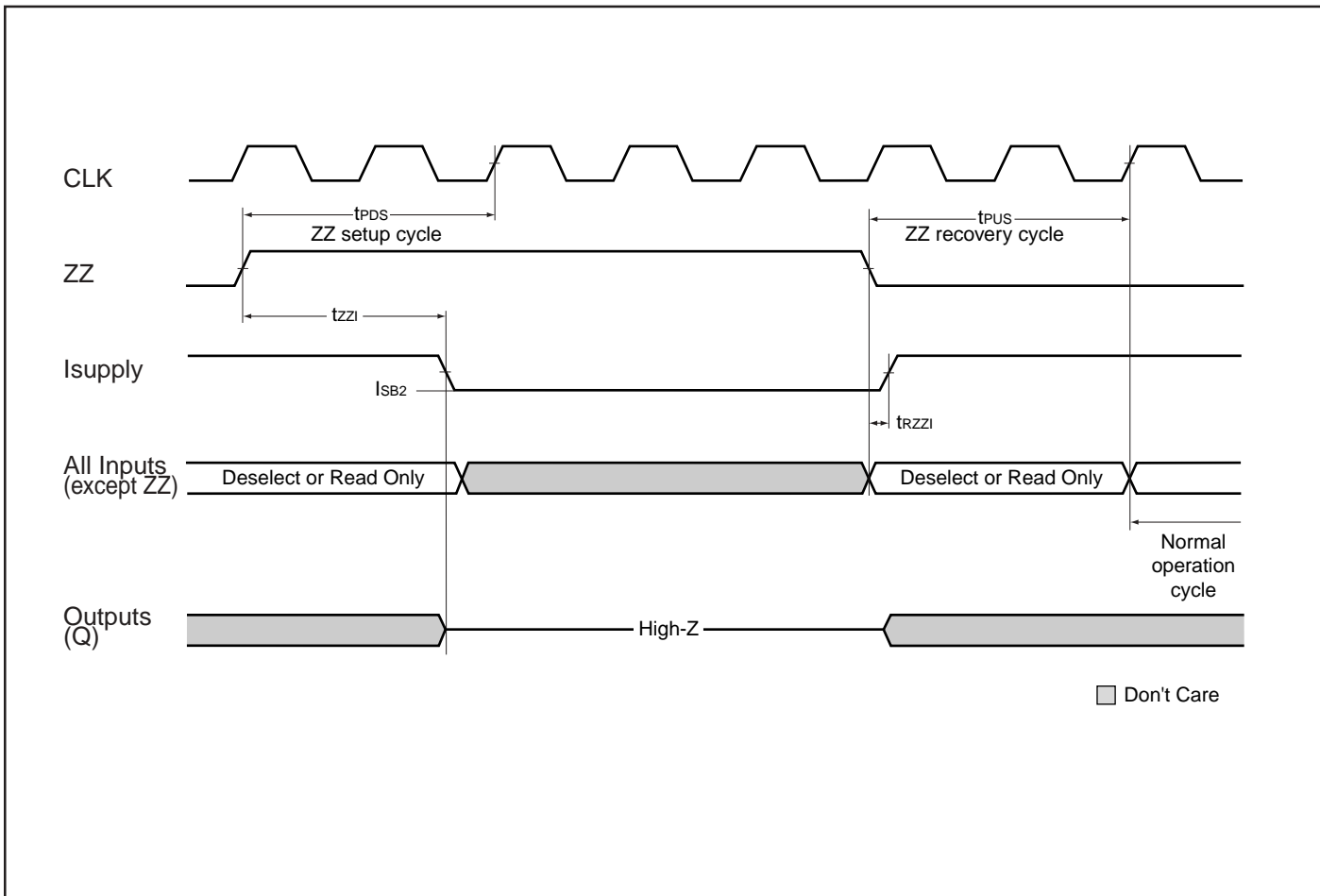
WRITE CYCLE TIMING



SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
ISB2	Current during SLEEP MODE	ZZ ≥ V _{IH} Com.	—	30	mA
		ZZ ≥ V _{IH} Ind.	—	40	
tpDS	ZZ active to input ignored		2	—	cycle
tpUS	ZZ inactive to input sampled		2	—	cycle
tZZI	ZZ active to SLEEP current		2	—	cycle
trZZI	ZZ inactive to exit SLEEP current		0	—	ns

SLEEP MODE TIMING



IEEE 1149.1 Serial Boundary Scan (JTAG)

The IS61LF25636T/D/J and IS61LF51218T/D/JT/D/JT/D/J have a serial boundary scan Test Access Port (TAP) in the PBGA package only. (Not available in TQFP package or with the IS61LPS25632T/D/J.) This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 2.5V I/O logic levels.

Disabling the JTAG Feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (GND) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

Test Access Port (TAP) - Test Clock

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

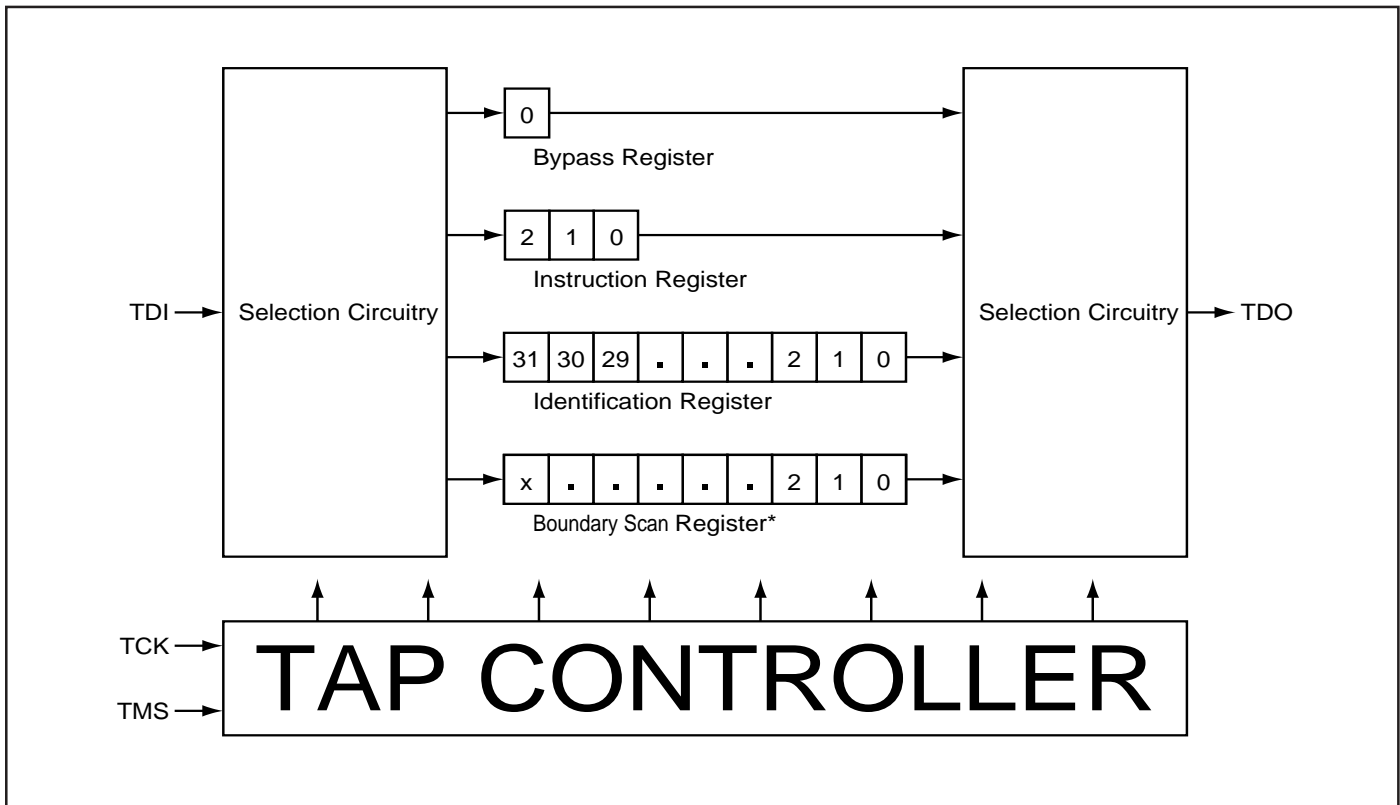
Test Mode Select (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

TAP CONTROLLER BLOCK DIAGRAM



Test Data Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (GND) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 70-bit-long register and the x18 configuration has a 51-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Scan Register Sizes

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

IDENTIFICATION (ID) REGISTER

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from

a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID REGISTER CONTENTS

Part #	Die Revision Code				Part Configuration								Vendor Defomotopm								ISSI Technology JEDEC Vendor ID Code								Presence Register			
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4		3	2	1
256K	X	X	X	X	0	0	1	1	0	0	0	1	0	0	X	X	X	X	X	X	0	0	0	1	1	0	1	0	1	0	1	1
512K	X	X	X	X	0	0	1	1	1	0	0	0	1	1	X	X	X	X	X	X	0	0	0	1	1	0	1	0	1	0	1	1

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (tcs and tch). To insure that the SRAM

clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK and CLK captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

Bypass

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

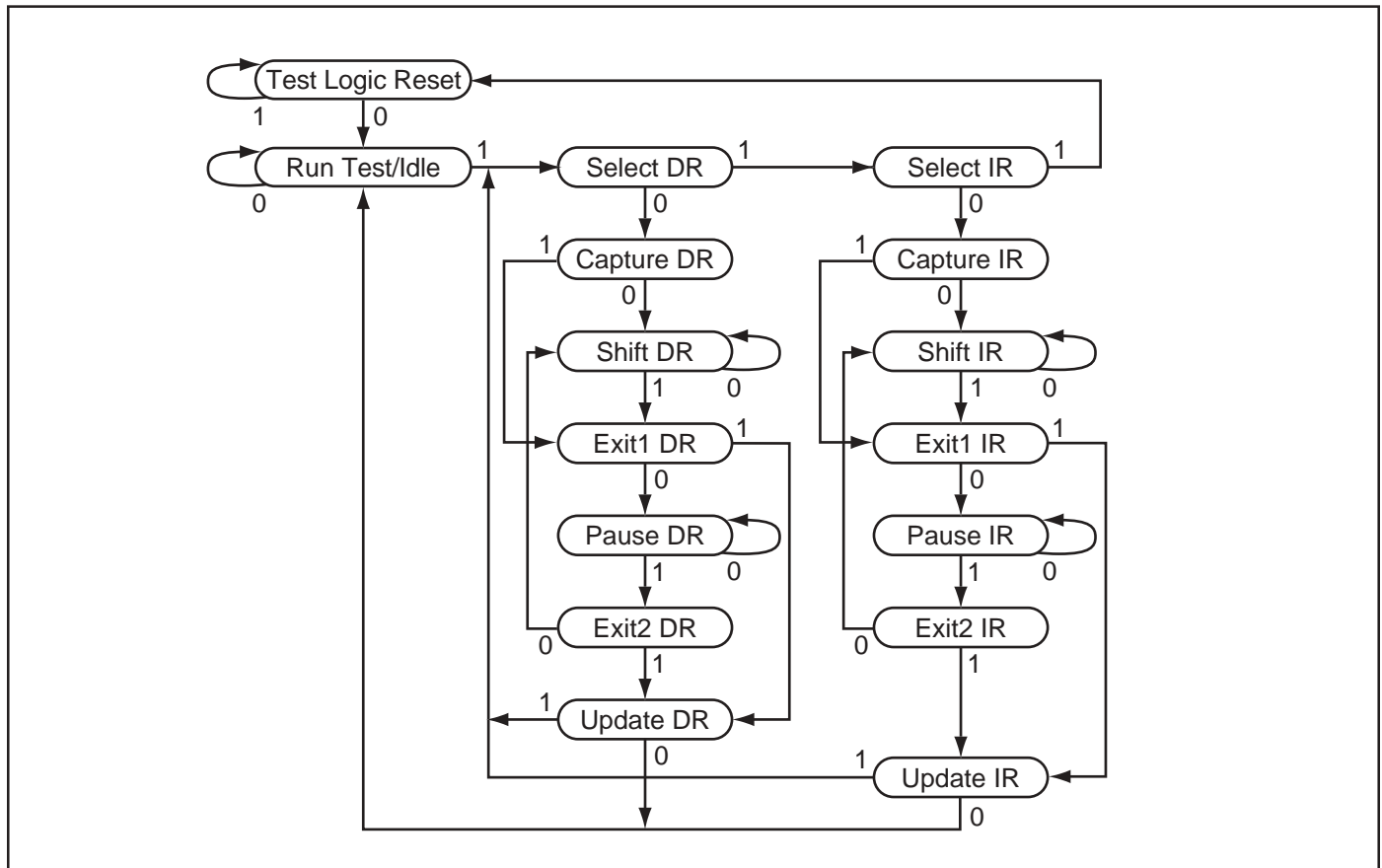
Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

INSTRUCTION CODES

Code	Instruction	Description
001	IDCODE	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
010	SAMPLE Z	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
011	RESERVED	Do Not Use: This instruction is reserved for future use.
100	SAMPLE/PRELOAD	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1 compliant.
101	RESERVED	Do Not Use: This instruction is reserved for future use.
110	RESERVED	Do Not Use: This instruction is reserved for future use.
111	BYPASS	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

TAP CONTROLLER STATE DIAGRAM



TAP ELECTRICAL CHARACTERISTICS Over the Operating Range^(1,2)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V _{OH1}	Output HIGH Voltage	I _{OH} = -2.0 mA	1.7	—	V
V _{OH2}	Output HIGH Voltage	I _{OH} = -100 mA	2.1	—	V
V _{OL1}	Output LOW Voltage	I _{OL} = 2.0 mA	—	0.7	V
V _{OL2}	Output LOW Voltage	I _{OL} = 100 mA	—	0.2	V
V _{IH}	Input HIGH Voltage		1.7	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage	I _{OLT} = 2mA	-0.3	0.7	V
I _x	Input Load Current	GND ≤ V _I ≤ V _{DDQ}	-5	5	mA

Notes:

- All Voltage referenced to Ground.
- Overshoot: V_{IH} (AC) ≤ V_{DD} + 1.5V for t ≤ t_{trcyc}/2,
Undershoot: V_{IL} (AC) ≤ 0.5V for t ≤ t_{trcyc}/2,
Power-up: V_{IH} < 2.6V and V_{DD} < 2.4V and V_{DDQ} < 1.4V for t < 200 ms.

TAP AC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Min.	Max.	Unit
t _{trcyc}	TCK Clock cycle time	100	—	ns
f _{trf}	TCK Clock frequency	—	10	MHz
t _{trH}	TCK Clock HIGH	40	—	ns
t _{trL}	TCK Clock LOW	40	—	ns
t _{trMSS}	TMS setup to TCK Clock Rise	10	—	ns
t _{trDIS}	TDI setup to TCK Clock Rise	10	—	ns
t _{trCS}	Capture setup to TCK Rise	10	—	ns
t _{trMSH}	TMS hold after TCK Clock Rise	10	—	ns
t _{trDIH}	TDI Hold after Clock Rise	10	—	ns
t _{trCH}	Capture hold after Clock Rise	10	—	ns
t _{trDOV}	TCK LOW to TDO valid	—	20	ns
t _{trDOX}	TCK LOW to TDO invalid	0	—	ns

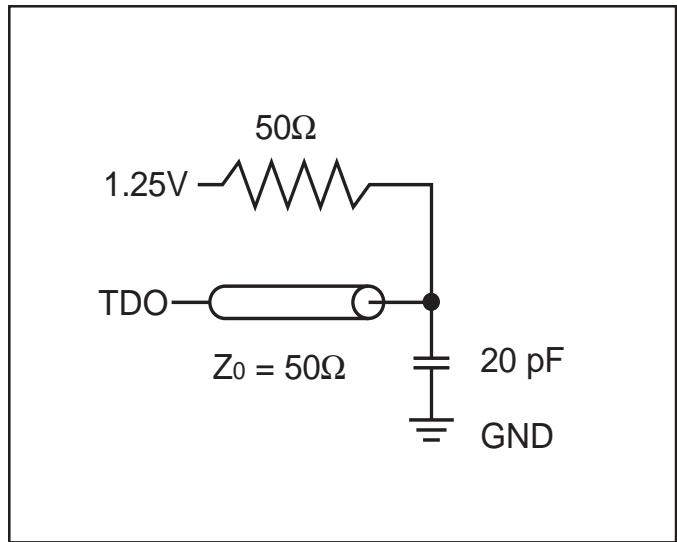
Notes:

- t_{trCS} and t_{trCH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
- Test conditions are specified using the load in TAP AC test conditions. t_{tr}/t_{trf} = 1 ns.

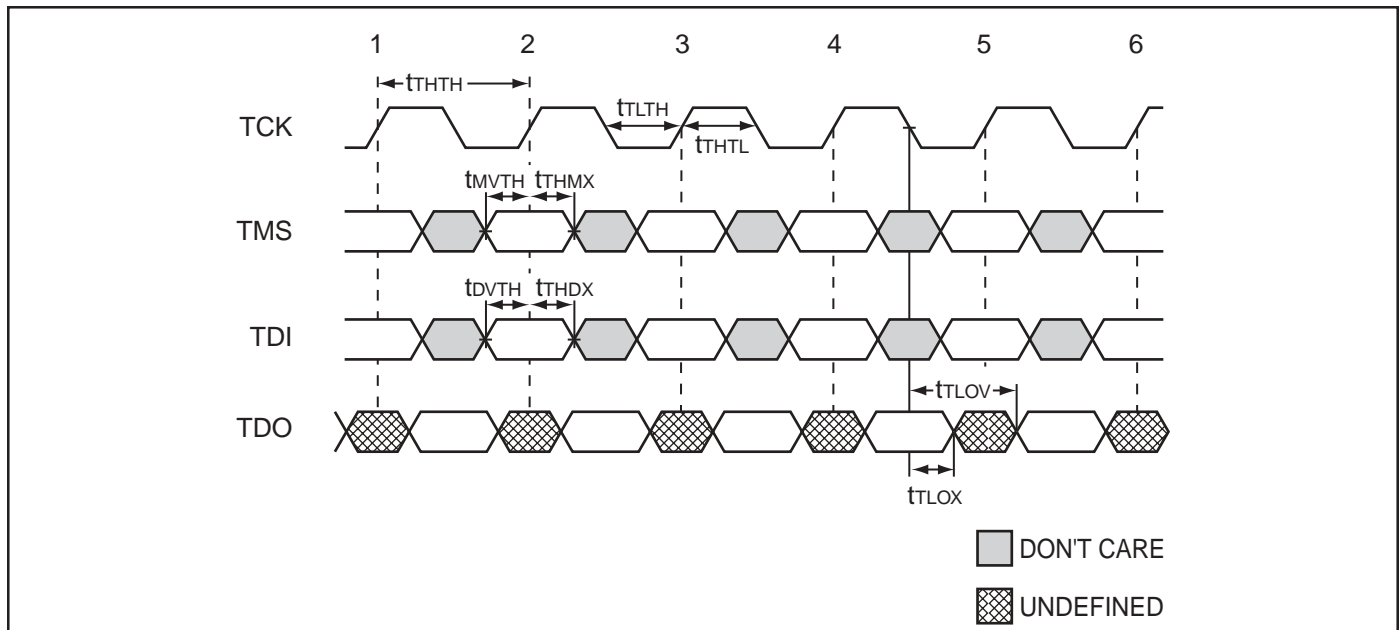
TAP AC TEST CONDITIONS

Input pulse levels	0 to 2.5V
Input rise and fall times	1ns
Input timing reference levels	1.25V
Output reference levels	1.25V
Test load termination supply voltage	1.25V

TAP OUTPUT LOAD EQUIVALENT



TAP TIMING



BOUNDARY SCAN ORDER (256K X 36)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	19	DQb	7G	37	BWa	5L	55	DQd	2K
2	A	3T	20	DQb	6F	38	BWb	5G	56	DQd	1L
3	A	4T	21	DQb	7E	39	BWc	3G	57	DQd	2M
4	A	5T	22	DQb	7D	40	BWd	3L	58	DQd	1N
5	A	6R	23	DQb	7H	41	CE2	2B	59	DQd	1P
6	A	3B	24	DQb	6G	42	\overline{CE}	4E	60	DQd	1K
7	A	5B	25	DQb	6E	43	A	3A	61	DQd	2L
8	DQa	6P	26	DQb	6D	44	A	2A	62	DQd	2N
9	DQa	7N	27	A	6A	45	DQc	2D	63	DQd	2P
10	DQa	6M	28	A	5A	46	DQc	1E	64	MODE	3R
11	DQa	7L	29	ADV	4G	47	DQc	2F	65	A	2C
12	DQa	6K	30	ADSP	4A	48	DQc	1G	66	A	3C
13	DQa	7P	31	ADSC	4B	49	DQc	2H	67	A	5C
14	DQa	6N	32	OE	4F	50	DQc	1D	68	A	6C
15	DQa	6L	33	BWE	4M	51	DQc	2E	69	A1	4N
16	DQa	7K	34	GW	4H	52	DQc	2G	70	A0	4P
17	ZZ	7T	35	CLK	4K	53	DQc	1H			
18	DQb	6H	36	A	6B	54	NC	5R			

BOUNDARY SCAN ORDER (512K X 18)

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	14	DQa	7G	27	CLK	4K	40	DQb	2K
2	A	2T	15	DQa	6F	28	A	6B	41	DQb	1L
3	A	3T	16	DQa	7E	29	BWa	5L	42	DQb	2M
4	A	5T	17	DQa	6D	30	BWb	3G	43	DQb	1N
5	A	6R	18	A	6T	31	CE2	2B	44	DQb	2P
6	A	3B	19	A	6A	32	\overline{CE}	4E	45	MODE	3R
7	A	5B	20	A	5A	33	A	3A	46	A	2C
8	DQa	7P	21	ADV	4G	34	A	2A	47	A	3C
9	DQa	6N	22	ADSP	4A	35	DQb	1D	48	A	5C
10	DQa	6L	23	ADSC	4B	36	DQb	2E	49	A	6C
11	DQa	7K	24	OE	4F	37	DQb	2G	50	A1	4N
12	ZZ	7T	25	BWE	4M	38	DQb	1H	51	A0	4P
13	DQa	6H	26	GW	4H	39	NC	5R			

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
6.5 ns	IS61LF25632T-6.5TQ	TQFP
	IS61LF25632D-6.5TQ	TQFP
7.5 ns	IS61LF25632T-7.5TQ	TQFP
	IS61LF25632D-7.5TQ	TQFP
	IS61LF25632D-7.5B	PBGA

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
6.5 ns	IS61LF25636T-6.5TQ	TQFP
	IS61LF25636D-6.5TQ	TQFP
	IS61LF25636D-6.5B	PBGA
	IS61LF25636J-6.5B	PBGA
7.5 ns	IS61LF25636T-7.5TQ	TQFP
	IS61LF25636D-7.5TQ	TQFP
	IS61LF25636D-7.5B	PBGA
	IS61LF25636J-7.5B	PBGA

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
6.5 ns	IS61LF51218T-6.5TQ	TQFP
	IS61LF51218D-6.5TQ	TQFP
	IS61LF51218D-6.5B	PBGA
	IS61LF51218J-6.5B	PBGA
7.5 ns	IS61LF51218T-7.5TQ	TQFP
	IS61LF51218D-7.5TQ	TQFP
	IS61LF51218D-7.5B	PBGA
	IS61LF51218J-7.5B	PBGA

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
6.5 ns	IS61LF25632T-6.5TQI	TQFP
	IS61LF25632D-6.5TQI	TQFP
7.5 ns	IS61LF25632T-7.5TQI	TQFP
	IS61LF25632D-7.5TQI	TQFP

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
6.5 ns	IS61LF25636T-6.5TQI	TQFP
	IS61LF25636D-6.5TQI	TQFP
7.5 ns	IS61LF25636T-7.5TQI	TQFP
	IS61LF25636D-7.5TQI	TQFP
	IS61LF25636D-7.5BI	TQFP
	IS61LF25636J-7.5BI	TQFP

Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
6.5 ns	IS61LF51218T-6.5TQI	TQFP
	IS61LF51218D-6.5TQI	TQFP
7.5 ns	IS61LF51218T-7.5TQI	TQFP
	IS61LF51218D-7.5TQI	TQFP
	IS61LF51218D-7.5BI	TQFP
	IS61LF51218J-7.5BI	TQFP