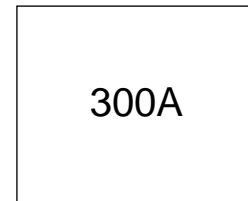


PHASE CONTROL THYRISTORS

Stud Version

Features

- Center amplifying gate
- Hermetic metal case with ceramic insulator
- International standard case TO-209AE (TO-118)
- Threaded studs UNF 3/4 - 16UNF2A or ISO M24x1.5
- Compression Bonded Encapsulation for heavy duty operations such as severe thermal cycling

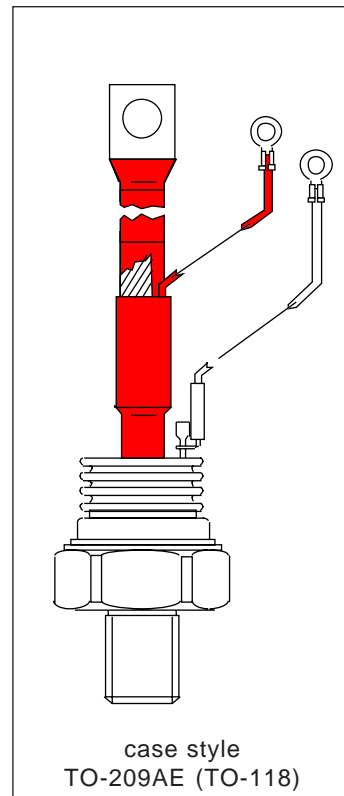


Typical Applications

- DC motor controls
- Controlled DC power supplies
- AC controllers

Major Ratings and Characteristics

Parameters	ST300S	Units
$I_{T(AV)}$	300	A
@ T_C	75	°C
$I_{T(RMS)}$	470	A
I_{TSM} @ 50Hz	8000	A
@ 60Hz	8380	A
I^2t @ 50Hz	320	KA ² s
@ 60Hz	292	KA ² s
V_{DRM}/V_{RRM}	400 to 2000	V
t_q typical	100	μs
T_J	- 40 to 125	°C



ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} , max. repetitive peak and off-state voltage V	V_{RSM} , maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J$ max mA
ST300S	04	400	500	50
	08	800	900	
	12	1200	1300	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

On-state Conduction

Parameter	ST300S	Units	Conditions
$I_{T(AV)}$ Max. average on-state current @ Case temperature	300	A	180° conduction, half sine wave
	75	°C	
$I_{T(RMS)}$ Max. RMS on-state current	470	A	DC @ 64°C case temperature
I_{TSM} Max. peak, one-cycle non-repetitive surge current	8000	A	t = 10ms No voltage reappplied
	8380		t = 8.3ms reappplied
	6730		t = 10ms 100% V_{RRM} reappplied
	7040		t = 8.3ms reappplied
I^2t Maximum I^2t for fusing	320	KA ² s	t = 10ms No voltage reappplied
	292		t = 8.3ms reappplied
	226		t = 10ms 100% V_{RRM} reappplied
	207		t = 8.3ms reappplied
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	3200	KA ² √s	t = 0.1 to 10ms, no voltage reappplied
$V_{T(TO)1}$ Low level value of threshold voltage	0.97	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.
$V_{T(TO)2}$ High level value of threshold voltage	0.98		$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ max.
r_{t1} Low level value of on-state slope resistance	0.74	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ max.
r_{t2} High level value of on-state slope resistance	0.73		$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ max.
V_{TM} Max. on-state voltage	1.66	V	$I_{pk} = 940A$, $T_J = T_J$ max, $t_p = 10ms$ sine pulse
I_H Maximum holding current	600	mA	$T_J = 25^\circ C$, anode supply 12V resistive load
I_L Typical latching current	1000		

Switching

Parameter	ST300S	Units	Conditions
di/dt Max. non-repetitive rate of rise of turned-on current	1000	A/μs	Gate drive 20V, 20Ω, t _r ≤ 1μs T _J = T _J max, anode voltage ≤ 80% V _{DRM}
t _d Typical delay time	1.0	μs	Gate current 1A, di _g /dt = 1A/μs V _d = 0.67% V _{DRM} , T _J = 25°C
t _q Typical turn-off time	100		I _{TM} = 550A, T _J = T _J max, di/dt = 40A/μs, V _R = 50V dv/dt = 20V/μs, Gate 0V 100Ω, t _p = 500μs

Blocking

Parameter	ST300S	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	500	V/μs	T _J = T _J max. linear to 80% rated V _{DRM}
I _{RRM} I _{DRM} Max. peak reverse and off-state leakage current	50	mA	T _J = T _J max, rated V _{DRM} /V _{RRM} applied

Triggering

Parameter	ST300S		Units	Conditions
P _{GM} Maximum peak gate power	10.0		W	T _J = T _J max, t _p ≤ 5ms
P _{G(AV)} Maximum average gate power	2.0			T _J = T _J max, f = 50Hz, d% = 50
I _{GM} Max. peak positive gate current	3.0		A	T _J = T _J max, t _p ≤ 5ms
+V _{GM} Maximum peak positive gate voltage	20		V	T _J = T _J max, t _p ≤ 5ms
-V _{GM} Maximum peak negative gate voltage	5.0			
I _{GT} DC gate current required to trigger	TYP.	MAX.	mA	T _J = - 40°C T _J = 25°C T _J = 125°C Max. required gate trigger/ current/ voltage are the lowest value which will trigger all units 12V anode-to-cathode applied
	200	-		
	100	200		
V _{GT} DC gate voltage required to trigger	2.5	-	V	T _J = - 40°C T _J = 25°C T _J = 125°C
	1.8	3		
	1.1	-		
I _{GD} DC gate current not to trigger	10.0		mA	T _J = T _J max Max. gate current/ voltage not to trigger is the max. value which will not trigger any unit with rated V _{DRM} anode-to-cathode applied
V _{GD} DC gate voltage not to trigger	0.25		V	

ST300S Series

Bulletin I25158 rev. B 01/94

International
IRF Rectifier

Thermal and Mechanical Specification

Parameter	ST300S	Units	Conditions
T_J Max. operating temperature range	-40 to 125	°C	
T_{stg} Max. storage temperature range	-40 to 150		
R_{thJC} Max. thermal resistance, junction to case	0.10	K/W	DC operation
R_{thCS} Max. thermal resistance, case to heatsink	0.03		Mounting surface, smooth, flat and greased
T Mounting torque, $\pm 10\%$	48.5 (425)	Nm (lbf-in)	Non lubricated threads
wt Approximate weight	535	g	
Case style	TO - 209AE (TO-118)		See Outline Table

ΔR_{thJC} Conduction

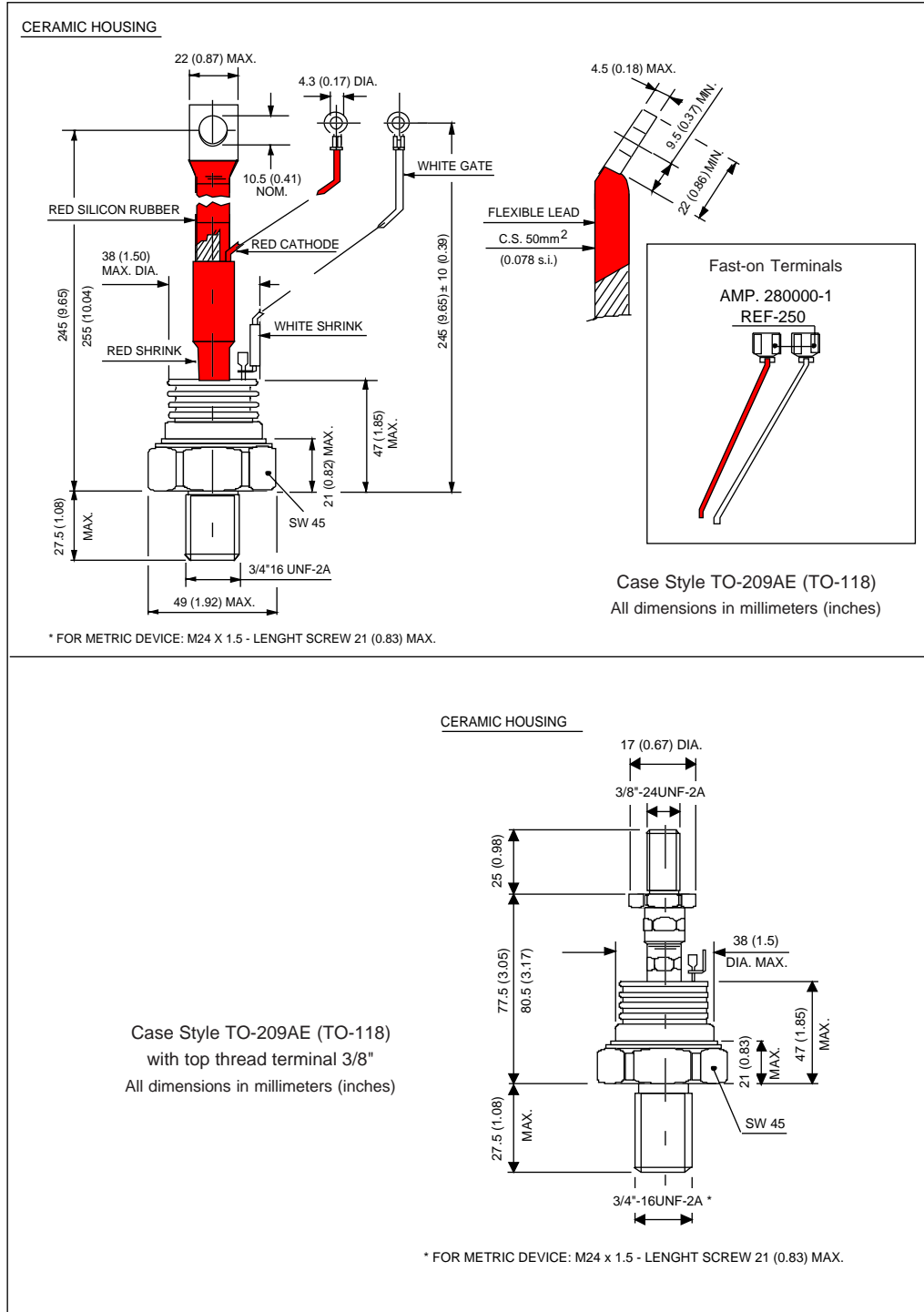
(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction	Rectangular conduction	Units	Conditions
180°	0.011	0.008	K/W	$T_J = T_J \text{ max.}$
120°	0.013	0.014		
90°	0.017	0.018		
60°	0.025	0.026		
30°	0.041	0.042		

Ordering Information Table

Device Code	
1	- Thyristor
2	- Essential part number
3	- 0 = Converter grade
4	- S = Compression bonding Stud
5	- Voltage code: Code x 100 = V_{RRM} (See Voltage Rating Table)
6	- P = Stud base 16UNF threads M = Stud base metric threads (M24 x 1.5)
7	- 0 = Eyelet terminals (Gate and Auxiliary Cathode Leads) 1 = Fast - on terminals (Gate and Auxiliary Cathode Leads) 3 = Threaded top terminal 3/8" 24UNF-2A
8	- Critical dv/dt: None = 500V/ μ sec (Standard value) L = 1000V/ μ sec (Special selection)

Outline Table



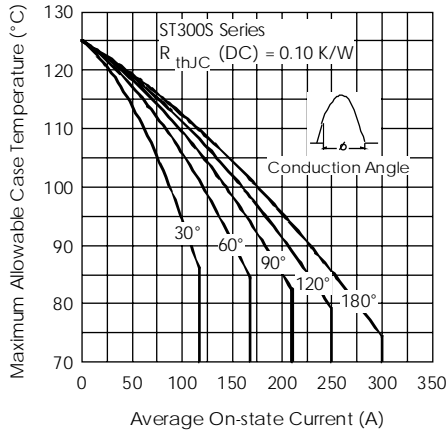


Fig. 1 - Current Ratings Characteristics

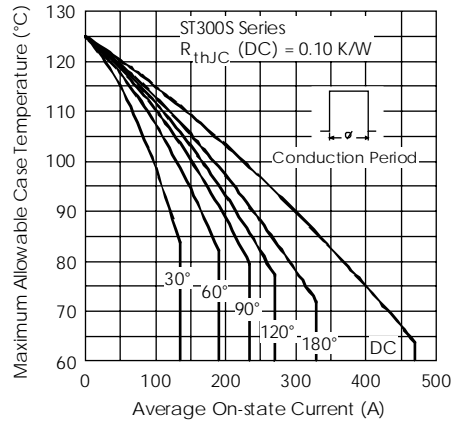


Fig. 2 - Current Ratings Characteristics

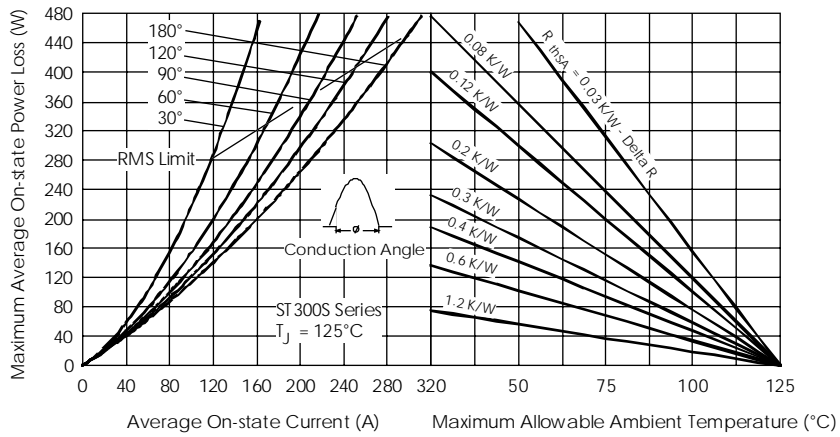


Fig. 3 - On-state Power Loss Characteristics

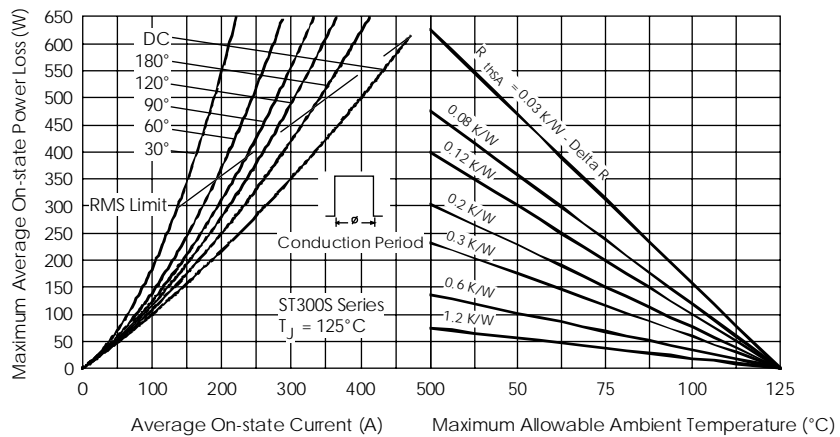


Fig. 4 - On-state Power Loss Characteristics

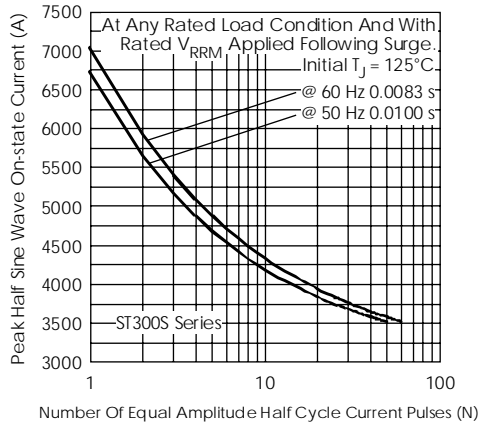


Fig. 5 - Maximum Non-Repetitive Surge Current

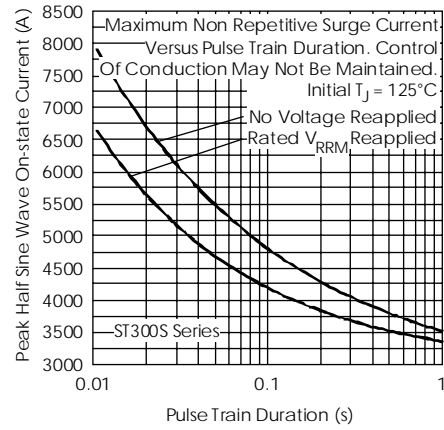


Fig. 6 - Maximum Non-Repetitive Surge Current

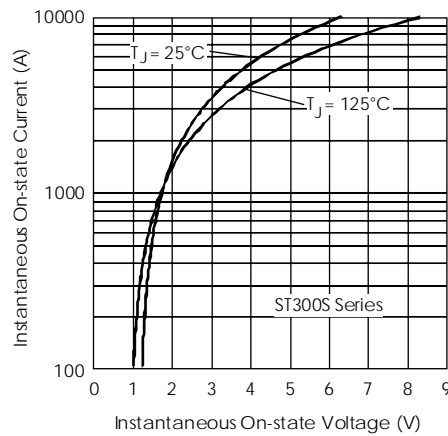


Fig. 7 - On-state Voltage Drop Characteristics

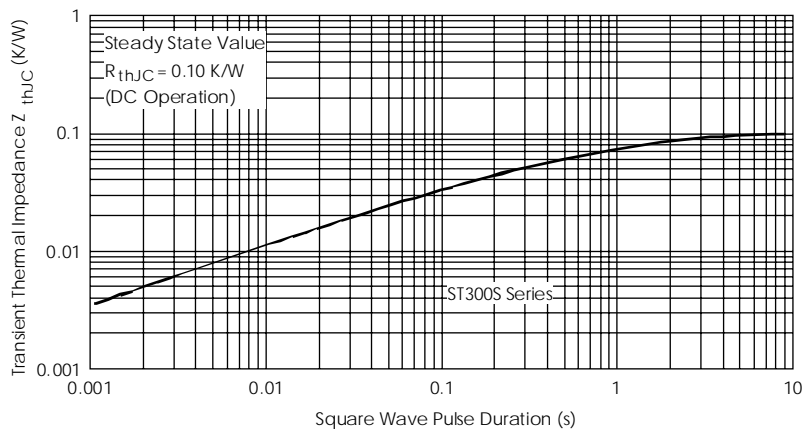


Fig. 8 - Thermal Impedance Z_{thJC} Characteristic

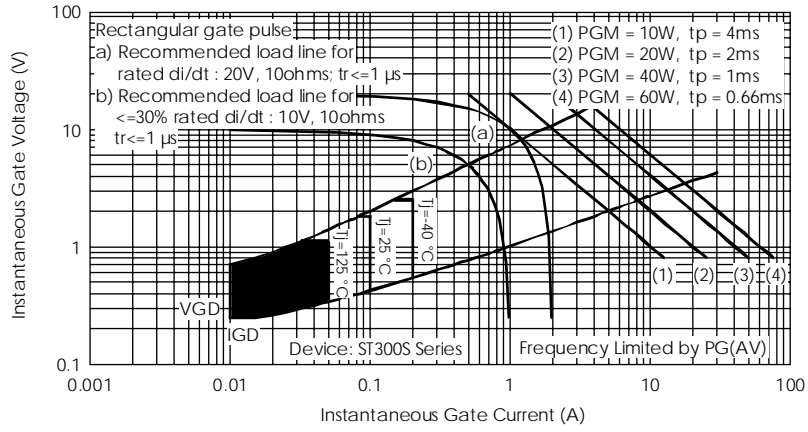


Fig. 9 - Gate Characteristics