

Features

- CMOS Low Power (Typ)..... 150mW
- Parallel Conversion Technique
- Sampling Rate at 5V Supply 15MHz
- 8-Bit Latched Three-State Output with Overflow Bit
- Accuracy (Typ)..... ± 1 LSB
- Single Supply Voltage 4V to 7.5V
- Linearity (INL):
 - HI3318JIP ± 1.5 LSB
 - HI3318JIB ± 1.5 LSB
- Sampling Rate:
 - HI3318JIP 15MHz (67ns)
 - HI3318JIB 15MHz (67ns)
- Video Digitizing
- High-Speed A/D Conversion
- Medical Imaging
- Radar Signal Processing
- Digital Communications Systems

Description

The HI3318 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low power consumption and high speed digitization.

The HI3318 operates over a wide full scale input voltage range of 4V up to 7.5V with maximum power consumption depending upon the clock frequency selected. When operated from a 5V supply at a clock frequency of 15MHz, the typical power consumption of the HI3318 is 150mW.

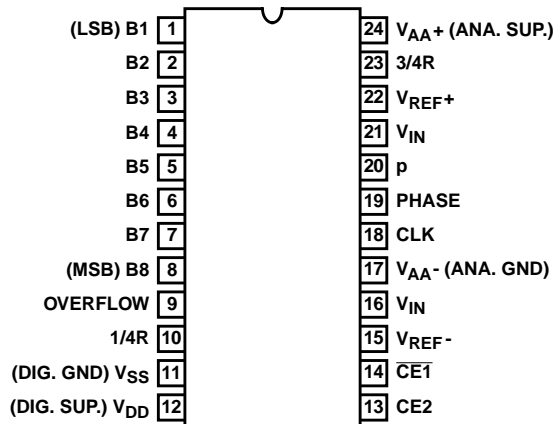
256 paralleled auto balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the HI3318. 255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

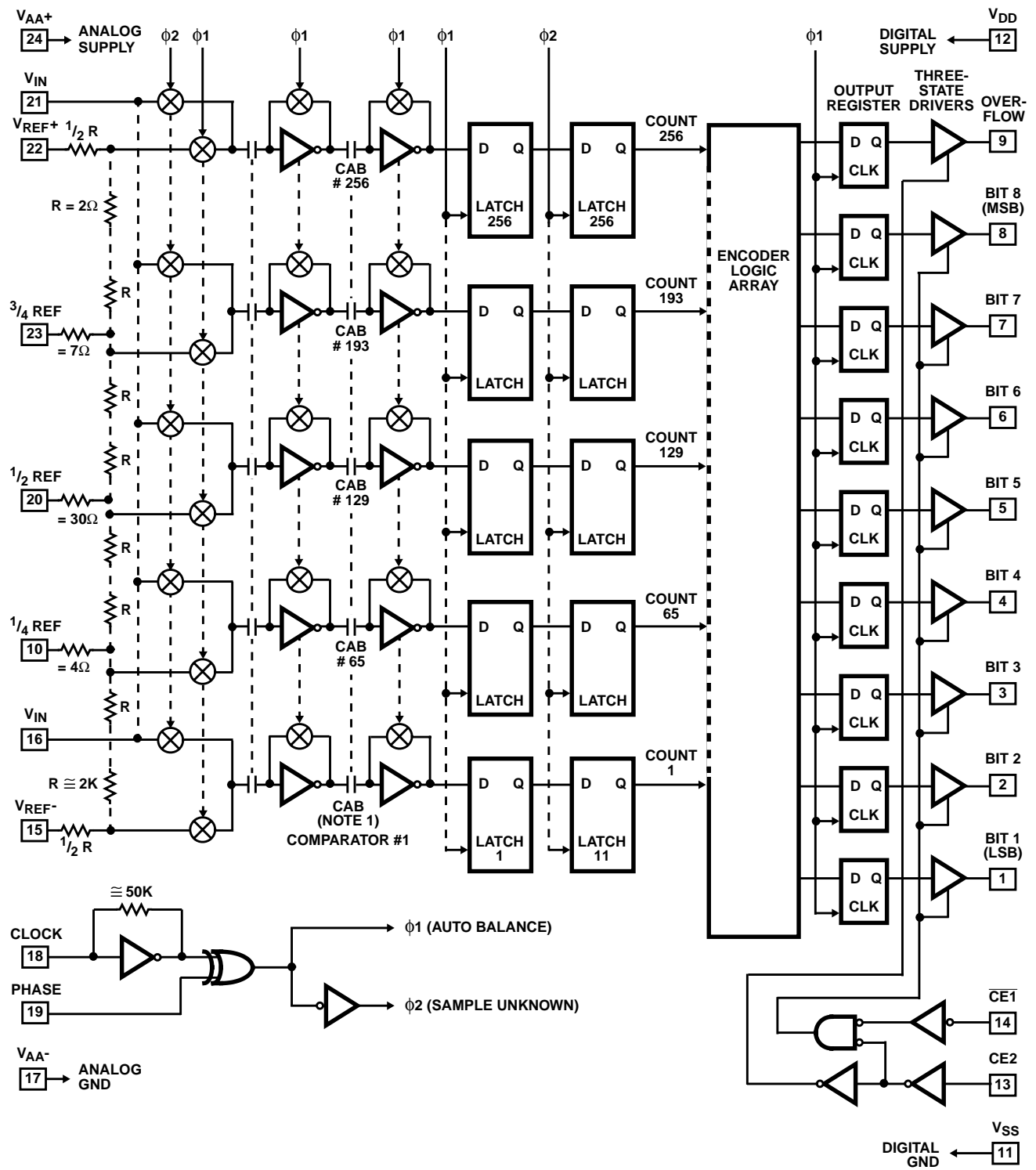
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|------------------|------------|----------|
| HI3318JIP | -40 to 85 | 24 Ld PDIP | E24.6 |
| HI3318JIB | -40 to 85 | 24 Ld SOIC | M24.3 |

Pinout

HI3318
(PDIP, SOIC)
TOP VIEW



Functional Block Diagram



NOTE:
1. Cascaded Auto Balance (CAB).

HI3318

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

| | |
|--|--|
| DC Supply Voltage Range (V_{DD} or V_{AA+}) | -0.5V to +8V (Referenced to V_{SS} or V_{AA-} Terminal, Whichever is More Negative) |
| Input Voltage Range | |
| CE2 and CE1 | $V_{AA-} - 0.5\text{V}$ to $V_{DD} + 0.5\text{V}$ |
| Clock, Phase, V_{REF-} , $1/2$ Ref. | $V_{AA-} - 0.5\text{V}$ to $V_{AA+} + 0.5\text{V}$ |
| Clock, Phase, V_{REF+} , $1/4$ Ref. | $V_{SS} - 0.5\text{V}$ to $V_{DD} + 0.5\text{V}$ |
| V_{IN} , $3/4$ REF, V_{REF+} | $V_{AA-} - 0.5\text{V}$ to $V_{AA-} + 7.5\text{V}$ |
| Output Voltage Range, Bits 1-8, Overflow (Outputs Off) | $V_{SS} - 0.5\text{V}$ to $V_{DD} + 0.5\text{V}$ |
| DC Input Current | $\pm 20\text{mA}$ |
| Clock, Phase, CE1, CE2, V_{IN} , Bits 1-8, Overflow | |
| Recommended V_{AA+} Operating Range | $V_{DD} \pm 1\text{V}$ |
| Recommended V_{AA-} Operating Range | $V_{SS} \pm 1\text{V}$ |

Thermal Information

| | |
|---|--|
| Thermal Resistance (Typical, Note 1) | $\theta_{JA} (^{\circ}\text{C}/\text{W})$ |
| PDIP Package | 60 |
| SOIC Package | 75 |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only) | 300°C |

Operating Conditions

| | |
|---|---|
| Operating Voltage Range (V_{DD} or V_{AA+}) | 4V (Min) to 7.5V (Max) |
| Temperature Range (T_A) | -40°C to 85°C |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications At 25°C , $V_{AA+} = V_{DD} = 5\text{V}$, $V_{REF+} = 6.4\text{V}$, $V_{REF-} = V_{AA-} = V_{SS}$, CLK = 15MHz, All Reference Points Adjusted, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|------|-----|-----------|----------|
| SYSTEM PERFORMANCE | | | | | |
| Resolution | | 8 | - | - | Bits |
| Integral Linearity Error | | - | - | ± 1.5 | LSB |
| Differential Linearity Error | | - | - | +1, -0.8 | LSB |
| Offset Error, Unadjusted | $V_{IN} = V_{REF-} + 1/2$ LSB | -0.5 | 4.5 | 6.4 | LSB |
| Gain Error, Unadjusted | $V_{IN} = V_{REF+} - 1/2$ LSB | -1.5 | 0 | 1.5 | LSB |
| DYNAMIC CHARACTERISTICS | | | | | |
| Maximum Input Bandwidth | (Note 1) HI3318 | 2.5 | 5.0 | - | MHz |
| Maximum Conversion Speed | CLK = Square Wave | 15 | 17 | - | MSPS |
| Signal to Noise Ratio, SNR = $\frac{\text{RMS Signal}}{\text{RMS Noise}}$ | $f_S = 15\text{MHz}$, $f_{IN} = 100\text{kHz}$ | - | 47 | - | dB |
| | $f_S = 15\text{MHz}$, $f_{IN} = 4\text{MHz}$ | - | 43 | - | dB |
| Signal to Noise Ratio, SINAD = $\frac{\text{RMS Signal}}{\text{RMS Noise} + \text{Distortion}}$ | $f_S = 15\text{MHz}$, $f_{IN} = 100\text{kHz}$ | - | 45 | - | dB |
| | $f_S = 15\text{MHz}$, $f_{IN} = 4\text{MHz}$ | - | 35 | - | dB |
| Total Harmonic Distortion, THD | $f_S = 15\text{MHz}$, $f_{IN} = 100\text{kHz}$ | - | -46 | - | dBc |
| | $f_S = 15\text{MHz}$, $f_{IN} = 4\text{MHz}$ | - | -36 | - | dBc |
| Effective Number of Bits, ENOB | $f_S = 15\text{MHz}$, $f_{IN} = 100\text{kHz}$ | - | 7.2 | - | Bits |
| | $f_S = 15\text{MHz}$, $f_{IN} = 4\text{MHz}$ | - | 5.5 | - | Bits |
| Differential Gain Error | Unadjusted | - | 2 | - | % |
| Differential Phase Error | Unadjusted | - | 1 | - | % |
| ANALOG INPUTS | | | | | |
| Full Scale Range, V_{IN} and $(V_{REF+}) - (V_{REF-})$ | Notes 2, 4 | 4 | - | 7 | V |
| Input Capacitance, V_{IN} | | - | 30 | - | pF |
| Input Current, V_{IN} , (See Text) | $V_{IN} = 5.0\text{V}$, $V_{REF+} = 5.0\text{V}$ | - | - | 3.5 | mA |
| REFERENCE INPUTS | | | | | |
| Ladder Impedance | | 270 | 500 | 800 | Ω |

HI3318

Electrical Specifications At 25°C, $V_{AA+} = V_{DD} = 5V$, $V_{REF+} = 6.4V$, $V_{REF-} = V_{AA-} = V_{SS}$, CLK = 15MHz,
All Reference Points Adjusted, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------------------|-------------|-----------|-------------|---------|
| DIGITAL INPUTS | | | | | |
| Low Level Input Voltage, V_{OL} CE1, CE2 | Note 4 | - | - | $0.2V_{DD}$ | V |
| Phase, CLK | Note 4 | - | - | $0.2V_{AA}$ | V |
| High Level Input Voltage, V_{IN} CE1, CE2 | Note 4 | $0.7V_{DD}$ | - | - | V |
| Phase, CLK | Note 4 | $0.7V_{AA}$ | - | - | V |
| Input Leakage Current, I_I (Except CLK Input) | Note 3 | - | ± 0.2 | ± 5 | μA |
| Input Capacitance, C_I | | - | 3 | - | pF |
| DIGITAL OUTPUTS | | | | | |
| Output Low (Sink) Current | $V_O = 0.4V$ | 4 | 10 | - | mA |
| Output High (Source) Current | $V_O = 4.5V$ | -4 | -6 | - | mA |
| Three-State Output Off-State Leakage Current, I_{OZ} | | - | ± 0.2 | ± 5 | μA |
| Output Capacitance, C_O | | - | 4 | - | pF |
| TIMING CHARACTERISTICS | | | | | |
| Auto Balance Time, ϕ_1 | | 33 | - | ∞ | ns |
| Sample Time, ϕ_2 | Note 4 | 25 | - | 500 | ns |
| Aperture Delay | | - | 15 | - | ns |
| Aperture Jitter | | - | 100 | - | ps |
| Data Valid Time, t_D | Note 4 | - | 50 | 65 | ns |
| Data Hold Time, t_H | Note 4 | 25 | 40 | - | ns |
| Output Enable Time, t_{EN} | | - | 18 | - | ns |
| Output Disable Time, t_{DIS} | | - | 18 | - | ns |
| POWER SUPPLY CHARACTERISTICS | | | | | |
| Device Current ($I_{DD} + I_A$) (Excludes I_{REF}) | Continuous Conversion (Note 4) | - | 30 | 60 | mA |
| | Auto Balance (ϕ_1) | - | 30 | 60 | mA |

NOTES:

1. A full scale sine wave input of greater than $f_{CLK}/2$ or the specified input bandwidth (whichever is less) may cause an erroneous code. The -3dB bandwidth for frequency response purposes is greater than 30MHz.
2. V_{IN} (Full Scale) or V_{REF+} should not exceed $V_{AA+} + 1.5V$ for accuracy.
3. The clock input is a CMOS inverter with a 50kΩ feedback resistor and may be AC coupled with 1V_{p-p} minimum source.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Waveforms

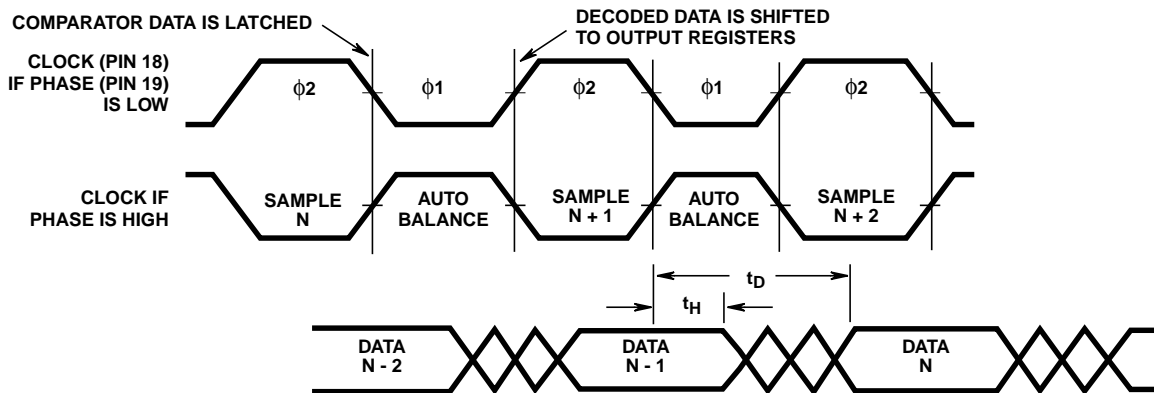


FIGURE 1. INPUT TO OUTPUT TIMING DIAGRAM

Timing Waveforms (Continued)

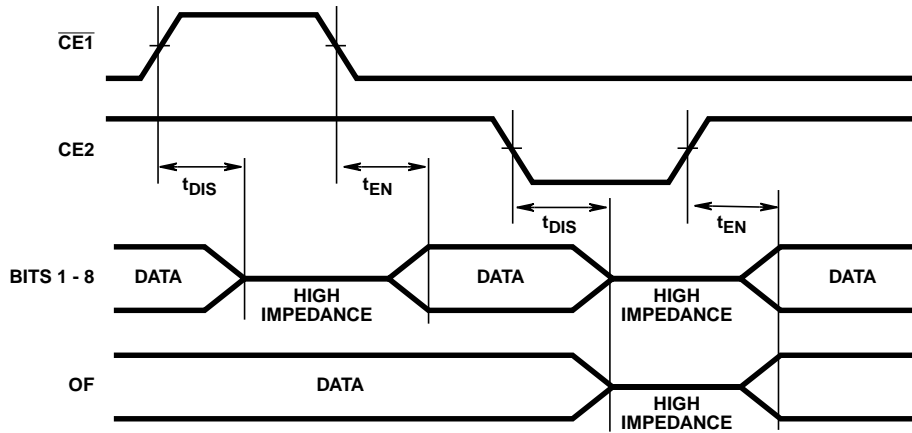


FIGURE 2. OUTPUT ENABLE TIMING DIAGRAM

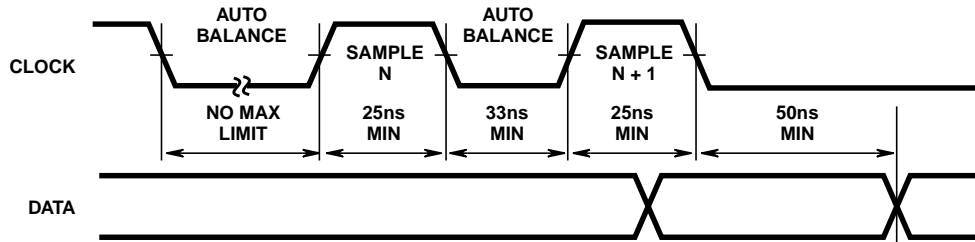


FIGURE 3A. STANDBY IN INDEFINITE AUTO BALANCE (SHOWN WITH PHASE = LOW)

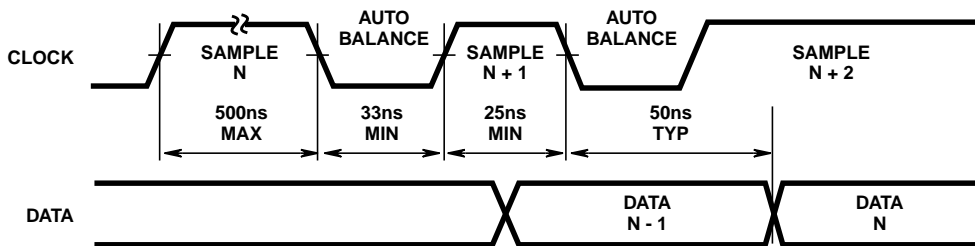


FIGURE 3B. STANDBY IN SAMPLE (SHOWN WITH PHASE = LOW)

FIGURE 3. PULSE MODE OPERATION

Typical Performance Curves

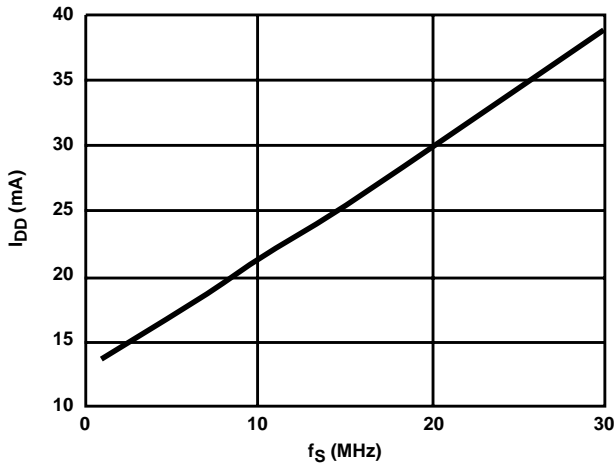


FIGURE 4. DEVICE CURRENT vs SAMPLE FREQUENCY

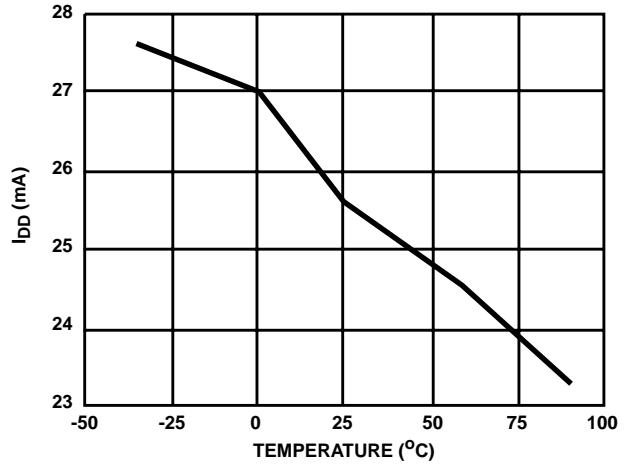


FIGURE 5. DEVICE CURRENT vs TEMPERATURE

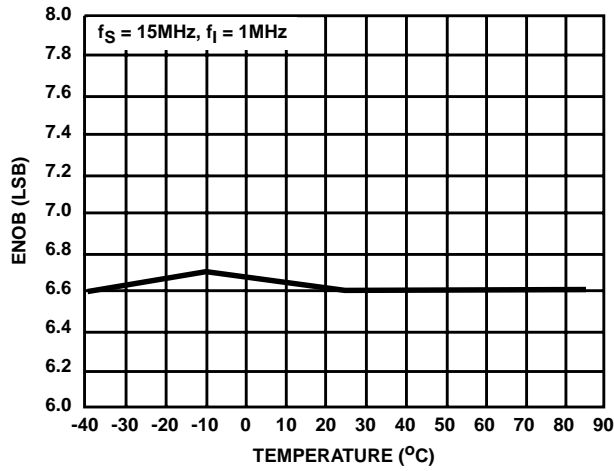


FIGURE 6. ENOB vs TEMPERATURE

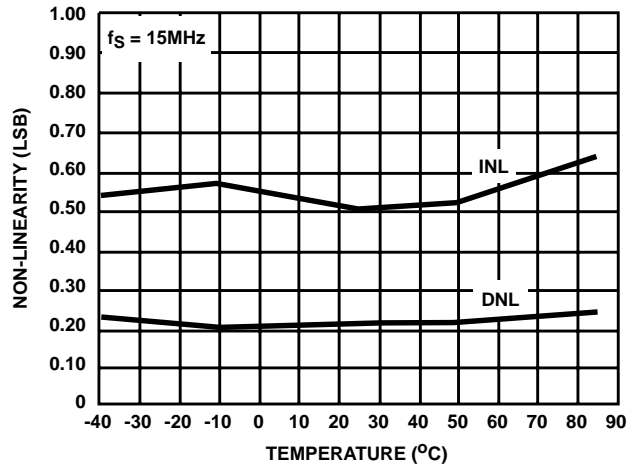


FIGURE 7. NON-LINEARITY vs TEMPERATURE

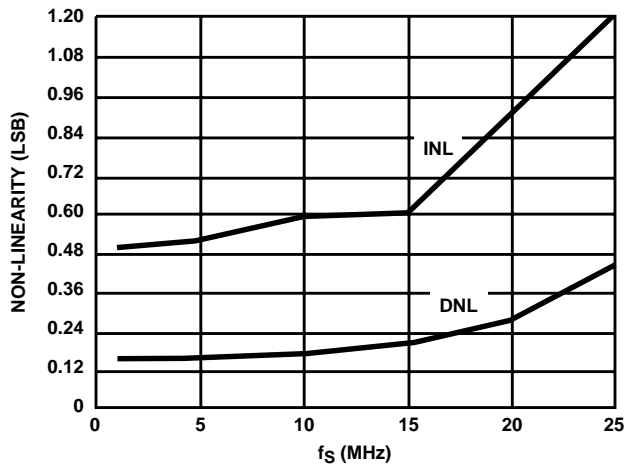


FIGURE 8. NON-LINEARITY vs SAMPLE FREQUENCY

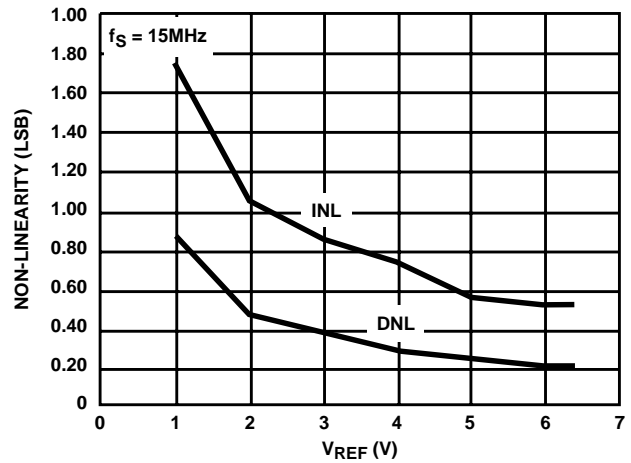


FIGURE 9. NON-LINEARITY vs REFERENCE VOLTAGE

Typical Performance Curves (Continued)

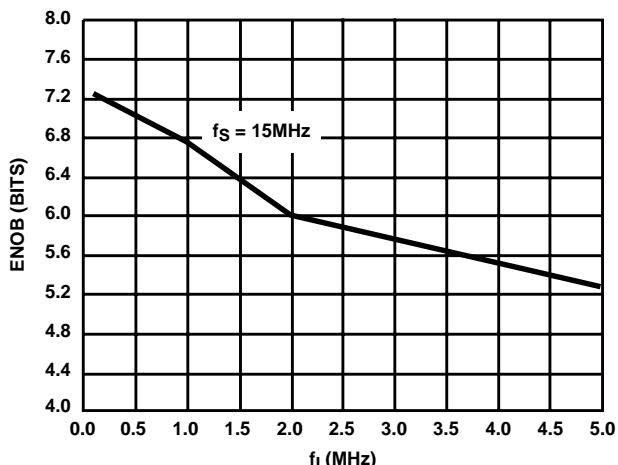


FIGURE 10. ENOB vs INPUT FREQUENCY

Pin Descriptions

| PIN | NAME | DESCRIPTION |
|-----|-------------------|---|
| 1 | B1 | Bit 1 (LSB) |
| 2 | B2 | Bit 2 |
| 3 | B3 | Bit 3 |
| 4 | B4 | Bit 4 |
| 5 | B5 | Bit 5 |
| 6 | B6 | Bit 6 |
| 7 | B7 | Bit 7 |
| 8 | B8 | Bit 8 (MSB) |
| 9 | OF | Overflow |
| 10 | 1/4 R | Reference Ladder 1/4 Point |
| 11 | V _{SS} | Digital Ground |
| 12 | V _{DD} | Digital Power Supply, +5V |
| 13 | CE2 | Three-State Output Enable Input, Active Low, See Truth Table. |
| 14 | CE1 | Three-State Output Enable Input Active High. See Truth Table. |
| 15 | V _{REF-} | Reference Voltage Negative Input |
| 16 | V _{IN} | Analog Signal Input |
| 17 | V _{AA-} | Analog Ground |
| 18 | CLK | Clock Input |
| 19 | PHASE | Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text). |
| 20 | 1/2 R | Reference Ladder Midpoint |
| 21 | V _{IN} | Analog Signal Input |
| 22 | V _{REF+} | Reference Voltage Positive Input |
| 23 | 3/4 R | Reference Ladder 3/4 Point |
| 24 | V _{AA+} | Analog Power Supply, +5V |

CHIP ENABLE TRUTH TABLE

| CE1 | CE2 | B1 - B8 | OF |
|-----|-----|-------------|-------------|
| 0 | 1 | Valid | Valid |
| 1 | 1 | Three-State | Valid |
| X | 0 | Three-State | Three-State |

X = Don't Care

Theory of Operation

A sequential parallel technique is used by the HI3318 converter to obtain its high speed operation. The sequence consists of the "Auto-Balance" phase, φ1, and the "Sample Unknown" phase, φ2. (Refer to the circuit diagram.) Each conversion takes one clock cycle (see Note). With the phase control (pin 19) high, the "Auto-Balance" (φ1) occurs during the high period of the clock cycle, and the "Sample Unknown" (φ2) occurs during the low period of the clock cycle.

NOTE: The device requires only a single phase clock. The terminology of φ1 and φ2 refers to the high and low periods of the same clock.

During the "Auto-Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(N/256) V_{REF}] - (1/512) V_{REF} \\ = [(2N - 1)/512] V_{REF}$$

Where:

$$V_{TAP}(n) = \text{reference ladder tap voltage at point } n, \\ V_{REF} = \text{voltage across } V_{REF-} \text{ to } V_{REF+}, \\ N = \text{tap number (1 through 256).}$$

The other side of these capacitors are connected to single-stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately (V_{AA+} - V_{AA-})/2. The first set of capacitors now charges to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers is also auto-balanced. The balancing of the second-

stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{IN} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{IN} will go to a "high" state at their outputs. All comparators that had tap voltages lower than V_{IN} will go to a "low" state.

The status of all these comparator amplifiers is AC coupled through the second-stage comparator and stored at the end of this phase (ϕ_2) by a latching amplifier stage. The latch feeds a second latching stage, triggered at the end of ϕ_1 . This delay allows comparators extra settling time. The status of the comparators is decoded by a 256 to 9-bit decoder array, and the results are clocked into a storage register at the end of the next ϕ_2 .

A 3-stage buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. CE1 will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device, a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous-Clock Operation

One complete conversion cycle can be traced through the HI3318 via the following steps. (Refer to timing diagram.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the first-stage latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto-balance" phase for the comparators. During this "low" state of the clock, the output of the latches settles and is captured by a second row of latches when the clock returns high. The second-stage latch output propagates through the decode array, and a 9-bit code appears at the D inputs of the output registers. On the next falling edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_D as valid data at the output of the three-state drivers. This also marks the end of the next "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse-Mode Operation

The HI3318 needs two of the same polarity clock edges to complete a conversion cycle: If, for instance, a negative going clock edge ends sample "N", then data "N" will appear after the next negative going edge. Because of this requirement, and because there is a maximum sample time of 500ns (due to capacitor droop), most pulse or intermittent sample applications will require double clock pulsing.

If an indefinite standby state is desired, standby should be in auto-balance, and the operation would be as in Figure 3A.

If the standby state is known to last less than 500ns and lowest average power is desired, then operation could be as in Figure 3B.

Increased Accuracy

In most cases the accuracy of the HI3318 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, five adjustments can be made to obtain better accuracy, i.e., offset trim; gain trim; and $1/4$, $1/2$ and $3/4$ point trim.

Offset Trim

In general, offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF-} input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is $1/2$ LSB. The equation is as follows:

$$V_{IN} (0 \text{ to } 1 \text{ transition}) = \frac{1}{2} \text{ LSB} = \frac{1}{2} (V_{REF}/256) = V_{REF}/512.$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50 Ω pot connected between V_{REF-} and ground will accomplish the adjustment. Set V_{IN} to $1/2$ LSB and trim the pot until the 0-to-1 transition occurs.

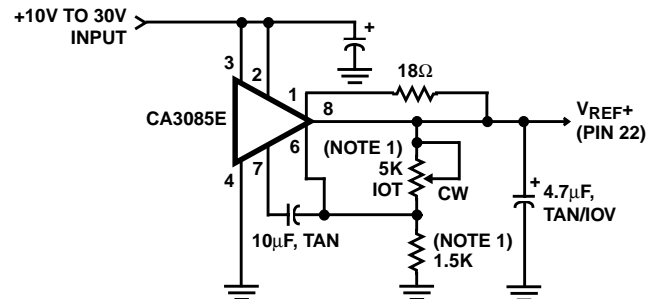
If V_{IN} for the first transition is greater than the theoretical, then the 50 Ω pot should be connected between V_{REF-} and a negative voltage of about 2 LSBs. The trim procedure is as stated previously.

Gain Trim

In general, the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 255 to overflow transition. That voltage is $1/3$ LSB less than V_{REF+} and is calculated as follows:

$$V_{IN} (255 \text{ to } 256 \text{ transition}) = V_{REF} - V_{REF}/512 = V_{REF}(511/512).$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 255 to overflow transition. Now adjust V_{REF+} until that transition occurs on the outputs.

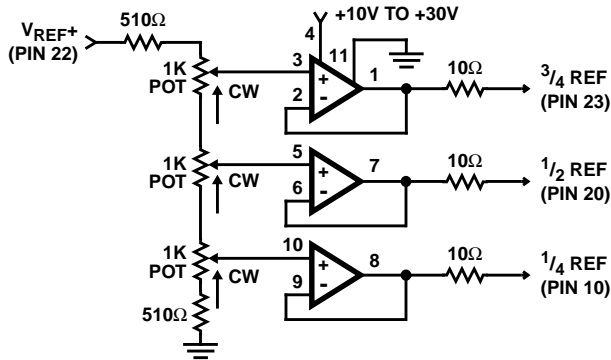


NOTE: Bypass V_{REF+} to analog GND near A/D with 0.1 μ F ceramic cap. Parts noted should have low temperature drift.

FIGURE 11. TYPICAL VOLTAGE REFERENCE SOURCE FOR DRIVING V_{REF+} INPUT

1/4 Point Trims

The 1/4, 1/2 and 3/4 points on the reference ladder are brought out for linearity adjusting or if the user wishes to create a nonlinear transfer function. The 1/4 points can be driven by the reference drivers shown (Figure 12) or by 2-K pots connected between V_{REF+} and V_{REF-}. The 1/2 (mid-) point should be set first by applying an input of 257/512 x (V_{REF}) and adjusting for an output changing from 128 to 129. Similarly the 1/4 and 3/4 points can be set with inputs of 129/512 and 385/512 x (V_{REF}) and adjusting for counts of 192 to 193 and 64 to 65. (Note that the points are actually 1/4, 1/2 and 3/4 of full scale +1 LSB.)



NOTES:

1. All Op Amps = 3/4 CA324E.
2. Bypass all reference points to analog ground near A/D with 0.1μF ceramic caps.
3. Adjust V_{REF+} first, then 1/3, 3/4 and 1/4 points.

FIGURE 12. TYPICAL 1/4 POINT DRIVERS FOR ADJUSTING LINEARITY (USE FOR MAXIMUM LINEARITY)

9-Bit Resolution

To obtain 9-bit resolution, two HI3318s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls, all of which are available on the HI3318.

The first step for connecting a 9-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the ninth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the CE1 control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 8) are now connected in parallel to complete the circuitry. The complete circuit for a 9-bit A/D converter is shown in Figure 14.

Grounding/Bypassing

The analog and digital supply grounds of a system should be kept separate and only connected at the A/D. This keeps digital ground noise out of the analog data to be converted. Reference drivers, input amps, reference taps, and the V_{AA}

supply should be bypassed at the A/D to the analog side of the ground. See Figure 15 for a block diagram of this concept. All capacitors shown should be low impedance 0.1μF ceramics and should be mounted as close to the A/D as possible. If V_{AA+} is derived from V_{DD}, a small (10Ω resistor or inductor and additional filtering (4.7μF tantalum) may be used to keep digital noise out of the analog system.

Input Loading

The HI3318 outputs a current pulse to the V_{IN} terminal at the start of every sample period. This is due to capacitor charging and switch feedthrough and varies with input voltage and sampling rate. The signal source must be capable of recovering from the pulse before the end of the sample period to guarantee a valid signal for the A/D to convert. Suitable high speed amplifiers include the HA-5033, HA-2542; and CA3450. Figure 16 is an example of an amplifier which recovers fast enough for sampling at 15MHz.

Output Loading

The CMOS digital output stage, although capable of driving large loads, will reflect these loads into the local ground. It is recommended that a local QMOS buffer such as CD74HC541 E be used to isolate capacitive loads.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the converter. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full scale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02,$$

where: V_{CORR} = 0.5dB.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

HI3318

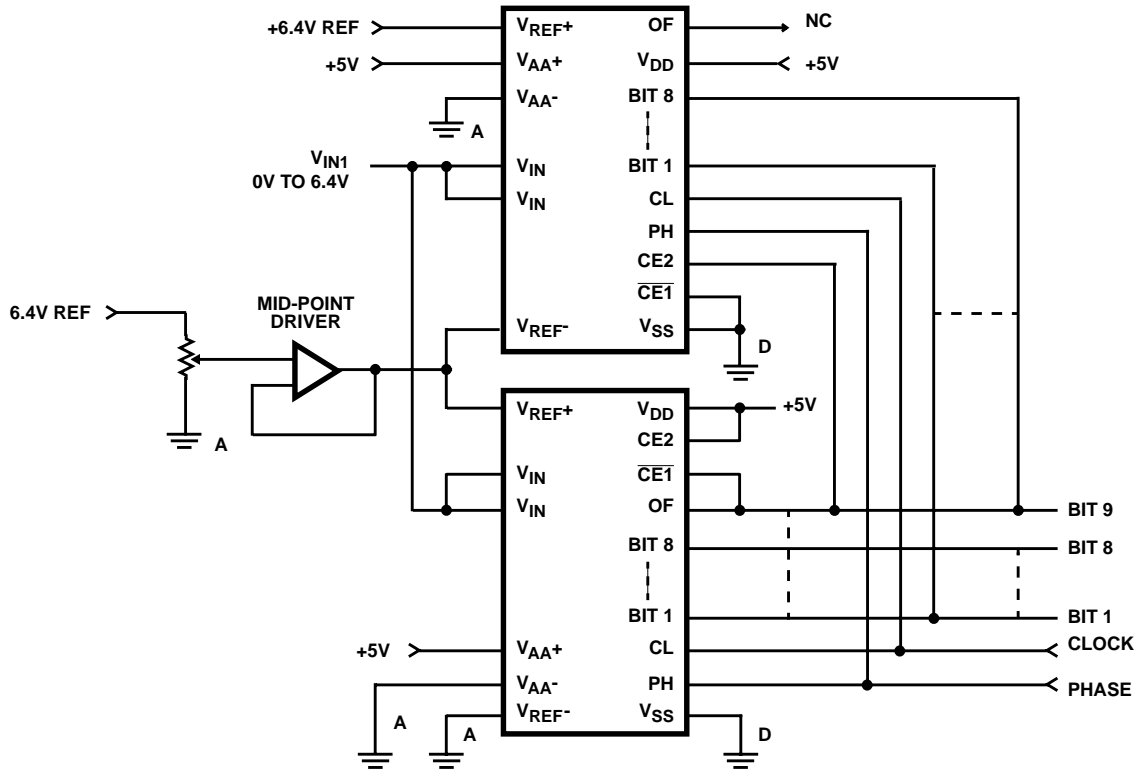


FIGURE 13. USING TWO HI3318s FOR 9-BIT RESOLUTION

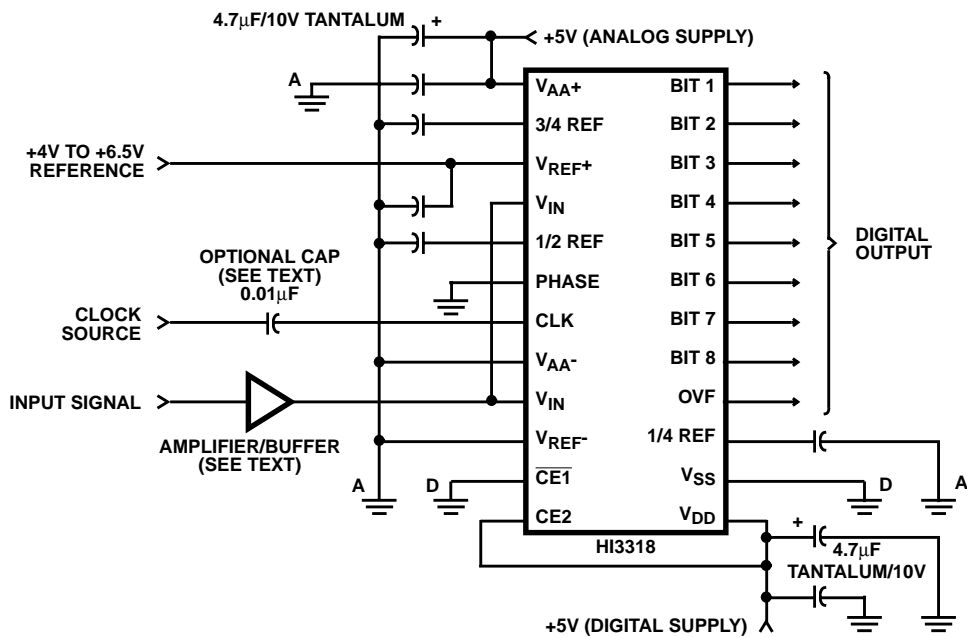


FIGURE 14. TYPICAL CIRCUIT CONFIGURATION FOR THE HI3318 WITH NO LINEARITY ADJUST

HI3318

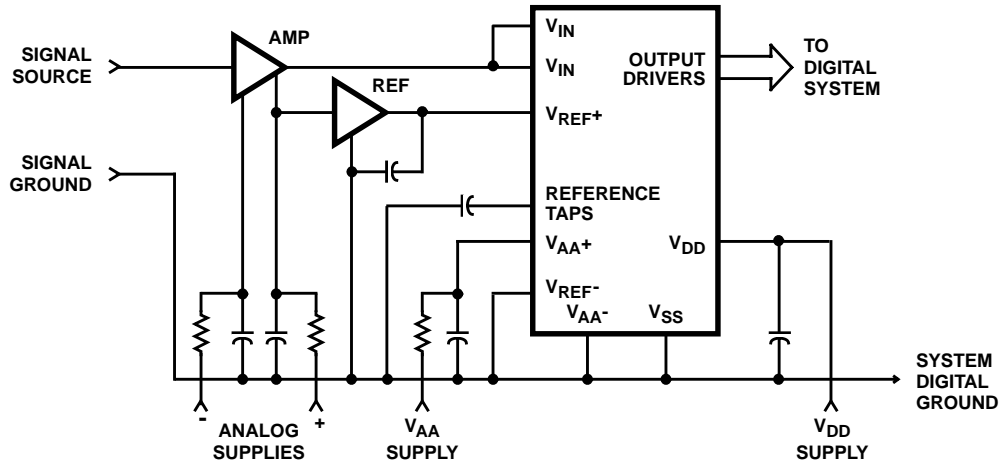
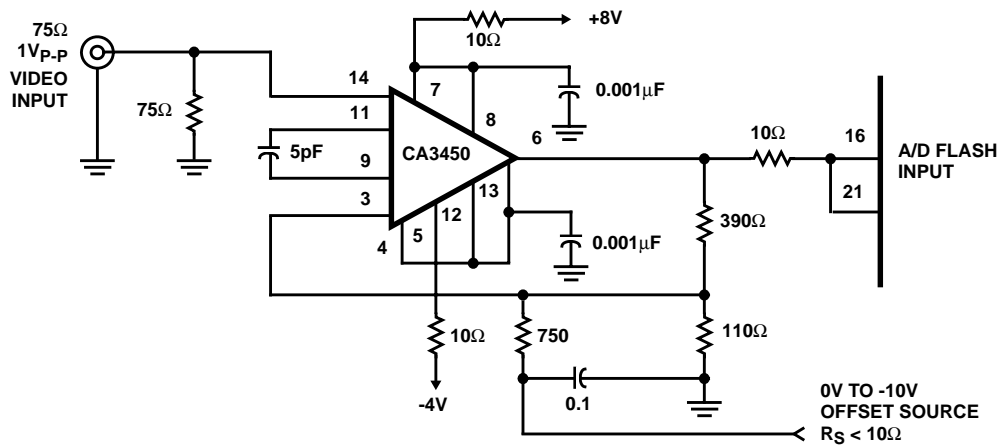


FIGURE 15. TYPICAL SYSTEM GROUNDING/BYPASSING



NOTE: Ground-planing and tight layout are extremely important.

FIGURE 16. TYPICAL HIGH BANDWIDTH AMPLIFIER FOR DRIVING THE HI3318

TABLE 1. OUTPUT CODE TABLE

| CODE DESCRIPTION | (NOTE 1) INPUT VOLTAGE | | BINARY OUTPUT CODE | | | | | | | | | DECIMAL COUNT |
|------------------------|-------------------------------|-------------------------------|--------------------|-----------|----|----|----|----|----|----|-----------|---------------|
| | V _{REF} 6.40V (V) | V _{REF} 5.12V (V) | OF | MSB B8 | B7 | B6 | B5 | B4 | B3 | B2 | LSB B1 | |
| Zero | 0.00 | 0.00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 LSB | 0.025 | 0.02 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 2 LSB | 0.05 | 0.04 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| 1/4 Full Scale | 1.60 | 1.28 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 64 |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| 1/2 Full Scale - 1 LSB | 3.175 | 2.54 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |
| 1/2 Full Scale | 3.20 | 2.56 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 128 |
| 1/2 Full Scale + 1 LSB | 3.225 | 2.58 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 129 |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| 3/4 Full Scale | 4.80 | 3.84 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 192 |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| • | • | • | | | | | | | | | • | • |
| Full Scale - 1 LSB | 6.35 | 5.08 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254 |
| Full Scale | 6.375 | 5.10 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |
| Over Flow | 6.40 | 5.12 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 511 |

NOTE: 1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Reducing Power

Most power is consumed while in the auto-balance state. When operating at lower than 15MHz clock speed, power can be reduced by stretching the sample (ϕ_2) time. The constraints are a minimum balance time (ϕ_1) of 33ns, and a maximum sample time of 500ns. Longer sample times cause droop in the auto-balance capacitors. Power can also be reduced in the reference string by switching the reference on only during auto-balance.

Clock Input

The Clock and Phase inputs feed buffers referenced to V_{AA+} and V_{AA-} . Phase should be tied to one of these two potentials, while the clock (if DC coupled) should be driven at least from 0.2 to 0.7 x ($V_{AA+} - V_{AA-}$). The clock may also be AC coupled with at least a 1V_{P-P} swing. This allows TTL drive levels or 5V QMOS levels when V_{AA+} is greater than 5V.

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