CMOS STATIC RAM
1 MEG (128K x 8-BIT)

IDT71024

FEATURES:
- 128K x 8 advanced high-speed CMOS static RAM
- Commercial (0° to 70°C), Industrial (-40° to 85°C) and Military (-55° to 125°C) temperature options
- Equal access and cycle times
  — Military: 15/17/20/25ns
  — Industrial: 15/20ns
  — Commercial: 12/15/17/20ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 300 and 400 mil Plastic SOJ, and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:
The IDT71024 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71024 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71024 is packaged in 32-pin 300 mil Plastic SOJ, 32-pin 400 mil Plastic SOJ, and 32-pin 400 x 820 mil LCC packages.

FUNCTIONAL BLOCK DIAGRAM
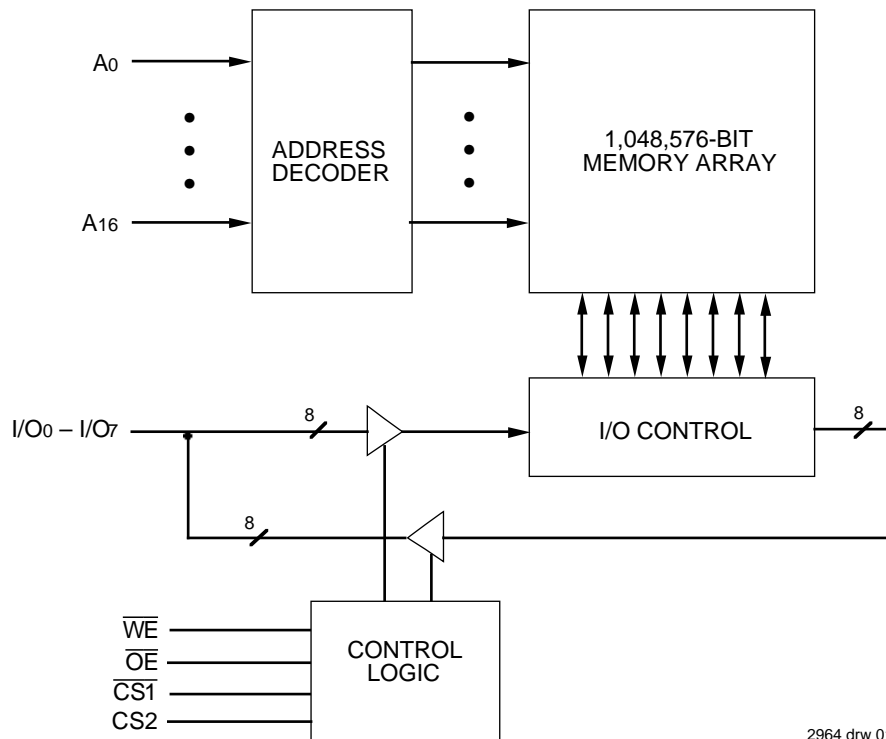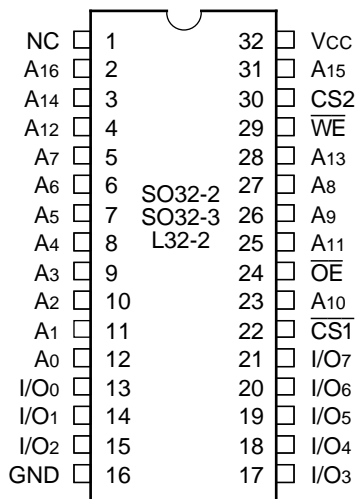

2964 drw 01

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MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES   **MAY 1997**

DSC-2964/08

PIN CONFIGURATION

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              ┌───∪───┐
       NC  ☐ 1      32 ☐ VCC
      A16  ☐ 2      31 ☐ A15
      A14  ☐ 3      30 ☐ CS2
      A12  ☐ 4      29 ☐ WE̅
       A7  ☐ 5      28 ☐ A13
       A6  ☐ 6  SO32-2  27 ☐ A8
       A5  ☐ 7  SO32-3  26 ☐ A9
       A4  ☐ 8  L32-2   25 ☐ A11
       A3  ☐ 9      24 ☐ OE̅
       A2  ☐ 10     23 ☐ A10
       A1  ☐ 11     22 ☐ CS1̅
       A0  ☐ 12     21 ☐ I/O7
     I/O0  ☐ 13     20 ☐ I/O6
     I/O1  ☐ 14     19 ☐ I/O5
     I/O2  ☐ 15     18 ☐ I/O4
      GND  ☐ 16     17 ☐ I/O3
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2964 drw 02

SOJ/LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l, Ind'l	Mil.	Unit
V_{TERM}[2]	Terminal Voltage Relative to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

2964 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE[1,2]

INPUTS				I/O	FUNCTION
WE̅	CS1̅	CS2	OE̅		
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}[3]	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}[3]	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

2964 tbl 01

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 0.5V
Industrial	-40°C to +85°C	0V	5.0V ± 0.5V
Military	-55°C to +125°C	0V	5.0V ± 0.5V

2964 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
2964 tbl 04
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71024		Unit
			Min.	Max.	
$|I_{LI}|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$|I_{LO}|$	Output Leakage Current	V_{CC} = Max., CS1̅ = V_{IH}, CS2 = V_{IL}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2964 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} − 0.2V)

Symbol	Parameter	71024S12		71024S15		71024S17		71024S20		71024S25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	160	—	155	180	150	170	140	160	—	145	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	35	—	35	40	35	40	35	40	—	35	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC}, or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0[2], V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	10	—	10	15	10	15	10	15	—	15	mA

NOTES: 2964 tbl 06
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} − 0.2V)

Symbol	Parameter	71024S15	71024S20	Unit
		Industrial	Industrial	
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	180	160	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	45	45	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC}, or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0[2], V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	15	15	mA

NOTES: 2964 tbl 07
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

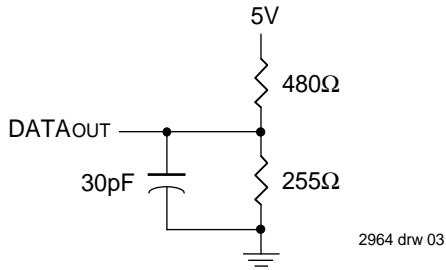**NOTE:**   2964 tbl 08
1. This parameter is guaranteed by device characterization, but is not production tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2964 tbl 09

Figure 1. AC Test Load
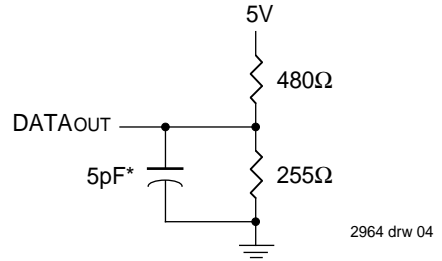
*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t$_{CLZ}$, t$_{OLZ}$, t$_{CHZ}$, t$_{OHZ}$, t$_{OW}$, and t$_{WHZ}$)

IDT71024
CMOS STATIC RAM 1MEG (128K x 8-BIT)   MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71024S12[1] Min.	Max.	71024S15 Min.	Max.	71024S17[3] Min.	Max.	71024S20 Min.	Max.	71024S25[2] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
tAA	Address Access Time	—	12	—	15	—	17	—	20	—	25	ns
tACS	Chip Select Access Time	—	12	—	15	—	17	—	20	—	25	ns
tCLZ[4]	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	3	—	ns
tCHZ[4]	Chip Deselect to Output in High-Z	0	6	0	7	0	8	0	8	0	10	ns
tOE	Output Enable to Output Valid	—	6	—	7	—	8	—	8	—	10	ns
tOLZ[4]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
tOHZ[4]	Output Disable to Output in High-Z	0	5	0	5	0	6	0	7	0	10	ns
tOH	Output Hold from Address Change	4	—	4	—	4	—	4	—	4	—	ns
tPU[4]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD[4]	Chip Deselect to Power-Down Time	—	12	—	15	—	17	—	20	—	25	ns
Write Cycle												
tWC	Write Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
tAW	Address Valid to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
tCW	Chip Select to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	13	—	15	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	7	—	8	—	9	—	9	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tOW[4]	Output Active from End-of-Write	3	—	3	—	3	—	4	—	4	—	ns
tWHZ[4]	Write Enable to Output in High-Z	0	5	0	5	0	7	0	8	0	9	ns

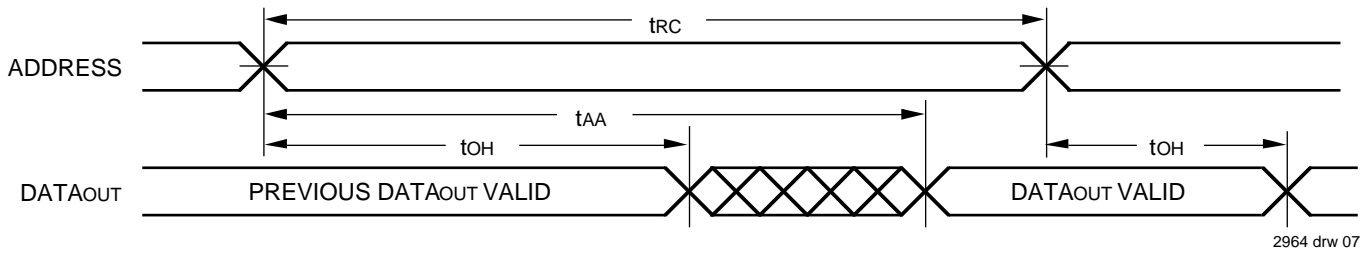**NOTES:**   2964 tbl 010
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. 0°C to +70°C and –55°C to +125°C temperature ranges only.
4. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
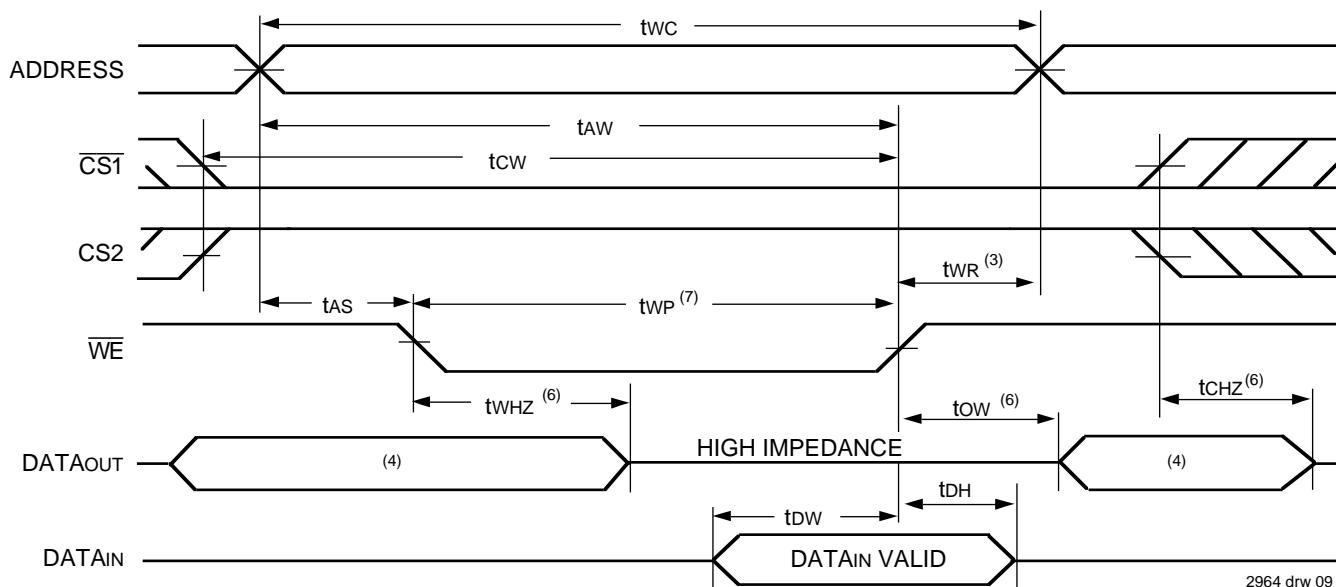
TIMING WAVEFORM OF READ CYCLE NO. 1[1]

2964 drw 06
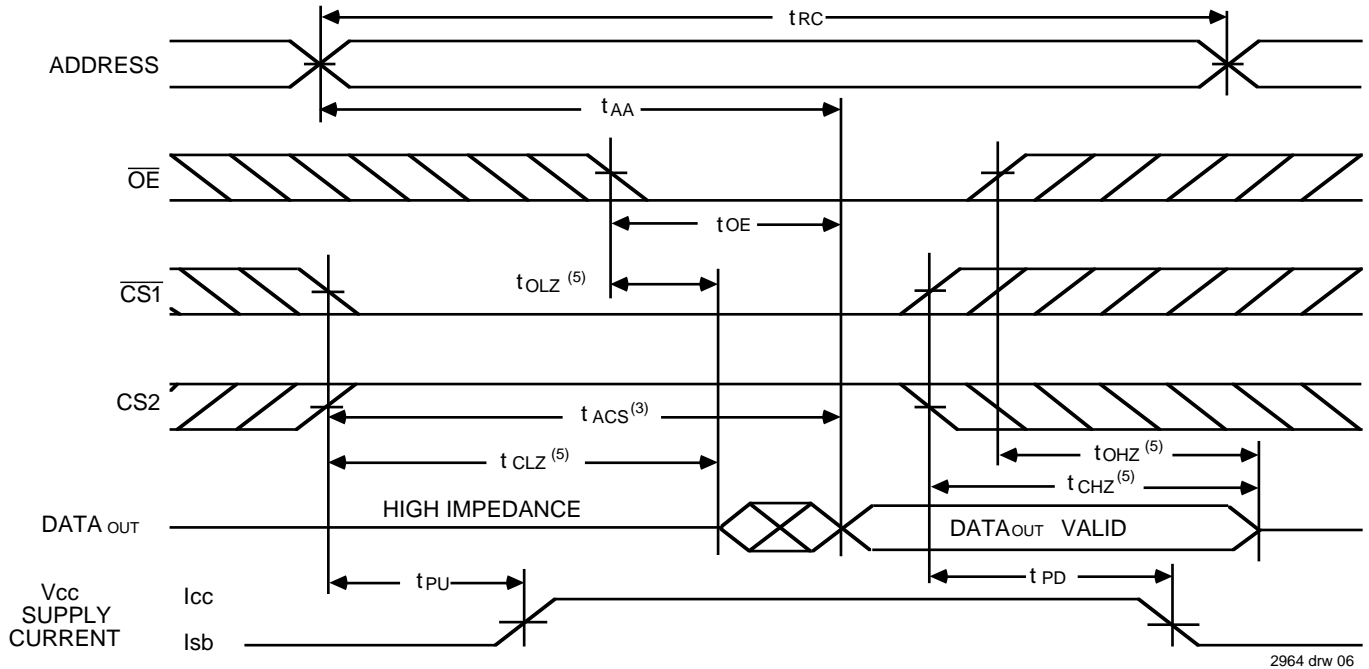
TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]

2964 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)[1, 2, 5, 7]

2964 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS1}}$ AND CS2 CONTROLLED TIMING)[1, 2, 5]
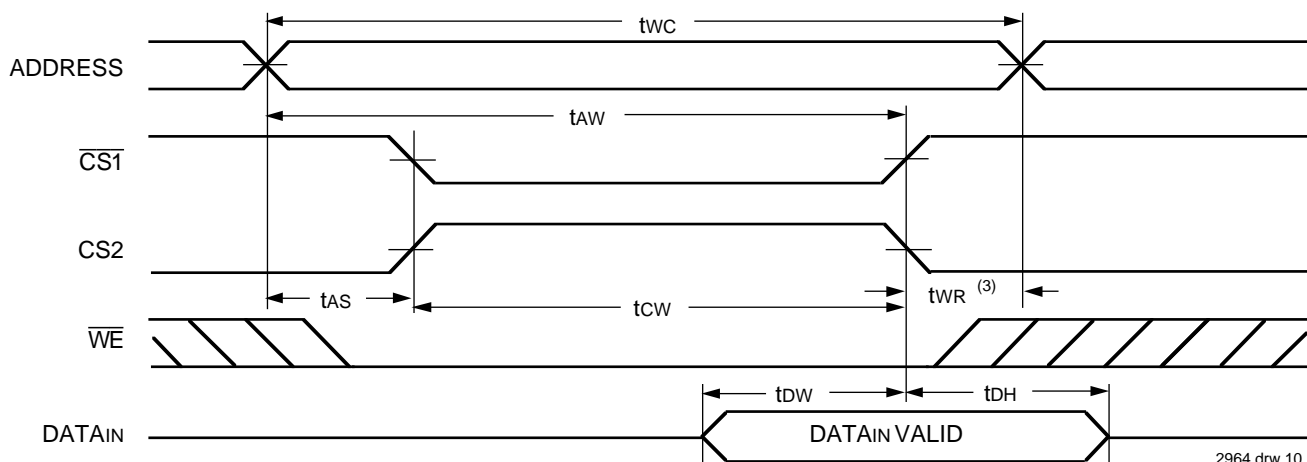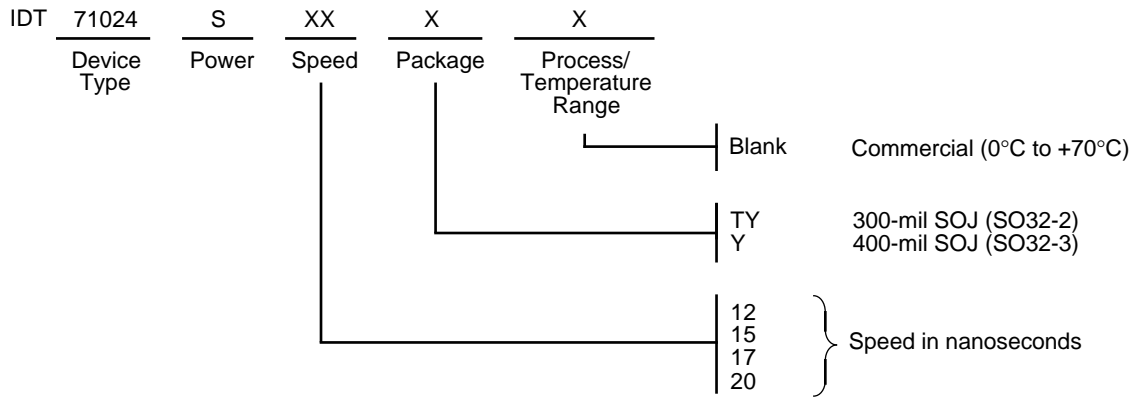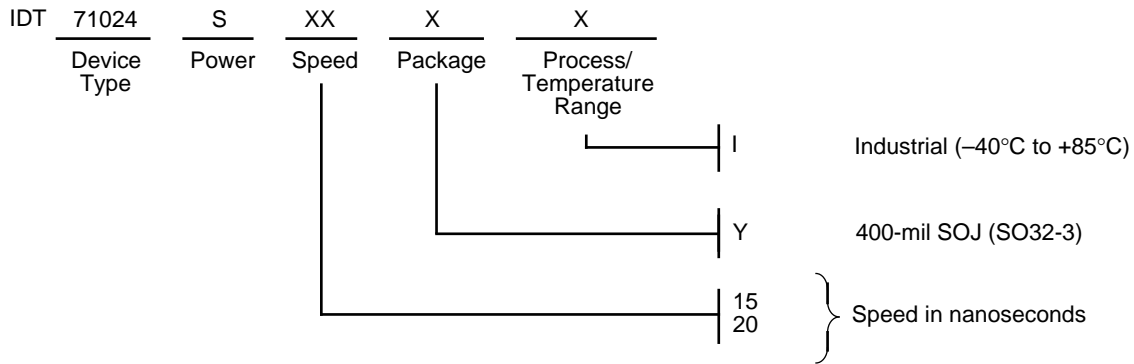

2964 drw 10

NOTES:
1. $\overline{\text{WE}}$ must be HIGH, $\overline{\text{CS1}}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{\text{CS1}}$, HIGH CS2, and a LOW $\overline{\text{WE}}$.
3. t_{WR} is measured from the earlier of either $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{\text{CS1}}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high impedance state. $\overline{\text{CS1}}$ and CS2 must both be active during the t_{CW} write period.
6. Transition is measured ±200mV from steady state.
7. $\overline{\text{OE}}$ is continuously HIGH. During a $\overline{\text{WE}}$ controlled write cycle with $\overline{\text{OE}}$ LOW, t_{WP} must be greater than or equal to t_{WHZ} + t_{DW} to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is HIGH during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
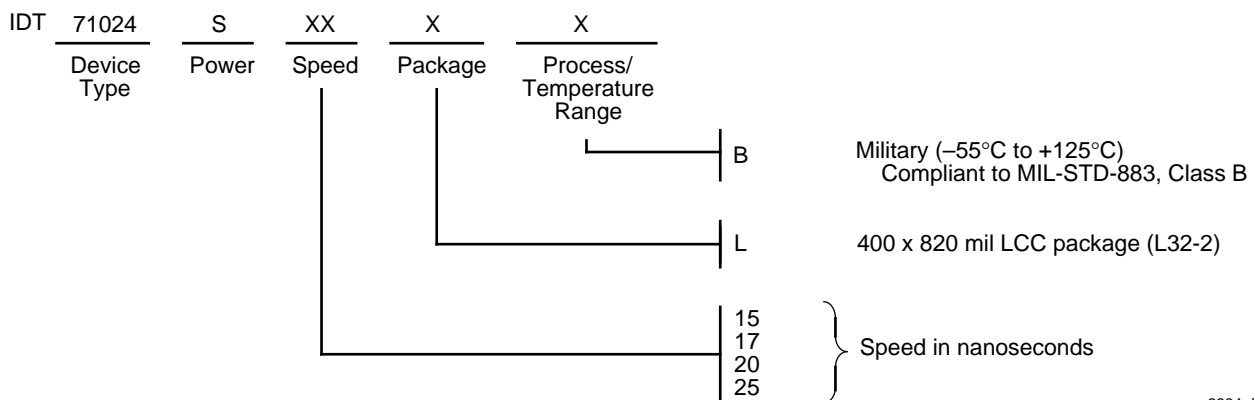
ORDERING INFORMATION

IDT   71024   S   XX   X   X

Device Type   Power   Speed   Package   Process/ Temperature Range

Blank   Commercial (0°C to +70°C)

TY   300-mil SOJ (SO32-2)
Y   400-mil SOJ (SO32-3)

12
15
17
20   } Speed in nanoseconds

2964 drw 11

IDT   71024   S   XX   X   X

Device Type   Power   Speed   Package   Process/ Temperature Range

I   Industrial (–40°C to +85°C)

Y   400-mil SOJ (SO32-3)

15
20   } Speed in nanoseconds

2964 drw 12

IDT   71024   S   XX   X   X

Device Type   Power   Speed   Package   Process/ Temperature Range

B   Military (–55°C to +125°C)
     Compliant to MIL-STD-883, Class B

L   400 x 820 mil LCC package (L32-2)

15
17
20
25   } Speed in nanoseconds

2964 drw 13