Document Title

8Mb SyncBurst Pipelined SRAM

Revision History

Revision No	History	Draft Date	Remark
0A	Initial Draft	September 24,2001	
0B	1. Move the $\overline{FT}$ pin for user-configurable Flow throught or pipelineed operation, That pin can be NC or connected to V_{CC} for pipelined operation. Refer to Pin configuration. 2. Revise the power supply charaetoristics at page 12 3. Resive the t_{KQ} of 250 MHZ from 2.5ns to 3ns. 4. Move the 100 MHZ speed grade.	August 13,2002	

256K x 32, 256K x 36, 512K x 18
8Mb S/DCD SYNCBURST Pipelined SRAMs

FEATURES

- Pipeline Mode operation
- Single/Dual Cycl Deselect
- User-selectable Output Drive Strength with XQ Mode
- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Single +3.3V, +10%, –5% core power supply
- Power-down snooze mode
- 2.5V or 3.3V I/O Supply
- Snooze MODE for reduced-power standby
- T version (three chip selects)
- D version (two chip selects)

DESCRIPTION

ICSI's 8Mb SyncBurst Pipelined SRAMs integrate a 512k x 18, 256k x 32, or 256k x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter.

Applications

The ICSI SyncBurst Pipelined SRAM family employs high-speed ,low-power CMOS designs that are fabricated using an advanced CMOS process to provide Level 2 Cache applications supporting Pentium and PowerPC microprocessors originally, the device now finds application ranging from DSP main store to networking chip set support.

FAST ACCESS TIME

	Symbol	-250	-200	-166	-133	Units
Pipeline	t_{KQ}	3	3.1	3.5	4	ns
3-1-1-1	t_{KC}	4	5	6	7.5	ns
	$I_{CC}1$	390	360	330	300	mA

Controls

All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin. The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

SCD and DCD Pipelined Reads

The device is a SCD (Single Cycle Deselect) and DCD(Dual Cycle Deselect) pipelined synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock. The user may configure this SRAM for either mode of operation using the SCD mode input on Bump 4L.

Byte Write and Global Write

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ($\overline{BWE}$).input combined with one or more individualbyte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

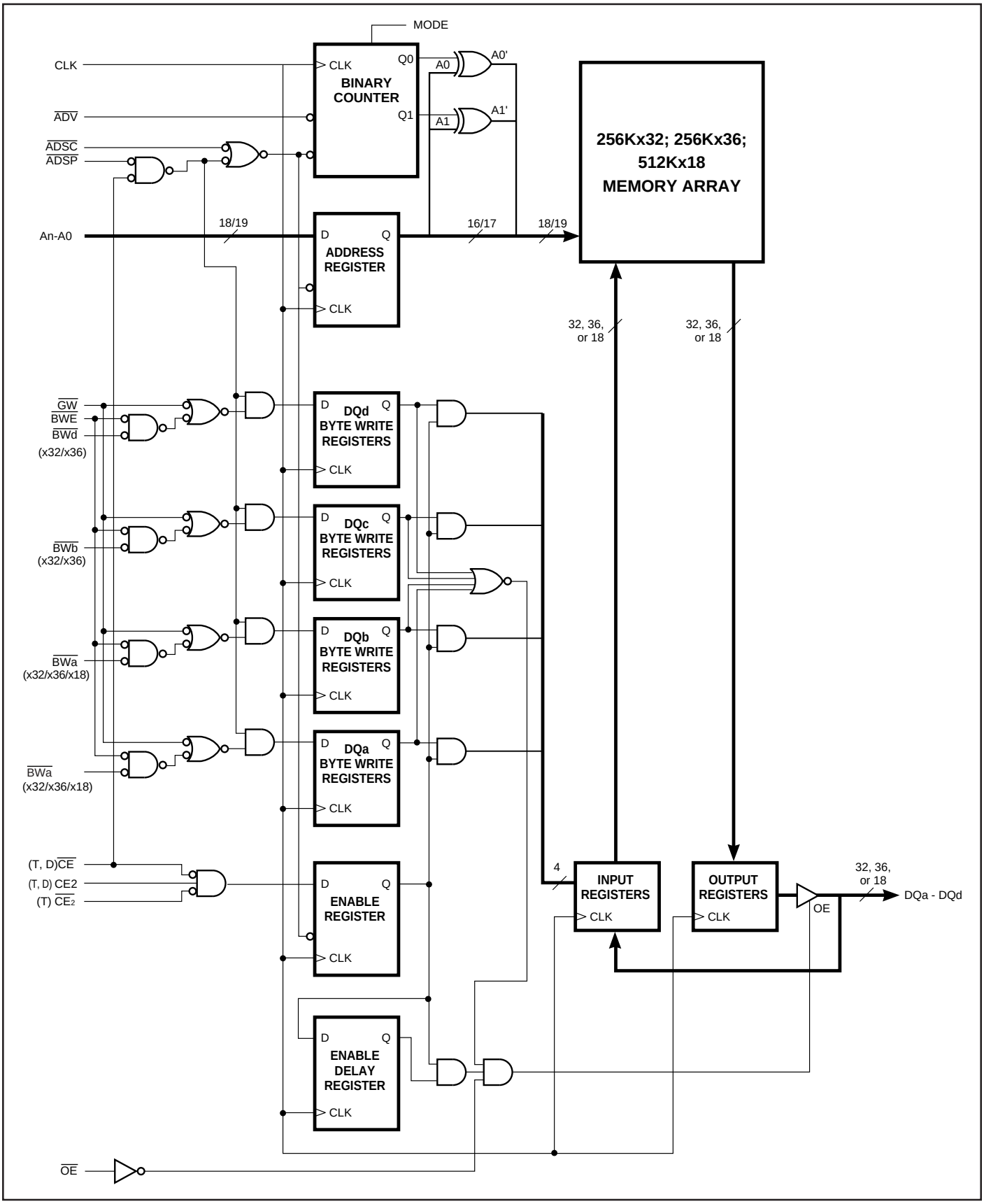
IOL/IOH Drive strength Options

The XQ pin allows selection between high drive strength (XQ low) for multi-drop bus applications and normal drive strength (XQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

Snooze Mode

Low power (Snooze mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Snooze mode.

BLOCK DIAGRAM

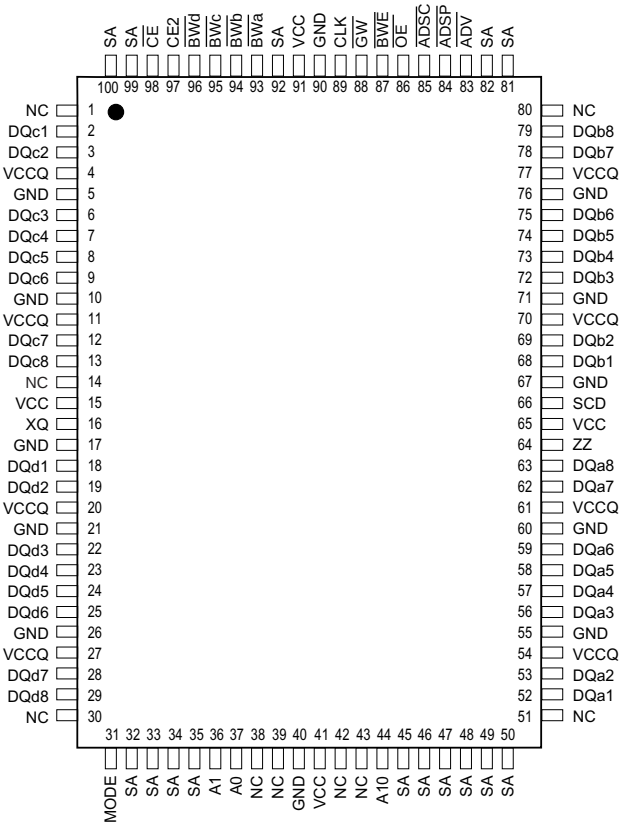


PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	SA	SA	$\overline{ADSP}$	SA	SA	VCCQ
B	NC	CE2	SA	$\overline{ADSC}$	SA	SA	NC
C	NC	SA	SA	VCC	SA	SA	NC
D	DQc1	NC	GND	XQ	GND	NC	DQb8
E	DQc2	DQc3	GND	$\overline{CE}$	GND	DQb6	DQb7
F	VCCQ	DQc4	GND	$\overline{OE}$	GND	DQb5	VCCQ
G	DQc5	DQc6	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb4	DQb3
H	DQc7	DQc8	GND	$\overline{GW}$	GND	DQb2	DQb1
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	DQd1	DQd2	GND	CLK	GND	DQa7	DQa8
L	DQd4	DQd3	$\overline{BWd}$	SCD	$\overline{BWa}$	DQa5	DQa6
M	VCCQ	DQd5	GND	$\overline{BWE}$	GND	DQa4	VCCQ
N	DQd6	DQd7	GND	A1	GND	DQa3	DQa2
P	DQd8	NC	GND	A0	GND	NC	DQa1
R	NC	SA	MODE	VCC	NC	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	VCCQ	NC	NC	NC	NC	NC	VCCQ

100-Pin TQFP (D Version)



256K x 32

Note:Ball R5 connecting to V_{CC} is acceptable

Note:pin 14 connecting to V_{CC} is acceptable

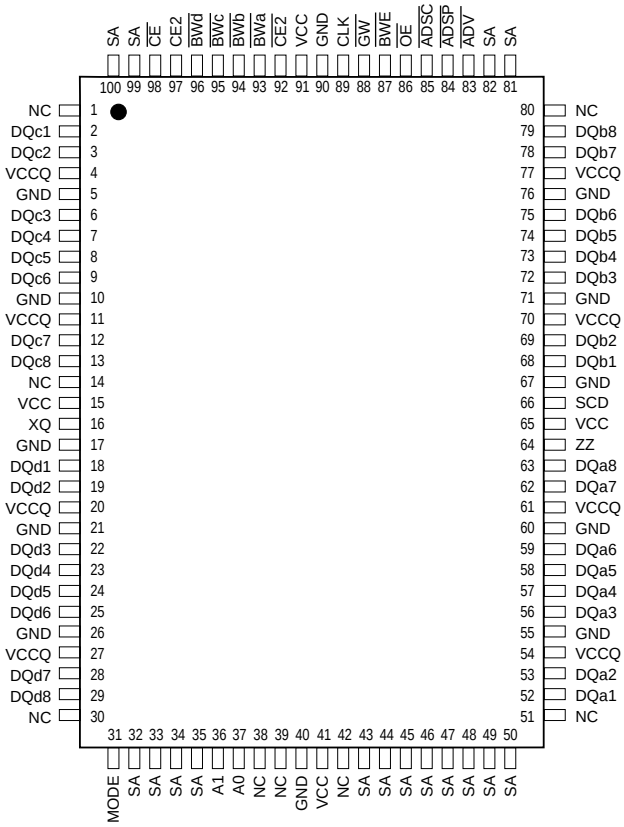
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
BWa -$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable

DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

100-Pin TQFP (T Version)



256K x 32

Note:Pin 14 connecting to Vcc is acceptable

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$ -$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$,CE2,$\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable

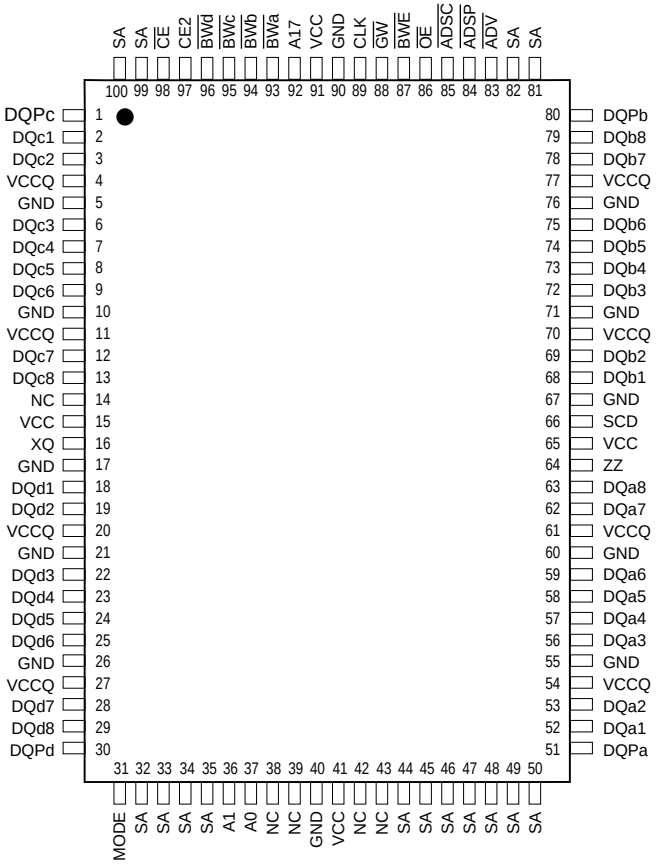
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	SA	SA	$\overline{ADSP}$	SA	SA	VCCQ
B	NC	CE2	SA	$\overline{ADSC}$	SA	SA	NC
C	NC	SA	SA	VCC	SA	SA	NC
D	DQc1	DQPc	GND	XQ	GND	DQPb	DQb8
E	DQc2	DQc3	GND	$\overline{CE}$	GND	DQb6	DQb7
F	VCCQ	DQc4	GND	$\overline{OE}$	GND	DQb5	VCCQ
G	DQc5	DQc6	$\overline{BWc}$	$\overline{ADV}$	$\overline{BWb}$	DQb4	DQb3
H	DQc7	DQc8	GND	$\overline{GW}$	GND	DQb2	DQb1
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	DQd1	DQd2	GND	CLK	GND	DQa7	DQa8
L	DQd4	DQd3	$\overline{BWd}$	SCD	$\overline{BWa}$	DQa5	DQa6
M	VCCQ	DQd5	GND	$\overline{BWE}$	GND	DQa4	VCCQ
N	DQd6	DQd7	GND	A1	GND	DQa3	DQa2
P	DQd8	DQPd	GND	A0	GND	DQPa	DQa1
R	NC	SA	MODE	VCC	NC	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	VCCQ	NC	NC	NC	NC	NC	VCCQ

100-Pin TQFP (D Version)



256K x 36

Note:Ball R5 connecting to V_{CC} is acceptable

Note:pin 14 connecting to V_{CC} is acceptable

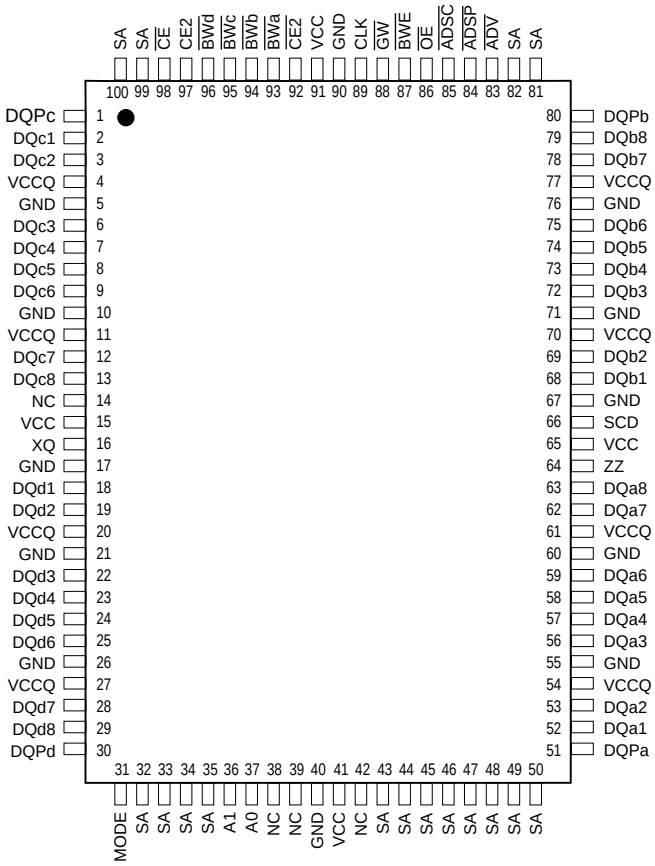
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
BWa -$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable

DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

100-Pin TQFP (T Version)



256K x 36

Note:Pin 14 connecting to Vcc is acceptable

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A17	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$ -$\overline{BWd}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$,CE2,$\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable

DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

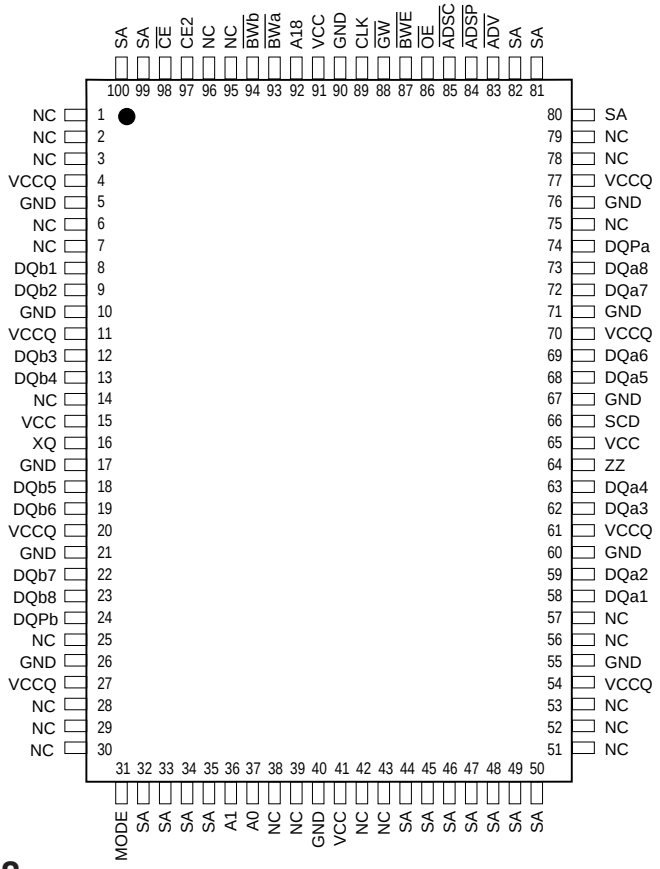
PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VCCQ	SA	SA	$\overline{ADSP}$	SA	SA	VCCQ
B	NC	CE2	SA	$\overline{ADSC}$	SA	SA	NC
C	NC	SA	SA	VCC	SA	SA	NC
D	DQc1	DQb2	GND	XQ	GND	DQPa	NC
E	NC	NC	GND	$\overline{CE}$	GND	NC	DQb8
F	VCCQ	DQc4	GND	$\overline{OE}$	GND	DQb7	VCCQ
G	NC	DQc3	$\overline{BWb}$	$\overline{ADV}$	GND	NC	DQb6
H	DQc4	NC	GND	$\overline{GW}$	GND	DQb5	NC
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	Nc	DQd5	GND	CLK	GND	NC	DQa4
L	DQd6	NC	GND	SCD	$\overline{BWa}$	DQa3	NC
M	VCCQ	DQd7	GND	$\overline{BWE}$	GND	NC	VCCQ
N	DQd8	NC	GND	A1	GND	DQa2	NC
P	NC	DQPd	GND	A0	GND	NC	DQa1
R	NC	SA	MODE	VCC	NC	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	VCCQ	NC	NC	NC	NC	NC	VCCQ

Note:Ball R5 connecting to V_{CC} is acceptable

100-Pin TQFP (D Version)



Note:pin 14 connecting to V_{CC} is acceptable

512K x18

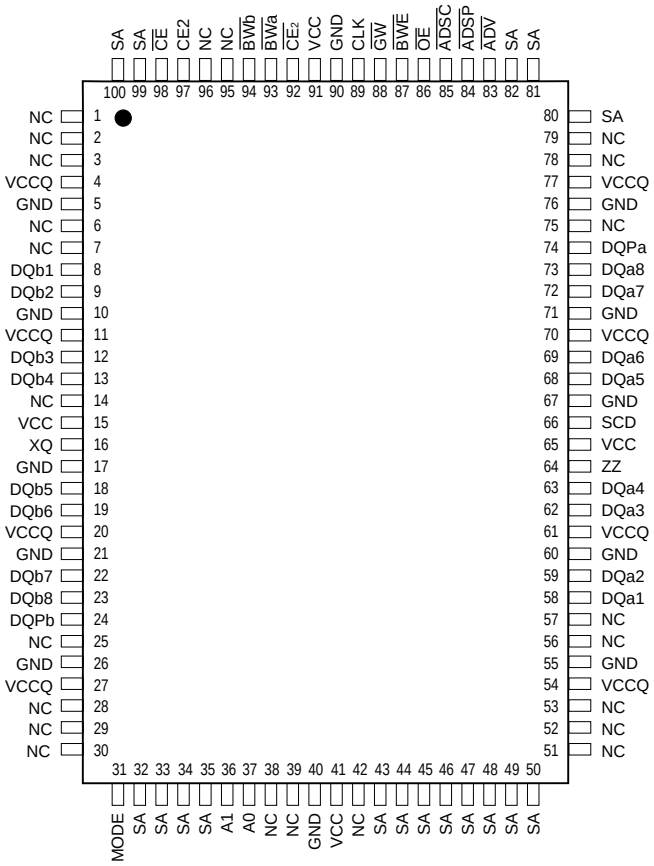
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$ -$\overline{BWb}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable

DQa-DQb	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPb	Parity Data I/O DQPa is parity for DQa1-8;DQPb is parity for DQb1-8

PIN CONFIGURATION

100-Pin TQFP (T Version)



512K x18

Note:Pin 14 connecting to Vcc is acceptable

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A18	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$ -$\overline{BWb}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$,CE2,$\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable

DQa-DQb	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
SCD	Single Cycle Deselect/Dual Cycle Deselect Mode Control
XQ	Output Drive Control
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply : +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPb	Parity Data I/O DQPa is parity for DQa1-8;DQPb is parity for DQb1-8

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	MODE	L	Linear Burst
		H or NC	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby
Single/Dual Cycle Deselect Control	SCD	L	Dual Cycle Deselect
		H or NC	Single Cycle Deselect
Output Drive Control	XQ	L	High Drive (Low Impedance)
		H	Low Drive (High Impedance)

Note:
There are pull-up devices on the MODE, XQ, and SCD pins and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

TRUTH TABLE

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

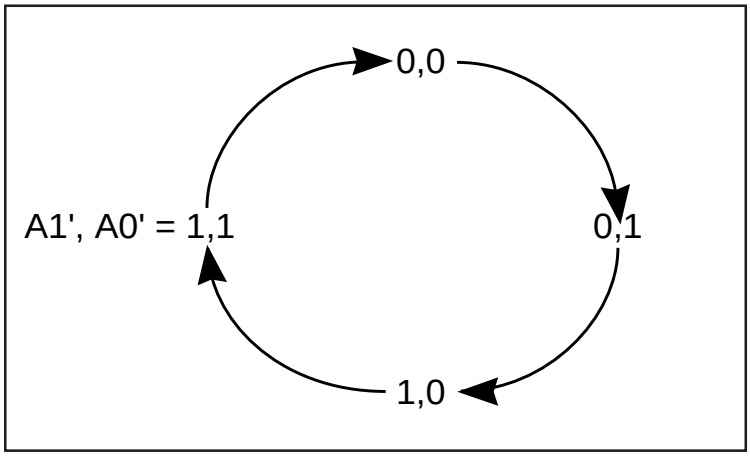
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = VCC or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{CCQ} + 0.5	V
V_{IN}	Voltage Relative to GND for	–0.5 to V_{CC} + 0.5	V
	for Address and Control Inputs		
V_{CC}	Voltage on Vcc Supply Relatiive to GND	–0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause perma-nent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	Vcc	VccQ
Commercial	0°C to +70°C	3.3V, +10%, –5%	2.375–3.6V
Industrial	–40°C to +85°C	3.3V, +10%, –5%	2.375–3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CCQ} = 2.5V	1.7	—	V
		I_{OH} = –4.0 mA, V_{CCQ} = 3.3V	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA, V_{CCQ} = 2.5V	—	0.7	V
		I_{OL} = 8.0 mA, V_{CCQ} = 3.3V	—	0.4	V
V_{IH}	Input HIGH Voltage	V_{CCQ} = 2.5V	1.7	V_{CCQ}+ 0.3	V
		V_{CCQ} = 3.3V	2.0	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CCQ} = 2.5V	–0.3	0.7	V
		V_{CCQ} = 3.3V	–0.3	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} (1)	–2	2	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}Q, $\overline{OE}$ = V_{IH}	–2	2	µA

Notes:
1. The MODE, ZZ, SCD, XQ, pin has an internal pullup. and input leakage = ±10 µA .

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Parameter	Test Conditions	Symbol		-250 Max.	-200 Max.	-166 Max.	-133 Max.	Unit
AC Operating	Device Selected,	I_{CC}1	Com.	390	360	330	300	mA
Supply Current	All Inputs ≤ V_{IL} or ≥V_{IH}		Ind.	410	380	350	320	
	f = 1/t_{KC}							
Clock Running	Device Deselected,	Icc2	Com.	110	100	90	85	mA
	V_{CC} = Max.,		Ind.	130	120	110	105	mA
	All Inputs ≤ V_{IL} or ≥V_{IH}							
	f = 1/t_{KC}							
COMS Standby	Device Deselected,	I_{SB}	Com.	90	90	90	90	mA
	V_{CC} = Max.,		Ind.	100	100	100	100	mA
	All Inputs ≤ 0.2V or ≥V_{CC} -0.2V							
	f = 0							
Power Dowin Mode	V_{CC} = Max	I_{ZZ}	Com.	80	80	80	80	mA
	ZZ ≥V_{CC} - 0.2V		Ind.	90	90	90	90	mA
	f = 0							
	All input ≤ 0.2V or ≥V_{CC} -0.2V							

CAPACITANCE (1,2)

Symbol	Parameter Conditions	Max.	Unit	
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V for 3.3V I/O $V_{CC}Q$/2V for 2.5V I/O
Output Load	See Figures 1 and 2

AC TEST LOADS

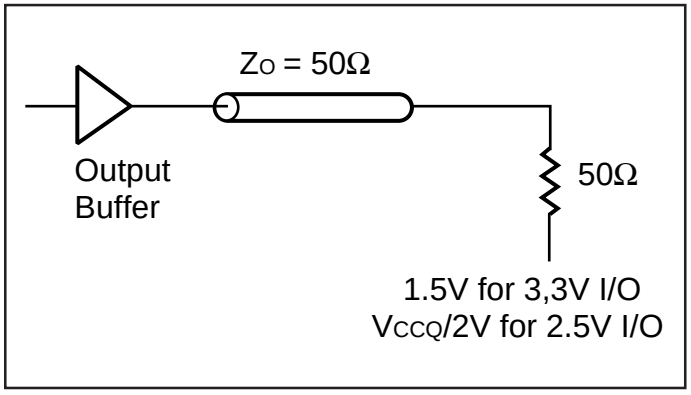


Figure 1

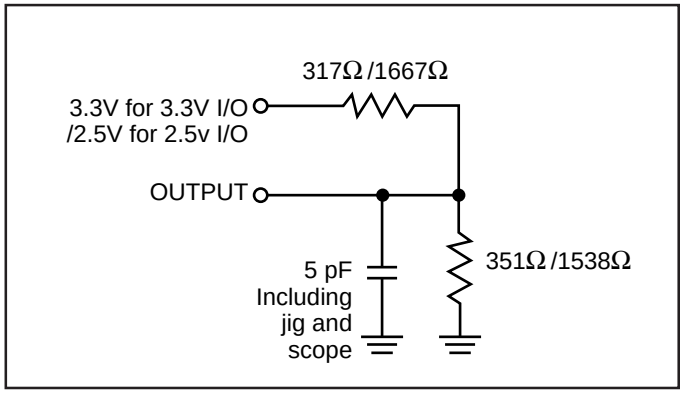


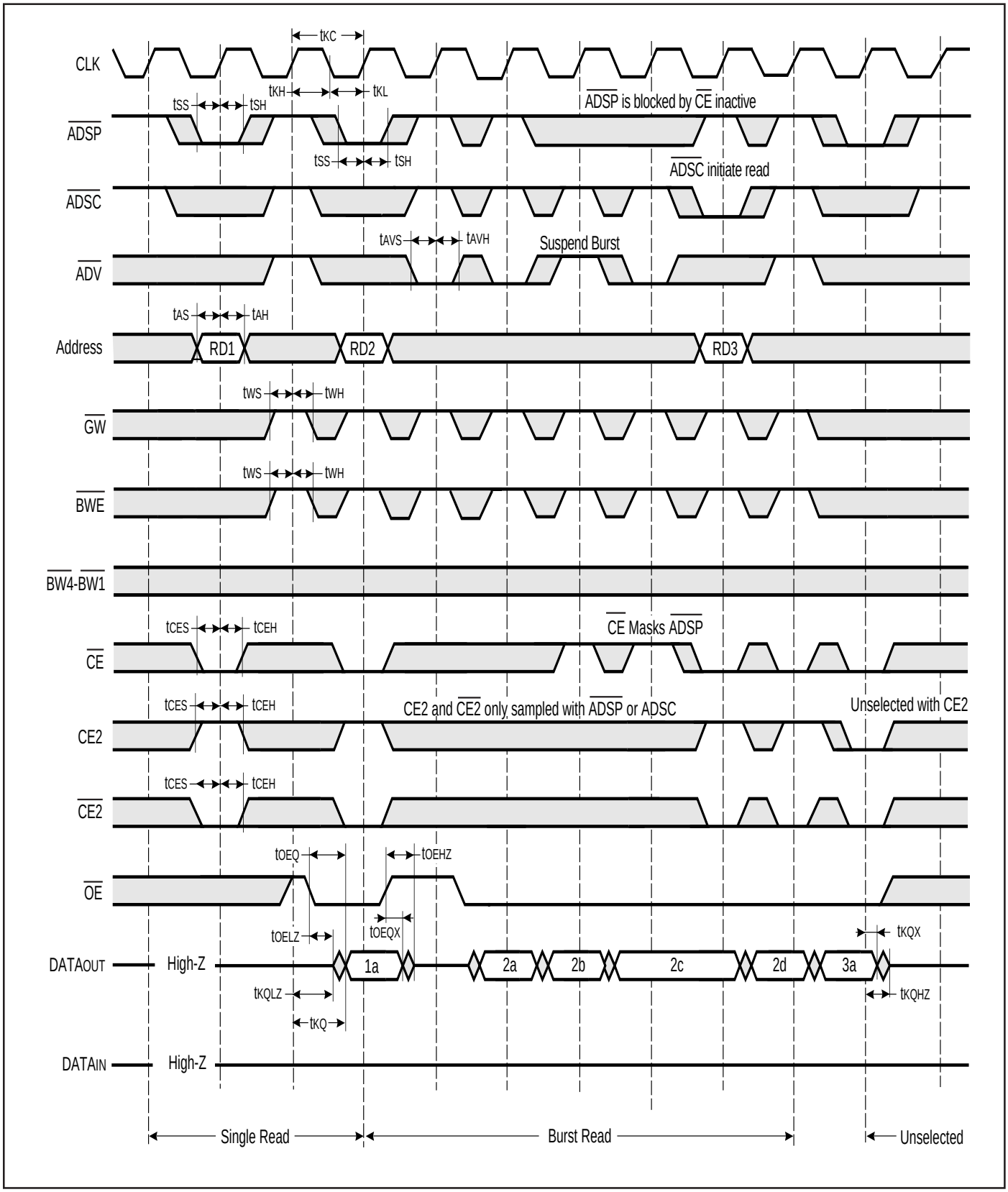
Figure 2

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

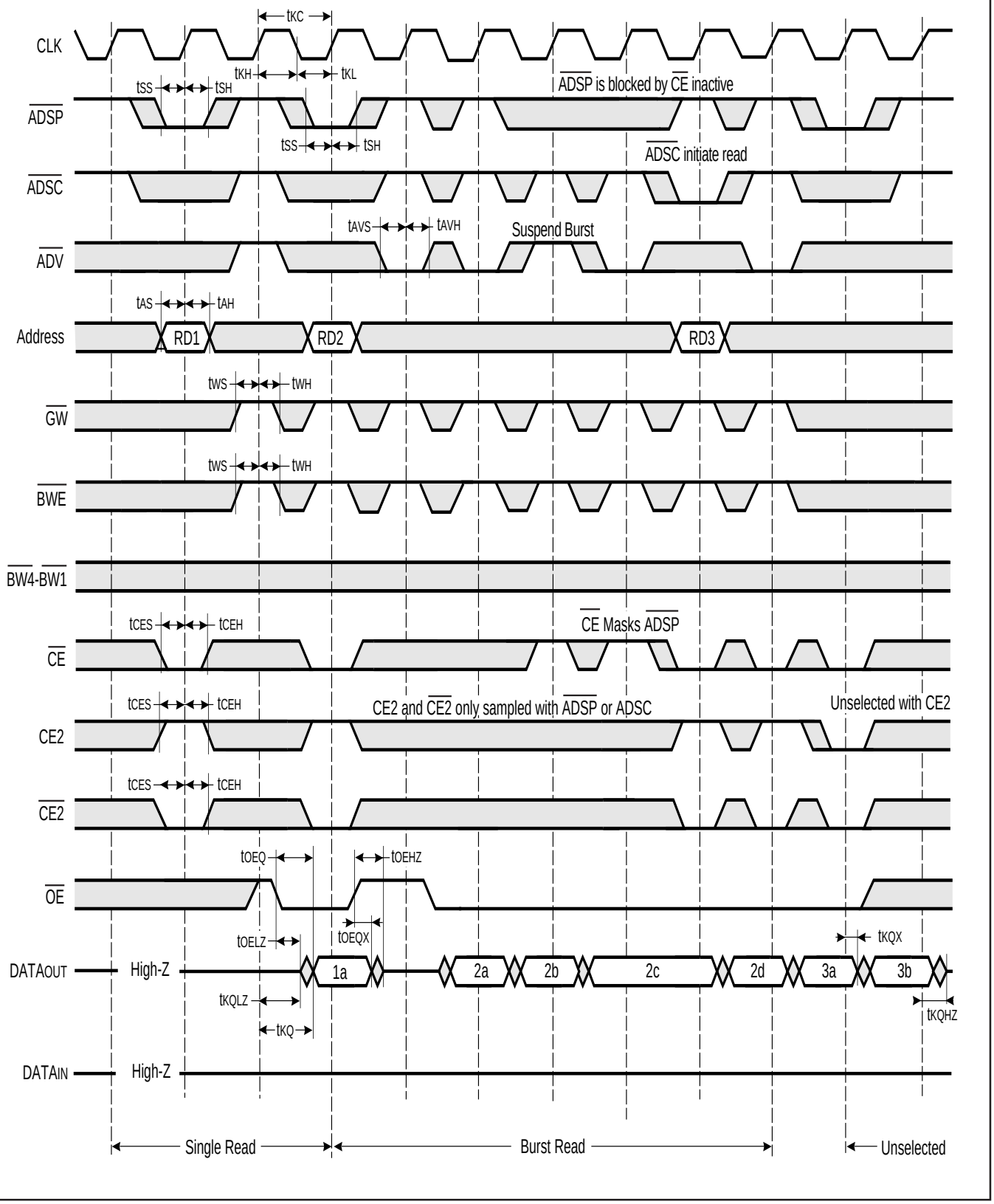
			-250		-200		-166		-133		
	Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Pipeline	t_{KC}	Cycle Time	4	—	5	—	6	—	7.5	—	ns
	t_{KQ}	Clock Access Time	—	3	—	3.1	—	3.5	—	4	ns
	t_{KQX}(1)	Clock High to Output Invalid	1.0	—	1.0	—	1.5	—	1.5	—	ns
	t_{KQLZ}(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	ns
	t_{KH}	Clock High Pulse Width	1.6	—	2	—	2.3	—	2.8	—	ns
	t_{KL}	Clock Low Pulse Width	1.6	—	2	—	2.3	—	2.8	—	ns
	t_{KQHZ}(1,2)	Clock High to Output High-Z	—	3.1	—	3.1	—	3.5	—	4	ns
	t_{OEQ}	Output Enable to Output Valid	—	3.1	—	3.1	—	3.5	—	4	ns
	t_{OELZ}(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	ns
	t_{OEHZ}(1,2)	Output Enable to Output High-Z	—	3.0	—	3.0	—	3.5	—	4	ns
	t_{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns
	t_{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns
	t_{WS}	Write Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns
	t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns
	t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	ns
	t_{DS}	Data Setup time	1.5	—	1.5	—	1.5	—	1.5	—	ns
	t_{DH}	Data Hold time	0.5	—	0.5	—	0.5	—	0.5	—	ns
	t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
	t_{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
	t_{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
	t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
	t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	ns
	t_{ZZS}	ZZ Setup Time	2	—	2	—	2	—	2	—	cyc
	t_{ZZREC}	ZZ Recovery Time	2	—	2	—	2	—	2	—	cyc

Note:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

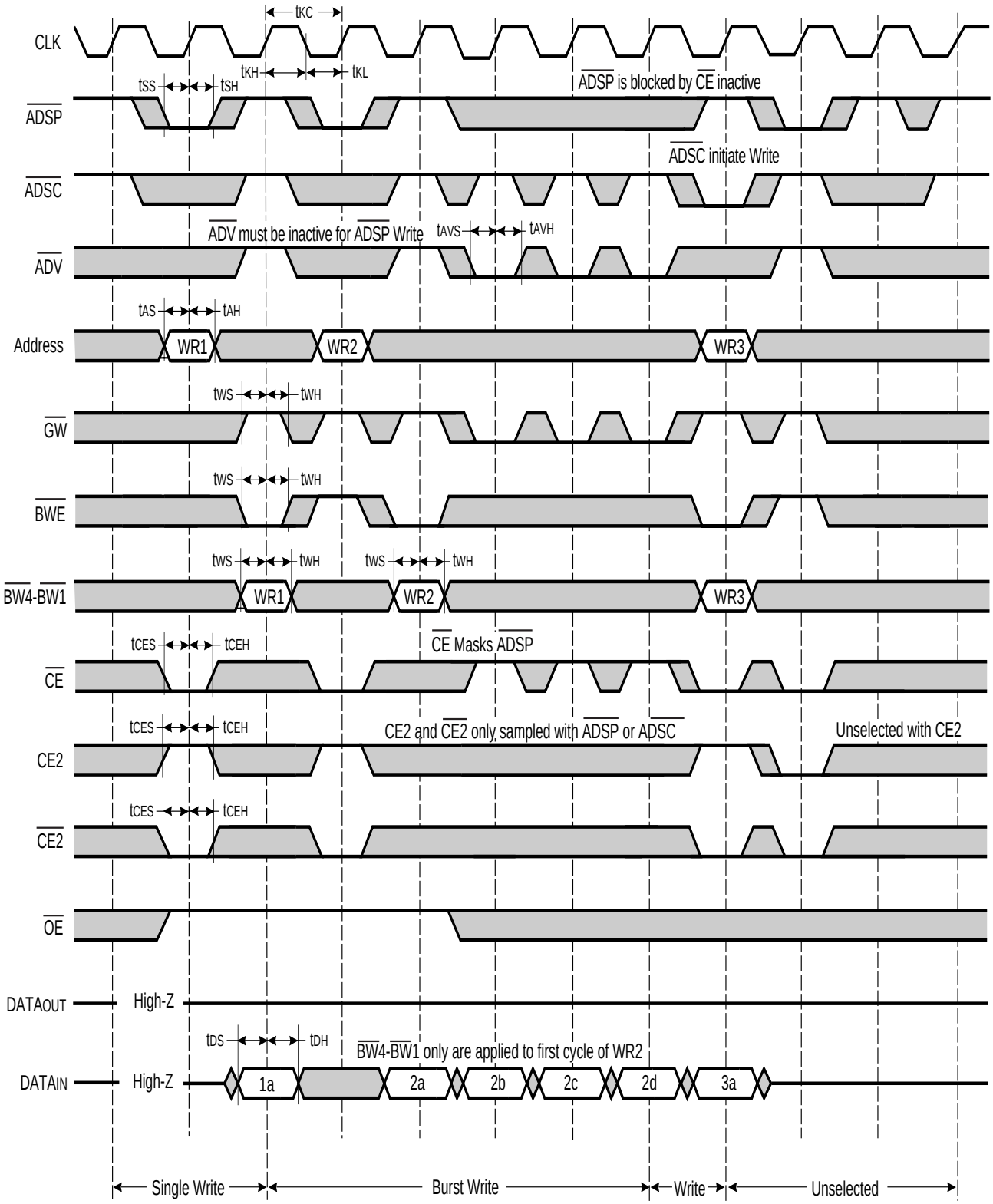
PIPELINED SCD READ CYCLE TIMING



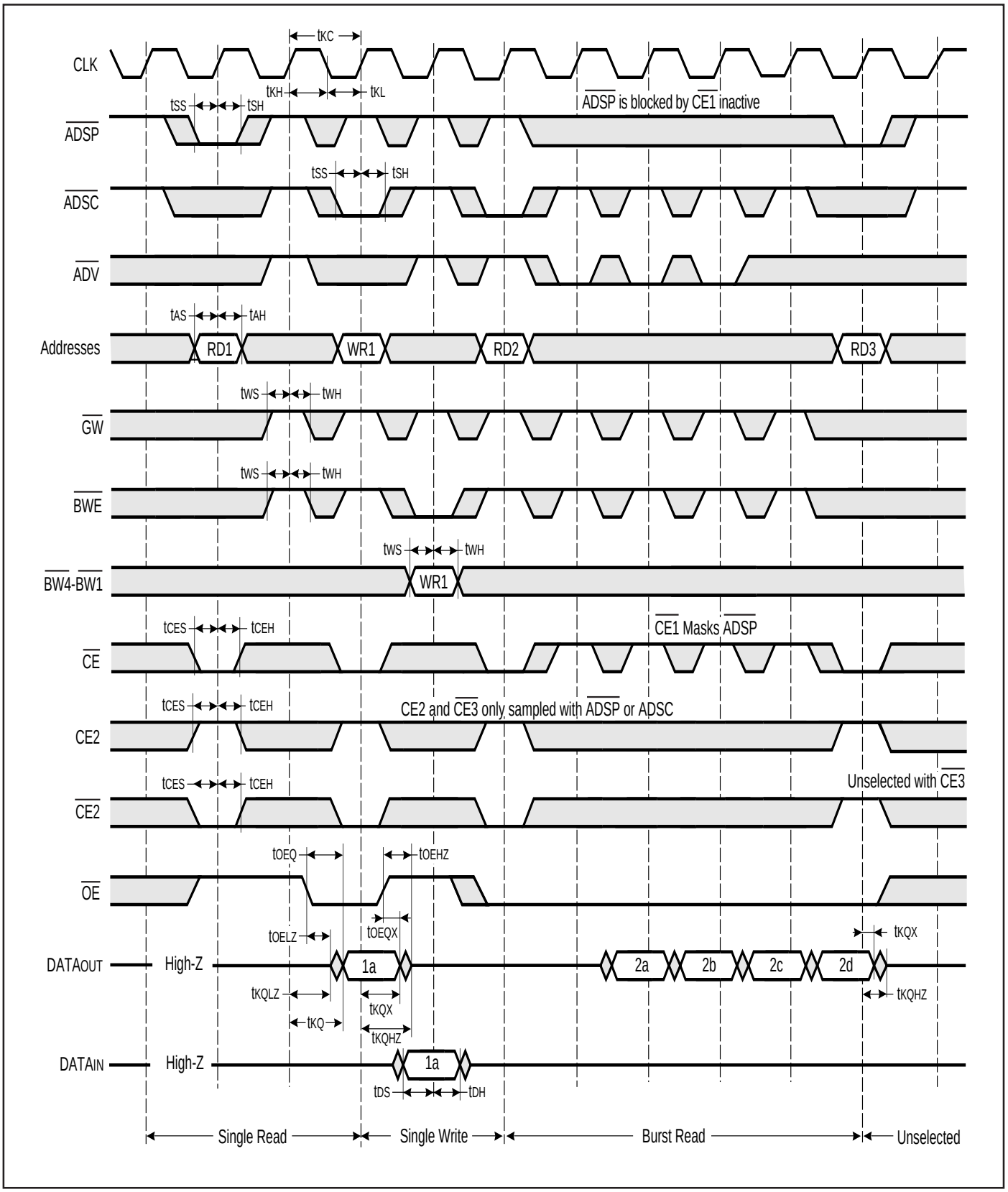
PIPELINED DCD READ CYCLE TIMING



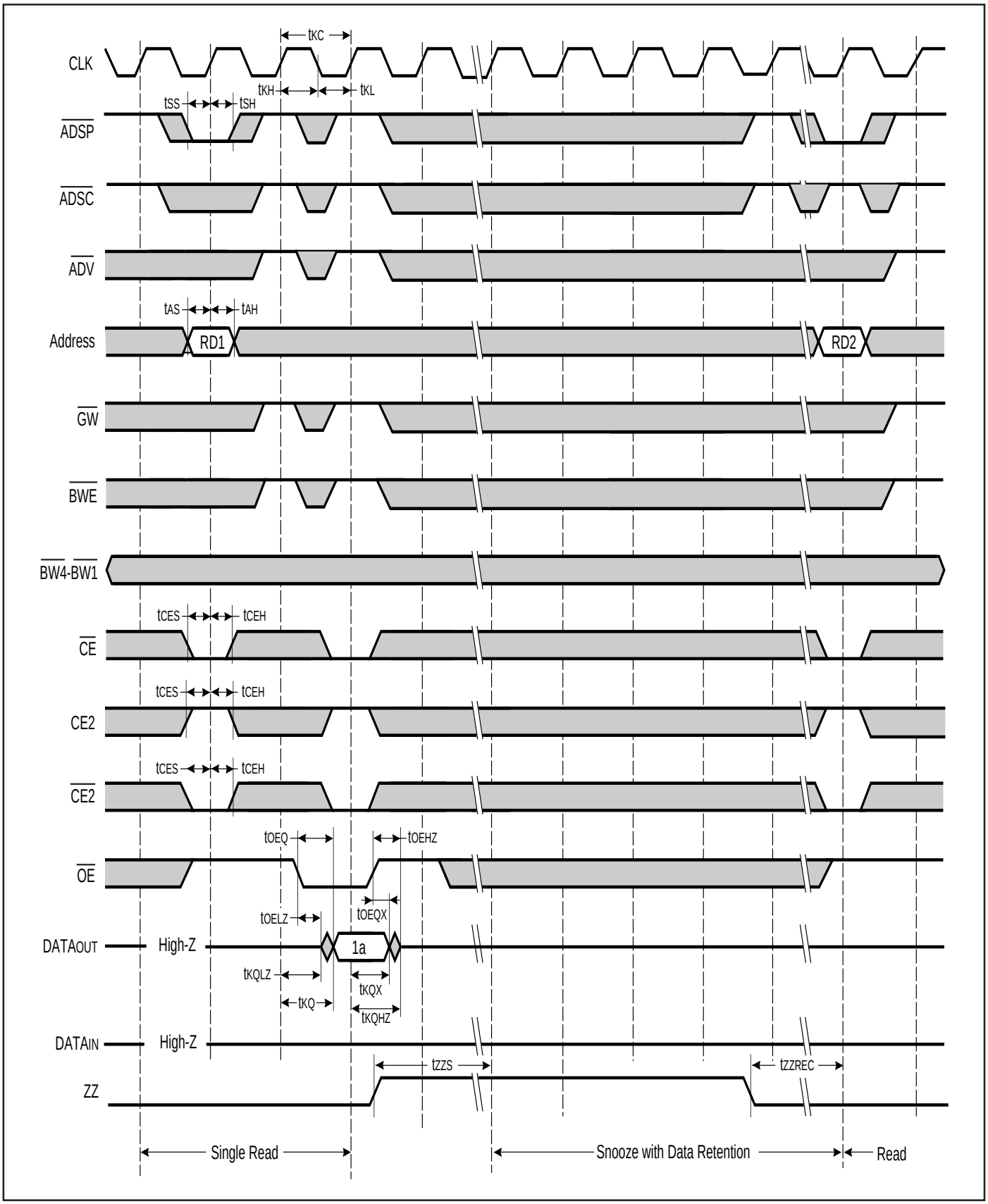
WRITE CYCLE TIMING



READ/WRITE CYCLE TIMING: PIPELINED



SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
250 MHz	IC61S25632T-250TQ	14*20*1.4mm LQFP
	IC61S25632D-250TQ	14*20*1.4mm LQFP
	IC61S25632D-250B	14*22mm PBGA
200 MHz	IC61S25632T-200TQ	14*20*1.4mm LQFP
	IC61S25632D-200TQ	14*20*1.4mm LQFP
	IC61S25632D-200B	14*22mm PBGA
166 MHz	IC61S25632T-166TQ	14x20x1.4mm LQFP
	IC61S25632D-166TQ	14x20x1.4mm LQFP
	IC61S25632D-166B	14*22mm PBGA
133 MHz	IC61S25632T-133TQ	14x20x1.4mm TQFP
	IC61S25632D-133TQ	14x20x1.4mm TQFP
	IC61S25632D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S25636T-250TQ	14*20*1.4mm LQFP
	IC61S25636D-250TQ	14*20*1.4mm LQFP
	IC61S25636D-250B	14*22mm PBGA
200 MHz	IC61S25636T-200TQ	14*20*1.4mm LQFP
	IC61S25636D-200TQ	14*20*1.4mm LQFP
	IC61S25636D-200B	14*22mm PBGA
166 MHz	IC61S25636T-166TQ	14x20x1.4mm LQFP
	IC61S25636D-166TQ	14x20x1.4mm LQFP
	IC61S25636D-166B	14*22mm PBGA
133 MHz	IC61S25636T-133TQ	14x20x1.4mm TQFP
	IC61S25636D-133TQ	14x20x1.4mm TQFP
	IC61S25636D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S51218T-250TQ	14*20*1.4mm LQFP
	IC61S51218D-250TQ	14*20*1.4mm LQFP
	IC61S51218D-250B	14*22mm PBGA
200 MHz	IC61S51218T-200TQ	14*20*1.4mm LQFP
	IC61S51218D-200TQ	14*20*1.4mm LQFP
	IC61S51218D-200B	14*22mm PBGA
166 MHz	IC61S51218T-166TQ	14x20x1.4mm LQFP
	IC61S51218D-166TQ	14x20x1.4mm LQFP
	IC61S51218D-166B	14*22mm PBGA
133 MHz	IC61S51218T-133TQ	14x20x1.4mm TQFP
	IC61S51218D-133TQ	14x20x1.4mm TQFP
	IC61S51218D-133B	14*22mm PBGA

Industrial Range: -40°C to 85°C

Speed	Order Part Number	Package
250 MHz	IC61S25632T-250TQI	14*20*1.4mm LQFP
	IC61S25632D-250TQI	14*20*1.4mm LQFP
	IC61S25632D-250B	14*22mm PBGA
200 MHz	IC61S25632T-200TQI	14*20*1.4mm LQFP
	IC61S25632D-200TQI	14*20*1.4mm LQFP
	IC61S25632D-200B	14*22mm PBGA
166 MHz	IC61S25632T-166TQI	14x20x1.4mm LQFP
	IC61S25632D-166TQI	14x20x1.4mm LQFP
	IC61S25632D-166B	14*22mm PBGA
133 MHz	IC61S25632T-133TQI	14x20x1.4mm TQFP
	IC61S25632D-133TQI	14x20x1.4mm TQFP
	IC61S25632D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S25636T-250TQI	14*20*1.4mm LQFP
	IC61S25636D-250TQI	14*20*1.4mm LQFP
	IC61S25636D-250B	14*22mm PBGA
200 MHz	IC61S25636T-200TQI	14*20*1.4mm LQFP
	IC61S25636D-200TQI	14*20*1.4mm LQFP
	IC61S25636D-200B	14*22mm PBGA
166 MHz	IC61S25636T-166TQI	14x20x1.4mm LQFP
	IC61S25636D-166TQI	14x20x1.4mm LQFP
	IC61S25636D-166B	14*22mm PBGA
133 MHz	IC61S25636T-133TQI	14x20x1.4mm TQFP
	IC61S25636D-133TQI	14x20x1.4mm TQFP
	IC61S25636D-133B	14*22mm PBGA

Speed	Order Part Number	Package
250 MHz	IC61S51218T-250TQI	14*20*1.4mm LQFP
	IC61S51218D-250TQI	14*20*1.4mm LQFP
	IC61S51218D-250B	14*22mm PBGA
200 MHz	IC61S51218T-200TQI	14*20*1.4mm LQFP
	IC61S51218D-200TQI	14*20*1.4mm LQFP
	IC61S51218D-200B	14*22mm PBGA
166 MHz	IC61S51218T-166TQI	14x20x1.4mm LQFP
	IC61S51218D-166TQI	14x20x1.4mm LQFP
	IC61S51218D-166B	14*22mm PBGA
133 MHz	IC61S51218T-133TQI	14x20x1.4mm TQFP
	IC61S51218D-133TQI	14x20x1.4mm TQFP
	IC61S51218D-133B	14*22mm PBGA

Integrated Circuit Solution Inc.
HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.
TEL: 886-3-5780333
Fax: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.
TEL: 886-2-26962140
FAX: 886-2-26962252
http://www.icsi.com.tw